Stable Time Reduction by LDO in PWM Switching Buck Converter

Jun-Hong Weng, Wen-Ting Lu, Kuan-Chou Chen, Wei-Han Huang

***Abstract*-- In this paper, the proposed voltage mode buck converter senses. The output voltage is compared with the reference voltage, and the error voltage is amplified by the error amplifier. Finally, through the PWM signal to achieve the circuit regulator effect. Compared with the current mode buck converter, the voltage-mode buck converter has better noise margin, low impedance power output and single feedback loop, making design and circuit analysis easier. The addition of the LDO circuit allows the buck converter to reach a stable voltage faster and turn off the LDO after the buck converter is stable to reduce unnecessary power waste.**

I. INTRODUCTION

With the development of portable electronic products, low power and high efficiency to become the primary test of portable electronic products. So that these electronic circuits that use the battery to supply power must operate at low voltage and low current to reduce energy consumption, allowing the battery to work for a long time. In addition, while the process technology continues to improve, due to the reliability of the consideration, the working voltage must also be reduced with the progress of the process, in order to save power consumption, the regulator is often used to reduce the operating voltage.

This paper presents a DC-DC converter that combines LDO to improve efficiency. Because the buck converter have to take an amount of time when the voltage reaches the desired stable output voltage, the LDO used to achieve the desired output voltage during this time. When the buck converter reaches a steady voltage, the LDO turned off to reduce power waste. When the LDO as an output voltage with low output voltage ripple and no EMI problem, in the buck converter as the output voltage when there is a better efficiency there is a wide input voltage range.

This voltage-mode switching regulator fabricated with TSMC 0.18um 3.3V CMOS process. In the proposed buck converter, the loading current is form 0.001A to 0.1A, and the efficiency is 90.1%. The line regulation and load regulation are 0.24mV/V and 0.11mV/mA respectively. The core area is 0.864 x 0.441 mm2.

II. CIRCUIT ARCHITECTURE

Fig.1 shows the system architecture of the proposed DC-DC converter that combines LDO. It consists of a buck DC-DC converter, a LDO, and a digital control circuit and off-chip LC components. Due to the buck DC-DC converter use voltage mode, its stability will be worse than the current mode, so we added the PID compensation technique to ensure the stability of buck DC-DC converter. Rf1 and Rf2 sense the output voltage Buck_Vo and provide a feedback voltage Vfb to the buck. The feedback voltage Vfb with the soft-start circuit output voltage is amplified by error amplifier. Finally, through the PWM circuit output signal to achieve the required output voltage. After throughing the digital control circuit, the output voltage can be determined by buck converter or LDO. Because the LDO has less time to achieve the stability voltage than buck converter. During buck converter achieving the stability voltage, the output voltage is supplied by LDO. When the buck converter reach the required output voltage then turn off LDO.

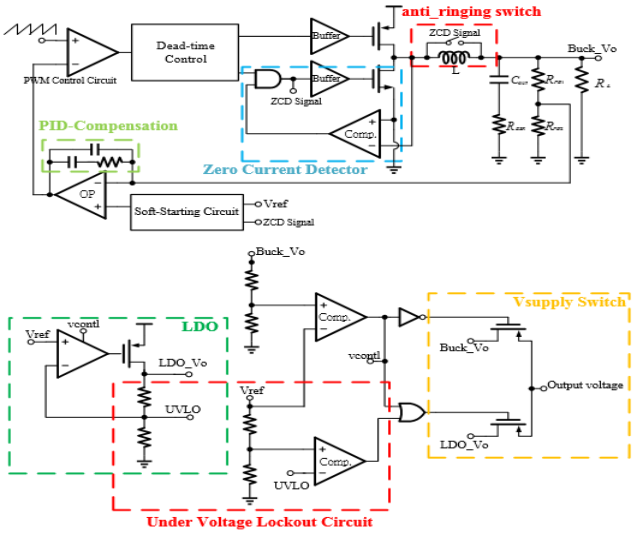

Fig. 1 Proposed DC-DC converter combine LDO

A. Soft-Starting Circuit

Fig. 2 show the Soft-Start circuit is used to avoid the moment when the switching converter is started. Since the output inductor has not yet formed an electric field, the power transistor has a great instantaneous current conduction [1]. So the soft-start circuit will be used to limit the reference voltage output to a linear climb voltage.

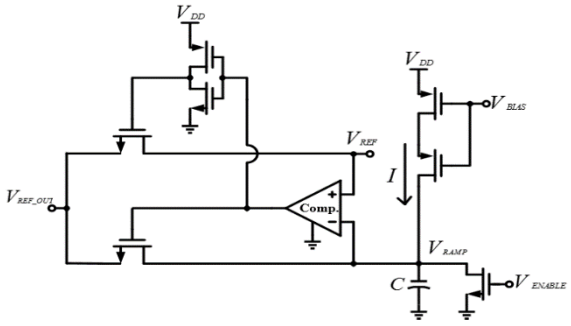

Fig. 2 Soft-Starting Circuit

The capacitor C is charged with a very small current I so that V_RAMP is a gradually rising voltage. When V_RAMP and V_REF are different, the V_RAMP voltage determines the output voltage.

B. Zero Current Detector Circuit

Fig. 3 show the Zero Current Detector circuit. When using a synchronous switching regulator, the N-type power transistor replaces the traditional diode to provide the load current. However, the N-type power transistor does not have the reverse bias characteristic of the diode. So the inductor current discharge will result in the output capacitor through the output inductor and N-type power transistor to the ground, resulting in the output capacitor on the charge caused by additional power consumption, in order to prevent this situation need to use zero current detection circuit[2].

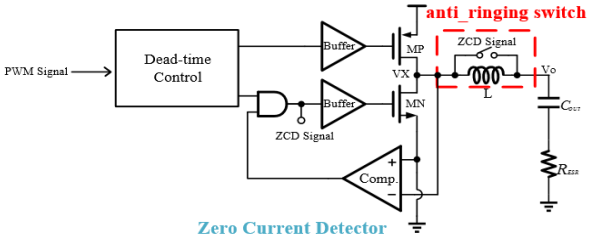

Fig. 3 Zero Current Detector Circuit

III. GCONCLUSION

Fig. 4 show the result of finally output voltage. First the finally output voltage is supplied by LDO when buck converter is in unstable state. When the buck reaches the stabilized voltage, the digital control circuit make a signal (V_contl) to turn off the LDO, and the BUCK output voltage is used as the final output voltage.

In this paper, add the structure of Soft-Start Circuit and Zero Current Detector Circuit to reduce the problems that may arise with traditional bucks and make the circuit more stable. The circuit of voltage mode buck converter can operate in the frequency range of 0.5MHz ~ 0.8MHz, load current range of 0.001A ~ 0.1A, the conversion efficiency is 90.1%, while the load regulation is 0.11mV / mA, line regulation is 0.24mV / V, and the output ripple < 20mV. It can be faster achieve stable voltage than the traditional buck converter by adding the LDO.

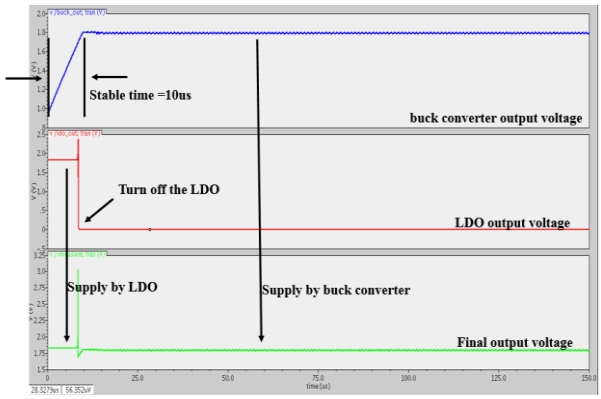

Fig. 4 simulation buck converter and LDO at output voltage=1.8 V

A. Circuit layout

The proposed DC-DC converter that combines LDO was mode switching regulator is fabricated with TSMC 0.18um 3.3V CMOS process. The chip circuit layout is shown in Fig. 5. The core area is 0.864 x 0.441 mm2.

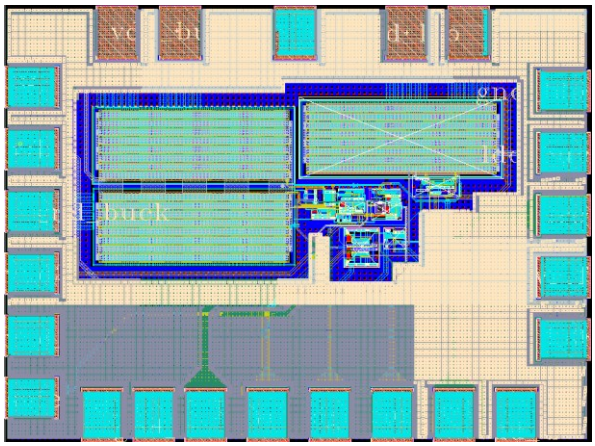

Fig. 5 Circuit layout

B. TABLE I Comparison with other works

	[3]	[4]	[5]	This work
Process	AMS 0.6um	TSMC 0.18um	TSMC 0.25um	TSMC 0.18um
Sensing-mode	Current-mode	Current-mode	Voltage-mode	Voltage-mode
Supply voltage(V)	1.2~2	2.4~4.6	2.5~5	2.5~4
Output voltage(V)	1	1	1.8	1.8
Frequency(MHz)	0.5	0.7~1.4	0.5~0.8	0.5~0.8
Load Regulation(mV/mA)	0.31	0.0107	1.875	0.11
Efficiency (%)	>89	91.16	89.65%	90.1
Load current(mA)	50~120	50~500	300	1~100
Output ripple(mV)	N/A	40	77.6@800KHz	20

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IV. REFERENCES

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