Integrated Phase Locked Loop and ILFD with VCO for Robotics Transmitter

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***Abstract*—This article presents phase locked loop (PLL) using frequency expansion technique. The oscillator uses a cross-coupled nMOSFET pair in shunt with the LC-resonator. The wide locking range divide-by-2 RLC injection-locked frequency divider (ILFD) is based on a cross-coupled oscillator. The RLC resonator is used to extend the locking range so that dual-band locking ranges can be merged in one locking range at both low and high injection powers. By utilizing pulse interpolation, the proposed architecture is capable of suppressing high-order harmonics of the reference spur as well as fundamental spur. Varactors in series with inductors are used to tune the oscillator frequency. In robotics implementation, a four-stage pulse interpolator achieves 6-dB additional spur suppression.**

I. INTRODUCTION

Periodic disturbance on the input of the voltage-controlled oscillator (VCO) in a PLL generates large reference-spur and spur harmonics, these spurs are mixed with various interferers leading to degradation of the overall system performance [1]. Therefore, research of suppressing reference spur is very popular recently [2]. Fig. 1 shows block diagram of a conventional phase locked loop [3]. The architecture using frequency expansion is shown in Fig. 2. Divide-by-2 injection-locked frequency dividers (ILFDs) [4–6] are a popular functional block in high-speed phase locked loops and other wireless transceivers. In the past, many divide-by-2 ILFD have been proposed. The injection device in an ILFD can be in series with cross-coupled transistor, and the popular ILFD is designed with a direct-cross-coupled VCO with a direct-injection MOSFET in shunt with a parallel LC resonator [4]. A dual-resonance resonator ÷2 ILFD [7, 8] has been shown to have two non-overlapped locking ranges at a fixed bias condition, and the locking range has the dual-band property.

II. INTEGRATED CIRCUITS DESIGN

A. Phase Locked Loop

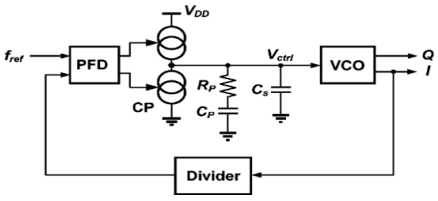

Fig.1. Schematic of a conventional PLL.

Fig. 2 shows the schematic of proposed PLL using frequency expansion technique. The PLL consists of VCO, loop filter, charge pump, phase-frequency detector (PFD), lock detector (LD), pulse-interpolator (PI), differential-single-ended converter, ÷60 frequency divider, and differential cascode voltage switch logic with resistive enhancement (DCVSL-R) [9] divider.

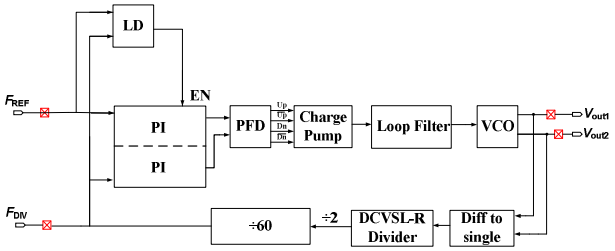

Fig.2. Block diagram of proposed PLL with pulse-interpolator (PI).

B. Proposed VCO

Fig. 3 is the designed circuit of CMOS VCO. (M_1, M_2) is the cross-coupled pair with capacitors (C_1, C_2) are capacitive cross-coupled transistors, which are used to generate negative resistance and neutralize the energy loss of the LC-resontar .

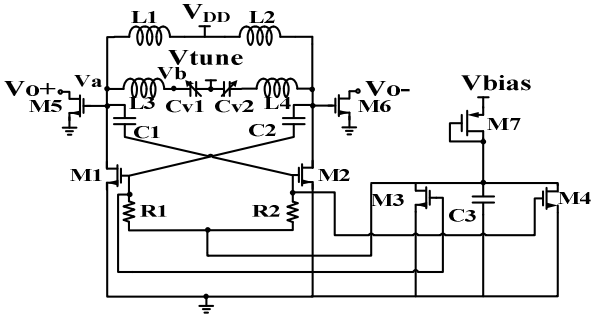

Fig.3. Schematic of the designed VCO.

C. Injection-locked Frequency Divider

Fig. 4 shows the schematic of the proposed ÷2 LC ILFD, which is composed of an injection MOS and a voltage controlled oscillator (VCO) consisted of a RLC resonator and a cross-coupled pair (M1, M2) to generate negative resistance to compensate for the resistive RLC-tank loss. Transistor M3 is the injection MOSFET with a dc gate bias Vinj. An injection signal is ac-coupled to the gate of M3. Transistors (M5, M4) are buffers biased at Vbuf through bonding wires. The RLC resonator consists of the inductors L1 (L2–L5), resistors (R1–R4), varactors (Cv1–Cv4) and parasitic active capacitor Cp, which is across the drains of the switching pair. The voltages VT1 and VT2 are used to vary the capacitance of varactors. The voltage VT1 and VT2 are applied to the varactors through the bonding wires. The RLC resonator has three resonant frequencies, and depending upon the bias condition and

component values, the ILFD can have the property of second-order resonator, fourth-order resonator or sixth-order resonator. The nonlinear analysis of a dual-band double-tuned LC VCO [10] is helpful for the understanding of ILFD operation.

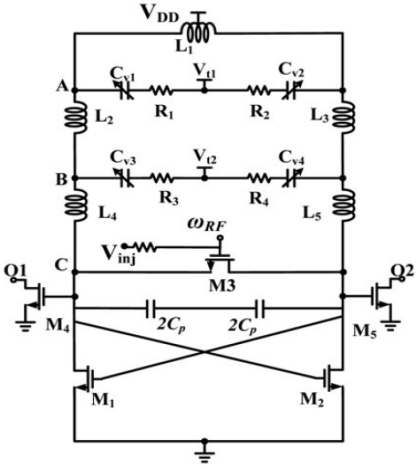

Fig. 4. Schematic of the ÷2 proposed ILFD

III. Measured Results

Table II illustrates performance comparison of PLLs. Integrated design of phase locked loop and ILFD with VCO for robotics wireless transmitter as shown in Fig. 5.

TABLE I. Performance Comparison of PLLs

Ref.	*Tech.* (μm)	Phase Noise(dBc/Hz) @1MHz offset	V_{DD} (V)	P_{diss} (mW)	Size (mm^2)	Ref Spur (dBc)
[11]	*0.18*	-122.4*	1.8	7*	0.86	--
[3]	*0.18*	-106	0.6	14.4	1.68	-39.83
[9]	*0.18*	-95	1.8	8.3*	0.56	-40
[2]	*0.18*	-	1.8	29.7	-	-
This	*0.18*	-113.2	1.8	24.2	0.72	-43.37

* Only VCO

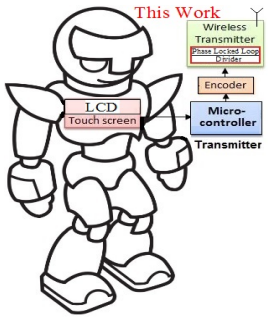

Fig.5. Integrated block of design for AI robotics wireless transmitter

IV. Conclusions

This article presents a 1.8V phase locked loop (PLL) using frequency expansion technique, which has been successfully implemented in the TSMC 0.18μm CMOS process. The PLL uses pulse-interpolator and lock detector to ensure lower spur at reference frequency offset by using the frequency expansion technique. The output frequency is 2.3GHz and reference spur is -43.97dBc @40MHz offset. The design of a wide-locking range divide-by-2 LC-tank RLC ILFD circuit has been presented via simulation and experimental study has wide locking range at both low and high injection powers because of using dual resonance phenomena. The ILFD has dual-band locking ranges and the role of R is used to degrade the quality factor of resonator and to widen the locking range and overlap the two locking ranges [12]-[15]. This approach is highly valuable for reliable RF circuit design particularly at low injection power. Integrated design of phase locked loop and ILFD with VCO for robotics wireless transmitter. The robotics can support natural computation through wireless transmitter for artificial intelligence (AI) application.

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