ADC and PLL for Optical Sensors in Depth and Virtual Reality Augmented Reality Applications

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***Abstract*—In this article a successive approximation register (SAR) analog-to-digital converter (ADC) and phase locked loop (PLL) implemented in tsmc 0.18-um CMOS process is presented for optical sensors in depth camera through virtual reality (VR) and augmented reality (AR) applications. By applying Vcm-based switching method that reduces switching power of the DAC, the proposed SAR ADC with phase locked loop design uses less capacitor in the DAC array. The proposed PLL with a complementary crossed-couple LC-tank voltage- controlled oscillator (VCO) and a mixed design of current mode logic (CML) and true single phase clock (TSPC) logic in the frequency divider.**

I. INTRODUCTION

SAR ADC is a very popular selection for low speed, high resolution applications primarily cause by low consumption and its digital nature [1]-[2]. Many literatures have been done on reducing the switching power such as a split-capacitor technique to make the switching power required to charge up a capacitor from ground to V_{ref} the same for both "down" and "up" transitions of the DAC [3]. The split-capacitor technique provides 37% savings in switching power over a conventional SAR. Literature uses an energy saving technique in combination with capacitor splitting, to achieve 56% savings in switching power [4] and a similar Vcm based switching and achieves 88% savings in switching power [5]. The proposed ADC circuit design adopts Vcm-based monotonic switching procedure. The three reference voltage levels and monotonic capacitor switching scheme result in a low consumption SAR ADC can support VR and AR head mount applications. The fully differential architecture achieves good common-mode noise rejection. The proposed ADC and PLL arrange to support RGB-D functions for optical sensors in 3D camera by depth camera are shown in Fig. 1

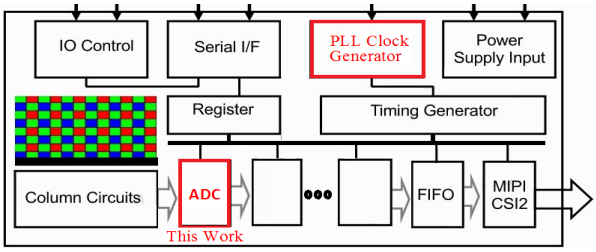

Fig. 1. The proposed optical sensors in 3D camera.

II. ARCHITECTURE OF SAR ADC AND PLL

Fig. 2 shows the proposed SAR ADC architecture. The architecture of PLL mainly consists of a phase/ frequency detector (PFD), a charge pump (CP) [6], a third-order loop filter and a VCO [7] in the feed-forward path and a frequency divider in the feedback path, as shown in Fig. 3. The PFD detects the phase error between the reference signal F_{REF} and the feedback signal F_{DIV}. The digital output signals of PFD control the VCO circuit through the CP circuit and the loop filter. The VCO is proportional to the filter output level and then connected to both frequency divider and output terminal.

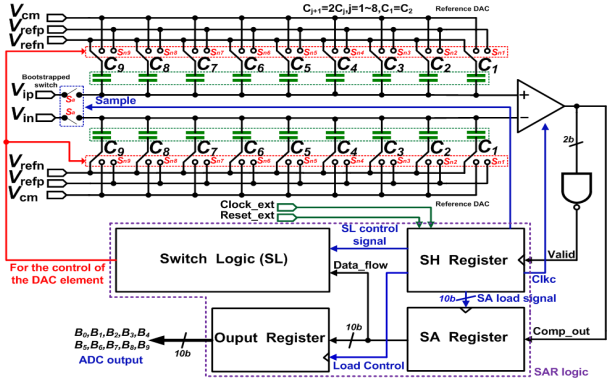

Fig. 2. The proposed SAR ADC architecture.

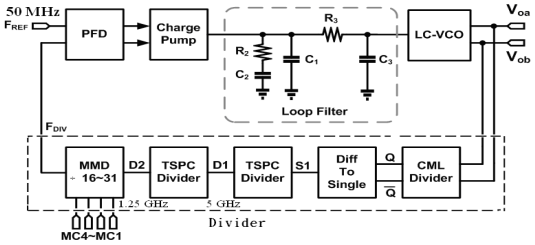

Fig. 3. Architecture of the proposed PLL.

III. MEASURED RESULTS

The SAR ADC and PLL were implemented in a 0.18 µm CMOS process (nominal VDD is 1.8V), and fabricated through the Taiwan Semiconductor Manufacturing Company (TSMC) in a single poly, 6-metal process, including MIM capacitor and Deep N-Well layer options. DNL and INL are influenced by capacitor array layout in DAC significantly and can be limited by routing of the DAC and capacitor mismatch after fabrication. SFDR values versus the sampling frequency and input frequency respectively [8]-[10]. The proposed an integer-N phase-locked loop (PLL) achieves a tuning range of 1460 MHz from target frequency corresponding to 14.6% and a phase noise of -113.47 dBc/Hz at an offset frequency of 1 MHz from the carry frequency. The simulated locking time is lower than 3.0 us and smallest power consumption of 39 mW with third-order low-pass filter. The proposed SAR ADC and

PLL integration for optical sensors in depth camera through natural computation. The optical sensors can support time of flight (ToF) technology to measure depth picture.

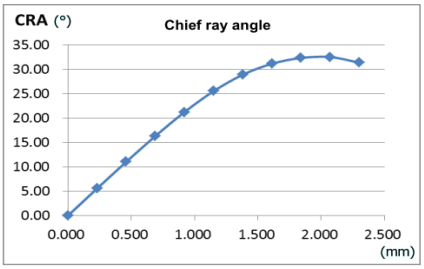

Fig. 4 The measured chief ray angle (CRA) in proposed optical sensors.

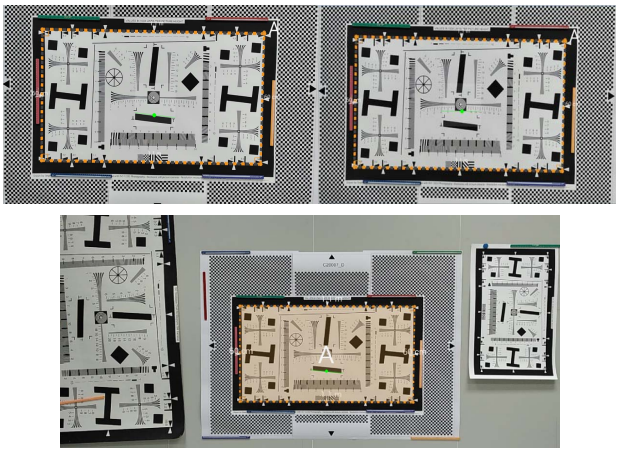

Fig. 5. The measured depth results with ISO12233 test chart by Measure.

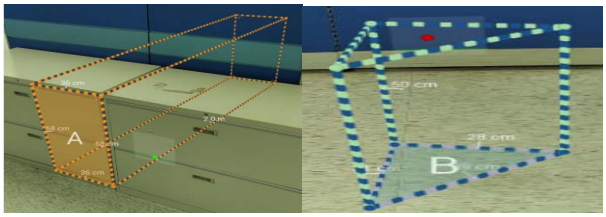

Fig. 6. The Measure illustrates the measured depth results in depth camera.

Fig. 7. The proposed design in depth camera for virtual reality and augmented reality application.

Fig. 4 illustrates the measured chief ray angle (CRA) of analog-to-digital converter and phase locked loop in proposed optical sensors. The measured distance results with ISO12233 testing chart by "Measure App" are shown in Fig. 5. The "Measure App" illustrates the measured depth results of analog-to-digital converter and phase locked loop of depth sensor by time of flight technology in proposed depth camera are shown in Fig. 6. Fig. 7 illustrates the mixed and augmented photo through natural computation by point cloud in depth camera for virtual reality and augmented reality applications.

IV. Conclusions

A SAR ADC and PLL were proposed in depth camera for virtual reality and augmented reality application. The proposed integrated optical sensors structure of the used comparator is a two-stage dynamic comparator. Besides, the asynchronous control logic increases the conversion rate. Using the Vcm-based switching method decrease the capacitor DAC area compares to the conventional SAR ADC. The experiment results demonstrate the performance of the SAR ADC and PLL in optical sensors. The "Measure App" illustrates the measured depth results of analog-to-digital converter and phase locked loop of depth sensor by time of flight technology in proposed RGB-D camera. The analog circuit design integrated algorithm with natural computation by point cloud in depth camera. The mixed and augmented photo through natural computation by point cloud in depth camera for virtual reality and augmented reality applications. The depth camera of optical sensors through natural computation can propose for virtual reality and augmented reality applications.

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