A Well-Arranged FIFO-Storage Distribution Design Plan for Fully Supporting 50 Different FFT Sizes in 3GPP-LTE Communication Applications

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***Abstract*—This paper presents a FIFO-Storage distribution design plan, which is an efficient FIFO arrangement for fully supporting 50 different FFT sizes pre-defined in 3GPP-LTE communication systems. Up to now, it is a first possible solution to deal with 50 various FFT sizes simultaneously. The total FIFO-storage length of our FIFO distribution plan needed is the same as the requirements of a purely single-mode SDF-based FFT design with 8192 points. By utilizing 20 distributed FIFO sub-banks and suitable switch-controlling scheme on each FIFO reading/writing length access, the FIFO-storing can be easily realized without any main FIFO-bit circuit overhead.**

Keywords—FIFO storage, Arrangement, Distribution, FFT, 3GPP-LTE applications.

I. INTRODUCTION

Fast Fourier Transform (FFT) is a popular design tool to transform time-domain signals to frequency domain both in algorithm-researching and architecture-developing worlds. In order to face very different wireless transmitted environments, current 3GPP-LTE standard [1] has defined 50 various FFT sizes and up to 8192 FFT points (N=8192). The challenge is how to make an efficient plan for arranging the data storage of these 50 different FFT-size situations in hardware circuit. Thus, we propose a well-arranged FIFO-Storage distribution design plan. The advantage is that the main FIFO-bit hardware resource needed is the same as the data storage in a purely single-mode SDF-based [2]-[4] FFT design with N=8192.

II. PROPOSED FFT-STORAGE DISTRIBUTION DESIGN PLAN

All FFT points (N) pre-defined in 3GPP-LTE applications are not limited to the power of 2. Instead, it includes the mixed powers of 2, 3, and 5, building up 50 different FFT sizes and a maximum FFT length of N=8192. The combination variety results in the hardware design difficulty, especially for the FIFO data storage. Therefore, we propose a multi-mode FFT system block diagram, as depicted in Fig. 1. It is basically based on single-path delay feedback (SDF) FFT hardware structure and encapsulated to separate into 2 portions.

The first portion indicates the main FFT-computing. There are 3 processing kernel engines (PKEs), such as PKE-1, PKE-2, and PKE-3, executing 2, 8, and 20 configuration types (different radix bases), respectively. PKE-3 circuit is constructed according to radix-5^2 based FFT-operation. By reconfigurable design principles, PKE-3 can operate the configuration types of radix-2^k, radix-3^k, radix-$3x2^k$, radix-$5x3^k$, and radix-3^2x2. Besides, PKE-2 is considered as a reduced form of PKE-3 whereas PKE-1 is treated as a simplified circuit of PKE-2 further. The configuration types supported by 3 PKEs are listed in more details in TABLE I.

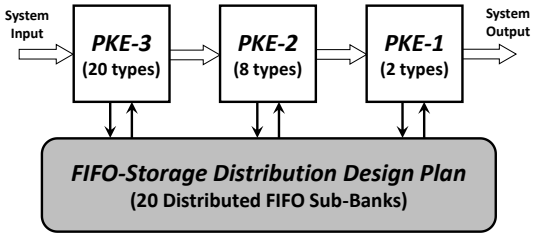

Fig. 1 Proposed multi-mode FFT system block diagram.

TABLE I. TYPES SUPPORTED BY PKE-1, PKE-2, AND PKE-3.

Type Index	Radix-$5^X x3^Y x2^Z$			Types Supported		
	X	Y	Z	PKE-1	PKE-2	PKE-3
$CT1_7$	0	0	7			V
$CT1_6$	0	0	6			V
$CT1_5$	0	0	5			V
$CT1_4$	0	0	4		V	V
$CT1_3$	0	0	3		V	V
$CT1_2$	0	0	2	V	V	V
$CT1_1$	0	0	1	V	V	V
$CT2_3$	0	3	0			V
$CT2_2$	0	2	0		V	V
$CT2_1$	0	1	0		V	V

Type Index	Radix-$5^X x3^Y x2^Z$			Types Supported		
	X	Y	Z	PKE-1	PKE-2	PKE-3
$CT3_5$	0	1	5			V
$CT3_4$	0	1	4			V
$CT3_3$	0	1	3			V
$CT3_2$	0	1	2		V	V
$CT3_1$	0	1	1		V	V
$CT4_2$	2	0	0			V
$CT4_1$	1	0	0			V
$CT5_2$	1	2	0			V
$CT5_1$	1	1	0			V
CT6	0	2	1			V

The second portion is our main design focus/spotlight, which is the data storage with the signals to/from PKEs. In the constructing structure, we divide all of FIFO-storage into 20 distributed FIFO sub-banks [see Fig. 2]. All of FIFO sub-bank sizes are designed as the power of 2. The reasons are not only regular SRAM configuration setting, but also easy controlling. The notation of (L) denotes the specified distributed FIFO sub-bank with a size of L. Different colors indicate different FIFO sizes. F-1 ~ F-3 have sizes of 1 and are always in "turn-on" state for PKE-1. F-4 ~ F-9 are for PKE-2 while F-10 ~ F-20 are for PKE-3. Our proposed FIFO-Storage distribution design plan has a total FIFO length of 8191, which is identical to a single-mode N=8192 SDF-FFT design needed. It represents that we have no main FIFO-bit hardware overhead.

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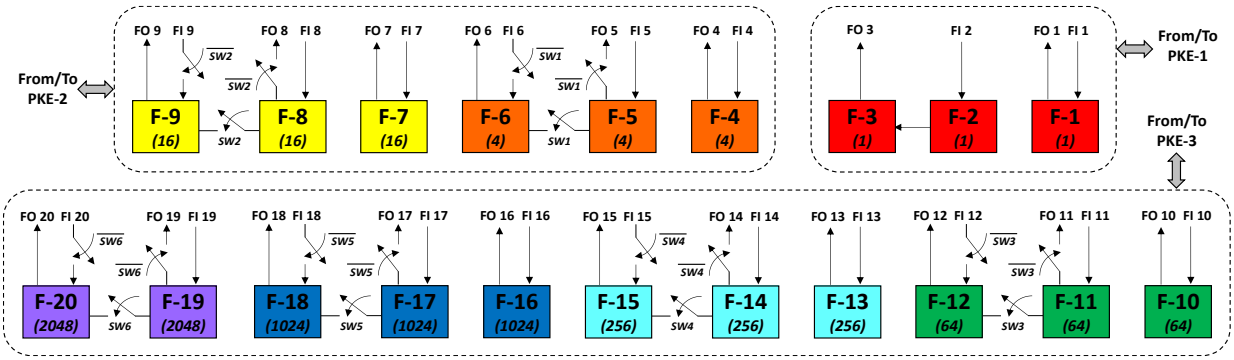

Fig. 2 Hardware design of proposed FIFO-storage distribution design plan.

TABLE II. FIFO READING/WRITING LENGTH ACCESS STATUS OF DISTRIBUTED FIFO SUB-BANKS: F-4 ~ F-9.

Configuration Type of PKE-2			FIFO-Length Access for FIFO Sub-banks					
Notation	k Values	Meaning	F-4	F-5	F-6	F-7	F-8	F-9
$CT1_k$	1 - 4	Radix-2^k	4	4 (k > 1)	4 (k > 1)	16 (k > 2)	16 (k > 3)	16 (k > 3)
$CT2_k$	1 - 2	Radix-3^k	*OFF*	4	4	*OFF*	12 (k = 2)	12 (k = 2)
$CT3_k$	1 - 2	Radix-$3x2^k$	4	4 (k = 2)	4 (k = 2)	*OFF*	2^{k+2}	2^{k+2}

[Note] (condition) : FIFO sub-bank is activated with specified length if meeting the condition.

TABLE III. FIFO READING/WRITING LENGTH ACCESS STATUS OF DISTRIBUTED FIFO SUB-BANKS: F-10 ~ F-20.

Configuration Type of PKE-3			FIFO-Length Access for FIFO Sub-banks										
Notation	k Values	Meaning	F-10	F-11	F-12	F-13	F-14	F-15	F-16	F-17	F-18	F-19	F-20
$CT1_k$	1 - 7	Radix-2^k	64	64 (k > 1)	64 (k > 1)	256 (k > 2)	256 (k > 3)	256 (k > 3)	1024 (k > 4)	1024 (k > 5)	1024 (k > 5)	2048 (k > 6)	2048 (k > 6)
$CT2_k$	1 - 3	Radix-3^k	*OFF*	L_a	L_a	*OFF*	$3*L_a$ (k > 1)	$3*L_a$ (k > 1)	*OFF*	*OFF*	*OFF*	$9*L_a$ (k > 2)	$9*L_a$ (k > 2)
$CT3_k$	1 - 5	Radix-$3x2^k$	64	64 (k > 1)	64 (k > 1)	256 (k > 2)	256 (k > 3)	256 (k > 3)	1024 (k > 4)	*OFF*	*OFF*	2^{k+6}	2^{k+6}
$CT4_k$	1 - 2	Radix-5^k	*OFF*	L_b	L_b	*OFF*	L_b	L_b	*OFF*	$5*L_b$ (k = 2)	$5*L_b$ (k = 2)	$5*L_b$ (k = 2)	$5*L_b$ (k = 2)
$CT5_k$	1 - 2	Radix-$5x3^k$	*OFF*	L_a	L_a	*OFF*	$3*L_a$ (k = 2)	$3*L_a$ (k = 2)	*OFF*	3^k*L_a	3^k*L_a	3^k*L_a	3^k*L_a
CT6	none	Radix-3^2x2	64	*OFF*	*OFF*	*OFF*	128	128	*OFF*	*OFF*	*OFF*	384	384

[Note] Parameter List : L_a = {24, 32, 36, 48, 64}, L_b = {12, 24, 36, 48}

In addition, the design specialty is that we add six extra controllable switches (SW1 ~ SW6) among certain distributed FIFO sub-banks to fulfill overall data-storing tasks needed. Take SW1 for design examples. While SW1=1, F-5 and F-6 are connected together, forming a larger data-storing space. The according input and output ends are FI 5 and FO 6, respectively. On the contrary, F-5 and F-6 independently operate while setting SW1=0. The other controllable switches also have analogous circuit behaviors. Most important of all, we can flexibly adjust FIFO reading/writing length access of each FIFO sub-banks for the requirements of each PKE circuit. TABLE II illustrates that each of F-4 ~ F-9 is set as "ON" or "OFF" according to the actual configuration types of PKE-2. Also, it determines the corresponding length access for correct processing. Besides, TABLE III shows the status of F-10 ~ F-20, highly depending on the practical configuration-type setting of PKE-3. Consequently, we can successfully achieve the data-storage missions for all of 50 FFT-size situations.

III. Conclusion

For dealing with 50 different FFT sizes pre-defined in 3GPP-LTE communication systems, we propose an efficient arrangement of FIFO-storage distribution design plan.

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