Performance Improvement of 18-bit ΣΔ A/D Convertor

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***Abstract* – The research paper presents a simulation study to develop and improve the overall performance of sigma delta (ΣΔ) A/D modulator, the circuit structure and technique used were explained and the processes of different parameters of ΣΔ modulator over the conventional modulator were explained clearly. Simulated results of the proposed ΣΔ system shows a good improvement in the spurious noise produced by the conventional A/D converter.**

Index Terms – ΣΔ A/D converter, signal to noise ratio sampling.

INTRODUCTION

The advancement of technology made the modulators important component of any electronic system, generally the signal is analog in many applications such as telecommunications, video and computer system that depend on digital or binary signal in it is operation, where it became necessary to convert the analog signal to a digital signal to take advantage of the power, flexibility and reliability of digital signal processing. The converters are complex because of consisting of many of the components of analog, such as Op-amps, sample and holds and comparative, therefore these modulators are very difficult to design, especially when they are implemented practically [1]. The performance of the circuits in the digital signal processing and communication systems generally is determined by the digital signal that's obtained from the analog data .[2]. The A/D modulator is forming a digital word representing the corresponding amount of the analog voltage or current given any value consisting of a number of bits (bits). The most important characteristics of the ADC converter is the resolution and the speed of the A/D converter, which is usually measured in samples per second (samples per second) [3].

The A/D converter is divided into two parts depending on the ratio of the sampling.

There are two types:

a) The first category is the (Nyquist rate ADCs) In which the input signal is modelled at a frequency twice the input signal frequency or more. Figure 1 shows the (Nyquist rate ADCs).

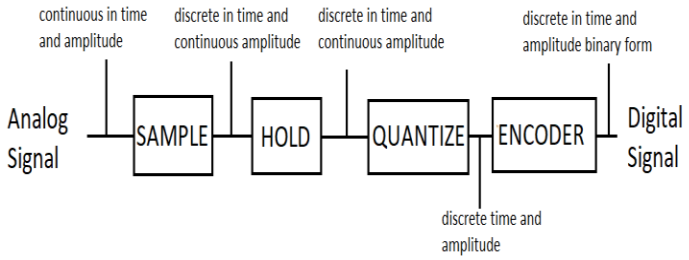

Fig 1: Nyquist rate ADCs.

b) The second category (oversampling ADCs) in which the data entry samples are taken at a frequency much more the value of input signal. Figure 2 Shows the (oversampling ADCs) [1].

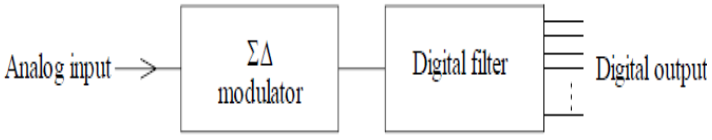

Fig 2: Oversampling ADCs.

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OVERSAMPLING IN ADC

Usually the oversampling modulator is called ΣΔ converter which is composed of two main blocks. The first one is called the ΣΔ modulator and the second block which is called digital filter as shown in Figure 3. Sigma delta modulators are different from the conventional analog to digital modulators that the input signal is sampled at a frequency greater than the input signal frequency. One of the most important benefits of ΣΔ modulators is to get rid of the fade inhibitor (anti-alias filters) And no need to harmonize the elements used, high accuracy and compatibility with digital technology VLSI, and noise shaping feature (Noise Shaping) and Oversampling noise.

Below are brief definitions of terms of Sigma delta modulators:

Noise Shaping (Integrator): The noise shaping filter (integrator) of a sigma delta modulator spreads the low quantization error (noise) in the concern bands.

Oversampling: It's the operation which sample input signal like speech signal in frequency twice or more than the input signal .

Digital filter: The digital filter is used to minimize signals and noise that are outside the concern band .

Decimal point: Decimator is decreasing the data rate down from the oversampling rate without losing data.

The (OSR) Over sampling ratio is a feature that reduce the quantization noise when the desired signal is collected and also increases (SNR).

Sigma delta modulators are capable of high accuracy of the conversion, so it's used in converting the continuous and alternate signals. Figure 3 shows the internal structure of the sigma delta ADC [4].

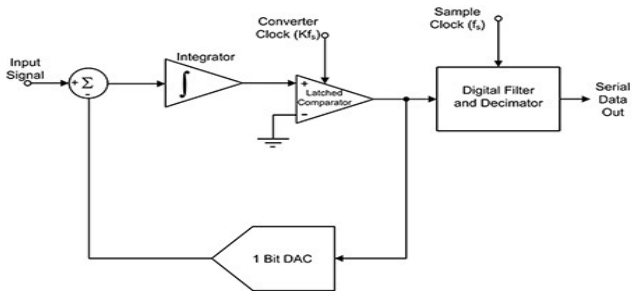

Fig3. Block diagram of A/D system ΣΔ.

SIGMA DELTA MODULATOR OPERATION PRINCIPLE

A) 1st Sigma-Delta Modulation

The sigma delta 1storder is composed of (One difference operator), (One discrete integrator) and (one-bit quantizer) as shown in Figure 4 [5],[6].

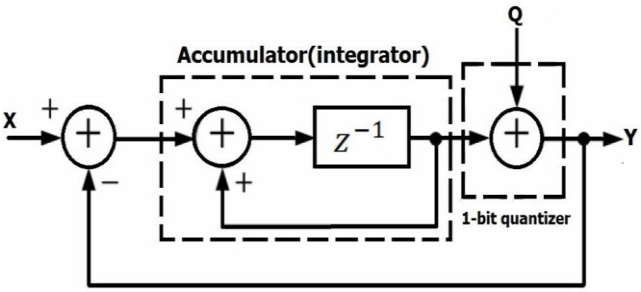

Fig 4. Block diagram of 1st ΣΔ modulator.

The ΣΔ modulator principle of working depends on noise shaping and the oversampling features. Therefore, the (OSR) Over sampling is a feature that reduce the quantization noise when the desired signal is collected and also increases (SNR). The input signal (X) is sampled at (Fs) frequency which it's more than twice of the input signal frequency. The (oversampling) known as the ratio between the sampling frequency (Fs) to twice the frequency of the input signal, as in the following equation [7][6]:

$$OSR = \frac{F_S}{2.F_B} \quad (1)$$

The over sampling has the advantage to reduce of minimize the quantization noise produced by the conventional A/D converter. The ΣΔ modulator tends to shift this noise out of the band of interest that is toward the high frequency band using suitable digital filter to be eliminated by the digital filter.

$$Y(z)= X(z).z^{-1}+ (1-z^{-1}) Q(z) \quad (2)$$

Therefore, Q(z) represents quantization noise. From the above equation we conclude that the input signal (X) remains fixed without change while shifts quantization noise to higher frequencies because of the presence of the $(1-z^{-1})$. The equations below show how the noise shaping process occurred as in [8]. The Noise Transfer Function Included in Figure (4) is as follows:

$$\frac{Y(z)}{Q(z)} = 1- z^{-1} \quad (3)$$

By deriving equation (3) it results he quantization noise power of the 1st order modulator is as follows:

$$S_y(f) = 2\,|1 - \cos(2\,\pi\,f\,T_{ck})\,| \quad (4)$$

$$S_y(f) = 2\,|1 - \cos(\frac{2\,\pi\,f}{F_s})\,| \quad (5)$$

$F_s = \frac{1}{T_{ck}}$ (Sampling frequency of the modulator)

Figure 5 illustrate the spectrum of the Noise Shaping, hence its noted from the figure, the Noise Shaping starts From the of zero at f = 0 And reach up to the value 4 At half the sampling frequency (f = $\frac{F_s}{2}$). By increases the sampling frequency, noise shaping function expanded horizontally, so the noise concentration will decrease at low frequencies [9].

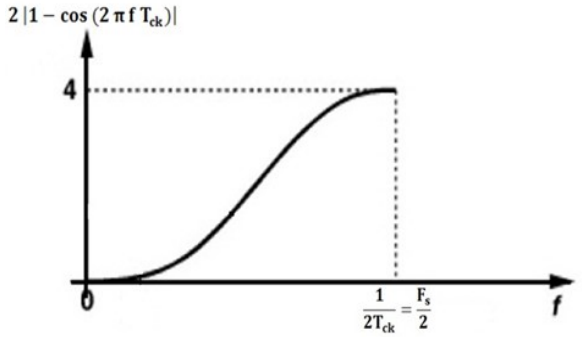

Fig. 5. Noise Shaping in the sigma-delta first order.

S/N ratio depends on the OSR according to the following equation [7]:

SNR= 6.02R + 1.76-5.17+30 log (OSR) (6)

R represents the number of bits in the modulator. As it's clear from the above equation we conclude that by doubling the OSR, the SNR will be improved by 9dB.

B) Sigma Delta Second Order Modulator

2nd order sigma delta modulator block diagram is illustrated in Fig. 6. Adding more integrators and summers components in sigma delta modulator can cause higher order quantization noise. As to sigma delta theory, increasing the modulator order causes decreasing the effect from the quantization noise, the nonlinearity distortion and the digital accuracy. But increasing the modulator order will causes complexity and difficulty in the circuit design and the implementation. To achieve the balance between the high accuracy and simple the circuit structure, second order sigma delta is used to solve this problem [8].

It's clear from, the 2nd order compared with a 1st order sigma delta, more noise power is shift away from the signal band.

An additional integrator is added to the structure. The first integrator transfer function is $1/(1-z^{-1})$.

The SNR modulator in the ideal filtering giving by:

$$\sigma_{ey}^2 = \sigma_e^2 \frac{\pi^2}{3} \left(\frac{2f_B}{f_s}\right)^3 \quad (7)$$

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10log\left(\frac{\pi^4}{5}\right) + 50log\left(\frac{f_s}{2f_B}\right) \quad (8)$$

The oversampling ratio, $Fs/2Fb = 2^r$, the SNR improved by 15 dB for each increment of r.

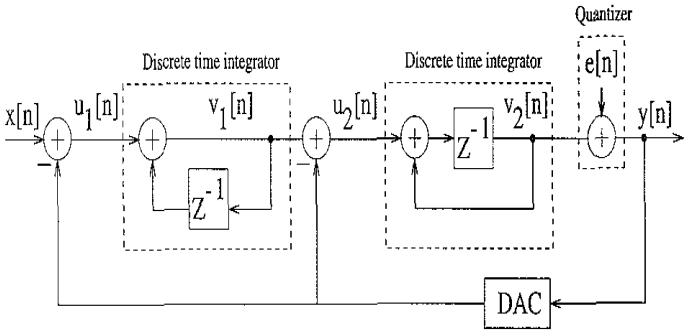

Fig. 6. Block diagram of 2nd ΣΔ modulator.

OTHER TYPES OF HIGHER ORDER ΣΔ MODULATOR

The 2nd order sigma delta of noise reduction with low OSR may not be sufficient to obtain large accuracy. By Adding an extra integrator inside the loop can enhance the noise shaping order [10]. However, higher order in sigma delta modulators cannot guaranteed stability. It is very hard to develop a comparator model and use a linear feedback to guarantee the stability of the high-level Sigma-delta converter system because of the nonlinear characteristics of the comparator. Consequently, most designs rely on multiple cascaded 1st and 2nd order sigma delta converters as a comparative method to achieve high order noise shaping. This structure is called a MASH [11] or cascading ΣΔ ADC system.

SYSTEM DESIGN AND RESULTS

Figure 7 shows the proposed ΣΔ modulator and a digital filter and all the system where simulated using MATLAB software.

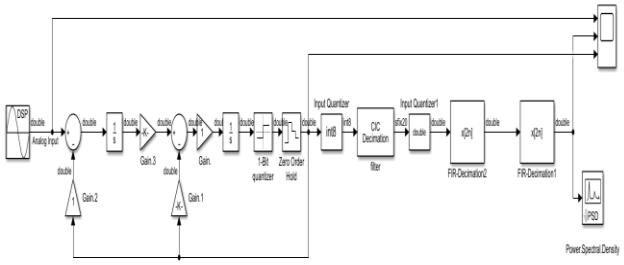

Fig7. The Sigma Delta A/D model.

Figure 7 shows the second order sigma delta modulator model which it consists of two difference operator, two integrators, 1-bit quantizer, and a negative feedback. Table 1 shows the characteristics of the Sigma Delta A/D.

18-bit sigma delta A/D for a signal equal to 40 KHz is simulated using MATLAB software.

TABLE 1
SIGMA DELTA MODULATOR CHARACTERISTICS

ADC Parameters	Values
B.W	40KHz
Fs	20.48 MHz
OSR	256
Modulator order (M)	2
Modulator bits No. (B_{mod})	1
Filter output bits No. (B)	18

At signal bandwidth (Pass Band Frequency) of 40 KHz the modulator could achieve a SNR of 71.3 dB. The modulator operating with sampling frequency (F_s) of 20.48 MHz and the down sampling ratio (DSR) of 256 & Stop Band Frequency (F_{stop}) of 42 KHz The output of the sigma delta modulator sample rate should be decreased to the Nyquist rate in order to remove the high quantization noise at high frequencies and to achieve high resolution the decimation filter must have the specific parameters as shown in Table 2.

TABLE 2
THE CHARACTERISTICS OF DECIMATION FILTER.

Parameters	Values
F_s	20.48 MHz
DSR	256
F_{pass}	40 KHz
F_{stop}	42 KHz

The digital input signal which composed of 18-bit is produced by the decimation filter. It is so difficult to build an ideal filter that give the specification in Table 2, but using multi stage filter or a complicated digital circuit can simplify the construction of this circuit.

Figure (8) shows the results of a 2nd order ΣΔ modulator at f_s =20.48 MHz and with 20 KHz sinewave at the input.

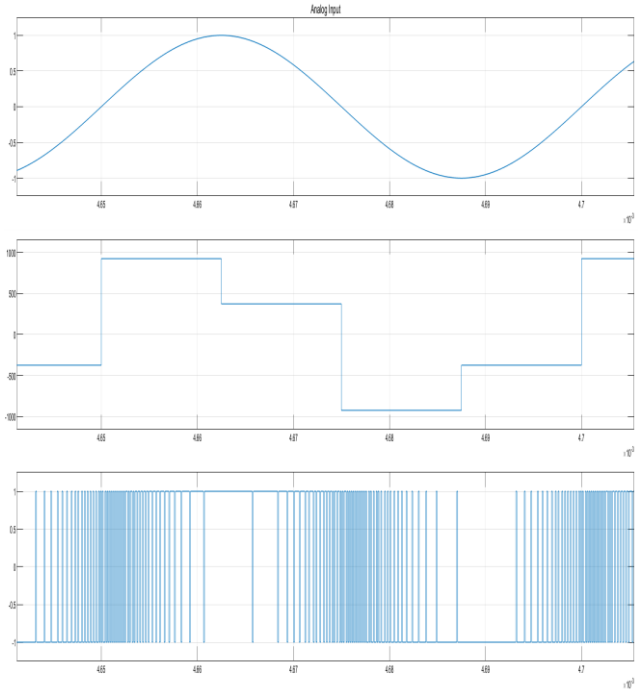

Fig 8. Second order modulator transient response for a sine-wave input of 20 KHz.

It is clear that the output signal is a square wave or a modulated pulse and it is a function of the input sinewave signal of +ones and -ones are increased in the positive and negative peak when a sine wave input respectively. When the input signal at zero amplitude, there are equal number of +ones and -ones, which is the expected response of a ΣΔ Modulator.

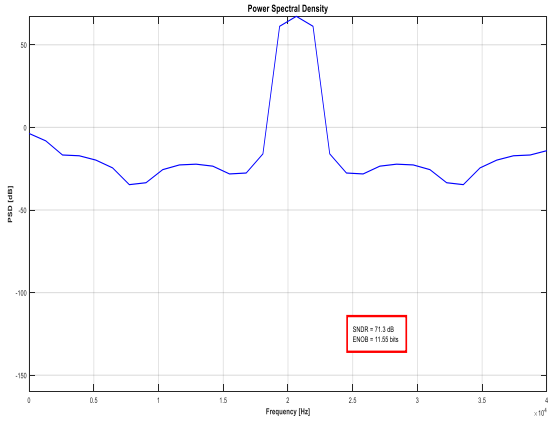

Fig 9. The frequency response of the 3rd order power output (CIC) filter with OSR is 64.

As shown in Figure 9 the quantization noise moved into the high frequency region. The second order ΣΔ modulator

output with OSR of 256 is designed to achieve SNR and ENOB to be 71.3dB and 11.55 bits.

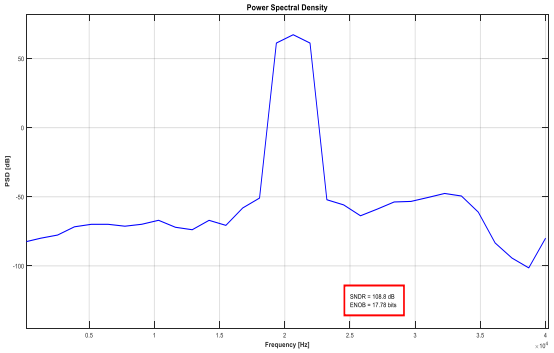

Fig 10. Frequency response of the power spectrum in the output of the2nd order ΣΔ converter with the expected 18-bit accuracy.

The decimation filter output spectral shown Figure 10, it is obvious that the decimation filter is capable to eliminate high and low frequency is not in the operation band frequency which means clearly enhancing the SNR of the system. Finally, the Sigma Delta ADC is capable to achieve a resolution of 17.78 bits and SNR of 108.8 dB.

As summary, the ΣΔ ADC improve the performance of the system using a 18 bit resolution, the sampling frequency which is used in the simulation is 20 MHz and the BW is about 40 KHz. The main step in the research is to find the optimum order loop that the filter contains and to find the over sampling ratio. Figure shows the relation between S/N and OSR values.

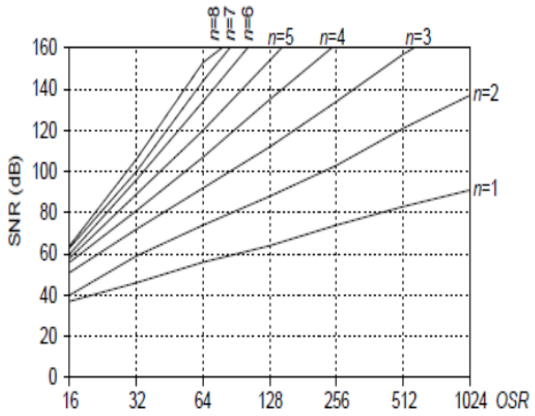

Figure 11: Relation between S/N and OSR.

In our paper the OSR = (fs/2xBW) = 250 and 18 bit matches to 108 dB dynamic range. The graph shows the relation between the oversampling ratio and the SNR, so that by increasing the order and/or OSR the resolution enhanced clearly. Therefore, SNR will have increased.

The methods to improve SNR:-

- Increases modulator order.
- Increasing the oversampling ratio.
- Increasing quantizer bits.

The modulators with higher order are unstable. This problem can be solved by using multi-stage-noise-shaping (MASH) modulator.

CONCLUSION

Simulation the sigma delta, A/D in this research illustrates that the different applications require sigma delta ADC with various specifications. various specifications can improve the overall system performance of any A/D converter through reducing the spurious noise produced by the conventional A/D converter. The ΣΔ modulator is designed with 18 bit filter output and with f_s =20 KHz for input signal equal, bandwidth equal to 40 KHz. The Sigma Delta single-loop is more appropriate for low-resolution voice and communications applications. Sensor applications and portable devices are required to obtain high accuracy and low power sigma delta ADCs .

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