Insertion Sort Circuit Design Applied on the Median Filter

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***Abstract*--In our paper, we proposed the insertion sort circuit of the median filter for the corrupted image. The median filter can be overcome the salt-pepper noise in the figure. We indicate the middle pixel value in a mask window of the figure to overcome the salt-pepper noise occurred. The method concept is easy and efficient. We use the Altera DE2-115 development board to verify our insertion sort circuits. We put the noise image in the SDRAM on the board, and filtered the image by the proposed circuits. In the result, we display the picture on the screen to show the processed image.**

I. INTRODUCTION

In the image processing, the median filter can smooth the image and keep the edge for detection. The median filter also can overcome the impulse noise in the image [1, 2]. The sort algorithm uses to implement the median filter. The image usually has several million pixels. The software process consumes the CPU times. The median filter can be implemented by the hardware circuits. The common hardware implemented circuits of the sort are the odd-even transposition sorting and odd-even merge sort [3-5]. In those implementations, they can use the parallel implementation to increase the efficiency. However, the data number is even in those methods with more compact. The middle value in a number list, the number must be odd. Thus, we proposed the implementation of the insertion sort. We adapt the basic sort cell circuit [6] to modulize the sort algorithm circuits.

II. BASIC CELL OF SORT CIRCUITS

In the design of sort circuits, we often need some cell circuits to compare two numbers. The basic sort cell shown in Figure 1 is adopted. It is a combinational logic circuit. We get two input values of A and B in the basic cell, the outputs are increasing or decreasing orders. For reducing time to finish the comparison, the parallel circuits is used. The number of the sorting cells is important to decide the whole chip area for several sort methodology circuits [4, 5].

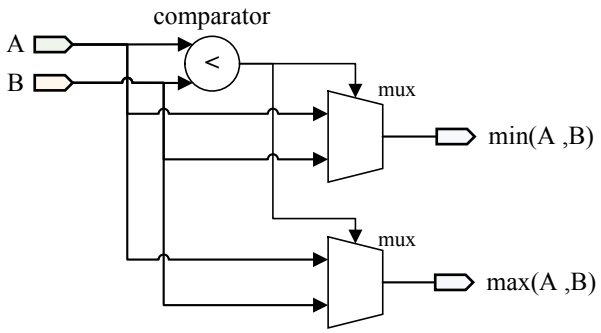
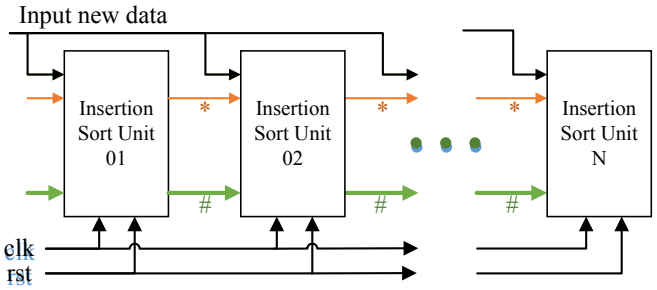


Figure 1 Basic Sort Cell Circuit

III. MEDIAN FILTER DESIGN

In image recognition, the edge detection is often used to simplify the image complexity and get the characteristic for recognition. The impulse noise in the image will become as edges to influence the recognition. The median filter filters the noise on the image, however it does not cause the wrong detection of the object edge. The operation of the median filter is taken the middle value of the given size window mask. Every pixel on the corrupted image is replaced by the middle value of the square mask window. The size window is square with odd number, e.g., 3x3 or 5x5. The total number of pixels in the window is odd then it can find the middle value. It is a nonlinear filter. In the sort algorithms, the insertion sort is faster than other methods. Since there are many pixels in an image to process, we adopt the insertion sort methodology. In Figure 2, we proposed our insertion sort implementation circuit. In the design, we can extend the compare number by instancing the insertion sort units. And the compare number is fine for odd or even. We modulize the basic unit on the insertion sort. Every basic insertion sort unit is shown in Figure 3.



*: Unit status

#: Data

Figure 2 Proposed Insertion Sort Implementation

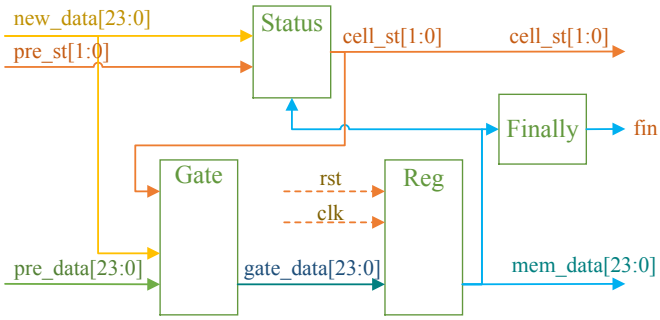


Figure 3 Insertion Sort Unit Circuit

IV. Experiments

In our design for the median filter, we implement the circuit on the Altera DE2-115 development board with Cyclone IV EP4CE115. We put the noise image in the memory. Using the architecture of the FPGA to verify the median filter. The block diagram is shown in Figure 4. The SRAM is used to store the original noise image and processed image. We have standby, display, and filtering modes in the circuit status. The VGA can show the original image and processed image, respectively. In Figure 5, we show the operation flow and the some results.

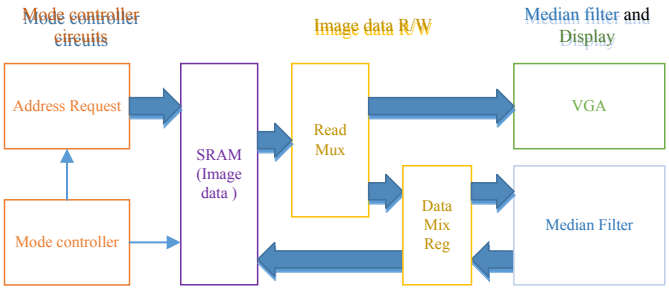


Figure 4 Block Diagram of the Insertion Sort Implementation

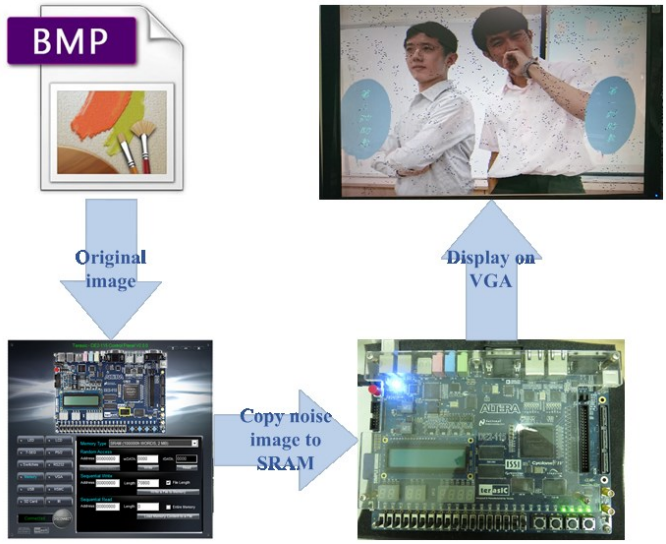


Figure 5 Flows of the Verification

V. Conclusions

We proposed the insertion sort circuit of the median filter for the corrupted image. The median filter can be overcome the salt-pepper noise and the insertion sort is faster than other methods. The insertion sort circuit is modulized by the basic unit. We can extend easily to any sorting number.

References

[1] H. Hwang and R. A. Haddad, "Adaptive median filters: new algorithms and results," *IEEE Transactions on Image Processing,* 4 (4), pp.499–502, 1995.

[2] M. Ahmad and Duraisamy Sundararajan, "A fast two-dimensional median filtering algorithm," *IEEE Transactions on Circuits and Systems,* 34(11), pp. 1364-1374, 1987.

[3] Kemal Oflazer, "Design and implementation of a single-chip 1-d median filter," *IEEE transactions on acoustics, speech, and signal processing,* 31(5), pp.1164–1168, 1983.

[4] C. Y. Lu and C. M. Wu, "A Hardware Design Approach of Sorting for FlexRay-based Clock Synchronization," *IEEE/SICE International Symposium on System Integration,* pp.1400-1405, 2011.

[5] U. A. Korat, P. Yadav, and H. Shah, "An Efficient Hardware Implementation of Vector-based Odd-even Merge Sorting," *Ubiquitous Computing, Electronics and Mobile Communication Conference (UEMCON), IEEE 8th Annual,* pp. 654-657, 2017.

[6] R. Marcelino, H. C. Neto, and J. M. Cardoso, "A Comparison of Three Representative Hardware Sorting Unit," *In Industrial Electronics, IECON'09. 35th Annual Conference of IEEE*, pp. 2805-2810, 2009.