A Fault-Tolerant Routing Method for 2D-Mesh Network-on-Chips Based on the Passage of Fault Blocks

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***Abstract*—Toward the realization of dependable high-end consumer electronics products, this paper proposes a fault-tolerant routing method for 2D mesh Network-on-Chips (NoCs). Unlike the conventional fault-tolerant routing methods which always detour faulty nodes, the proposed method is based on a new concept; packets can pass through faulty nodes. For the method, we enhance the common NoC architecture and add switches and links around the each node. Simulation result shows that the proposed method reduces average communication latency by about 75.9%, compared with the conventional method.**

I. INTRODUCTION

Network-on-Chip (NoC) is a promising paradigm for the design of large scale embedded systems in high-end consumer electronics products. In NoCs, a number of circuit modules (i.e. nodes) in a VLSI chip are connected by an on-chip interconnection network through routers and nodes communicate one another by transmitting packets on the network. However, if nodes are faulty, packets are not sent to destination nodes correctly. In VLSI technology, failure occurrence can not be avoided. Therefore, to cope with the defects and faults in the system fabrication and run time, fault-tolerant packet routing is essential to realize dependable NoCs.

One of the suitable methods for NoCs Region-based fault-tolerant routing [1] - [3]. In this method, rectangular fault regions are generated with detour paths, so that packets can proceed toward their destinations avoiding faulty nodes. However, as the number of faulty nodes increases, detour paths become long and thus, communication latency is increased.

In this paper, to overcome this problem, we propose a new fault–tolerant routing method which allows packets to pass through faulty nodes. Unlike the conventional fault-tolerant routing methods which *always detour* faulty nodes, this method is based on a new concept; packets can *pass through* faulty nodes.

II. A FAULT TOLERANT ROUTING FOR 2DM NOCS

Target NoC topology is popular 2D mesh (2DM) which has *n* and *m* homogeneous nodes in row and column direction, respectively. Fig. 1 shows the general architecture of the 2DM-NoC. A node consists of a processor core and a router. Routers are connected at most four neighbor nodes (i.e. north, south, east, and west) via two unidirectional links to configure a regular mesh topology. Each router forwards packets to one of the neighbours to transmit them to the destination nodes.

In the region-based fault-tolerant routing methods, rectangular Fault Blocks (FBs) is generated to avoid faulty nodes, and detour paths are defined along the FBs. Detour

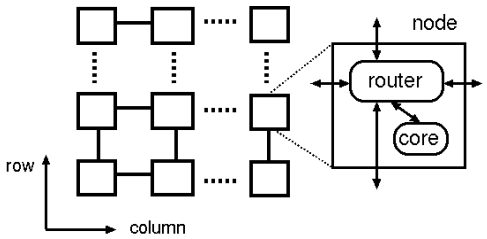

Fig. 1 Architecture of 2DM-NoC

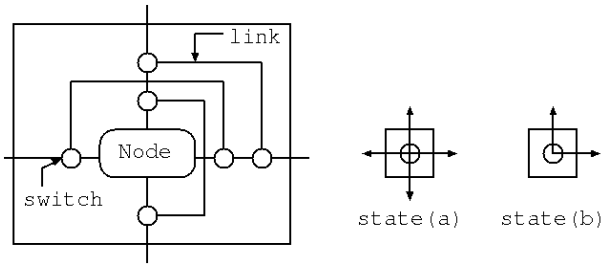

Fig. 2 Proposed architecture

paths are classified into three types according to the locations; Fault Ring (FR, inside the network), Fault Chain (FC, on the west side of the network), South Chain (SC, on the south side of the network). Routes of packets are determined by the rules defined for each detour path. In case there exist many faulty nodes, detour paths become long and communication latency is increased, which is the practical disadvantage for NoCs.

III. PROPOSED FAULT THROUGH NOC ARCHITECTURE

To overcome the above problem, we propose a fault-tolerant routing method based on a new concept; packets can passes through faulty nodes. Fig. 2 shows the architecture for the proposed method, where links and switches is added at the around each node. The possible states for passing through the faulty node are also shown in Fig. 2. The state (a) allows packets to pass through in west-east and north-south directions at the same time, and state (b) allows in west-north direction.

Fig. 3 shows the proposed fault-tolerant routing method. Basically, the proposed method is based on the conventional routing method [3]. In Fig. 3, C and D represent the current and destination nodes, respectively, and reference node means the east-north node of each detour path. The bold rules in Fig. 3 expressly allow packets to pass through the faulty nodes. Note that, packets may pass through the faulty nodes by the result of other rules. Example case of each rule is shown in Fig. 4. This method guarantees the deadlock-freeness because the states (a) and (b) does not cause any turns prohibited in [3].

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Passage-Fault_Region (C, D)

If (C is D)
   consume the packet
elsif (D is to west of C)
   if (C is on a SC and west neighbor is faulty)
      Next_Route = West  /* (Fig. 4 (a)) */
   elsif (C is on a FR, west neighbor is faulty
         and C and D are not on the same row)
      Next_Route = South
   elsif (C is on a FR and
         C and D are on the same row)
      Next_Route = West  /* (Fig. 4 (b)) */
   else
      Next_Route = West
   endif
elsif (D is to north of C)
   if (C is on a FR, north neighbor is faulty and
      C and D are on the same column)
     Next_Route = North /* (Fig. 4 (c)) */
   elsif (C is on a FR, north neighbor is faulty and
         D is southeast than the reference node)
      Next_Route = East
   else
      Next_Route = North
   endif
elsif (D is to South of C)
   if (C is on a FR, south neighbor is faulty and
      C and D are on the same column)
     Next_Route = South /* (Fig. 4 (d)) */
   elsif (C is on a FC south neighbor is faulty)
     Next_Route = South /* (Fig. 4 (e)) */
   elsif (C is on a FR and C is
         at a west end of FR of C)
      Next_Route = West
   else
      Next_Route = South
   endif
else /* D is to east of C */
   if (east neighbor is faulty)
     Next_Route = East /* (Fig. 4 (f)) */
   else
      Next_Route = East
   endif
endif
```

Fig. 3 Routing rule of proposed method

The proof of the deadlock-freeness is omitted here due to limitations of space.

IV. Performance Evaluation

To evaluate the performance of the proposed method, we conducted computer simulations. In the simulations, faults are generated randomly and FBs are formed. For each fault distribution, packets are generated randomly at each node. One packet is divided to five flits. Simulation parameters are listed in Table I. Packets pass through each router in three cycles if

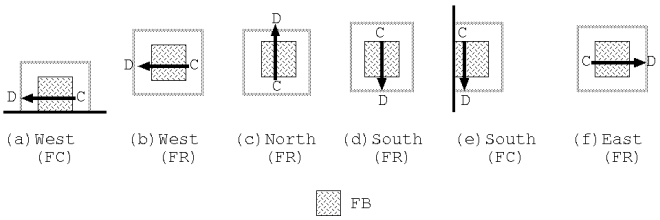

Fig. 4 Example case of pass through

TABLE I
Simulation Parameters

Network size	10 × 10
Input buffer depth	4 flits
Fault rate	10 %
Total simulation length	50,000 cycles

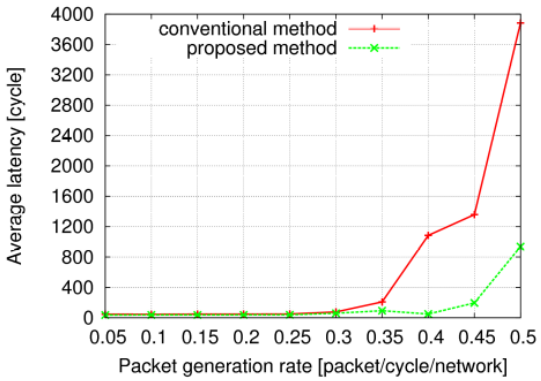

Fig. 5 Average latency

there is no contention; packet moves to the adjacent router at the third cycle. Each trial is repeated 100 times changing fault distribution to measure the average latency which is defined for each packet as the total cycles required to reach the destination node from the source node.

Fig. 5 shows the average latency. When packet generation rate is relatively low, the average latency of both methods is almost the same. On the other hand, when it is high, the proposed method outperforms the conventional method. The proposed method reduces average latency by about 75.9% at the packet generation rate of 0.5. This result is because of the shorter detour paths provided by passing through faulty nodes.

V. Conclusion

In this paper, we propose a new fault-tolerant routing method which allows packets to pass through faulty nodes. Future work includes the circuit design of the proposed method and the estimation of the hardware overhead.

Reference

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