Performance Analysis of Alternative Adder Cell Structures Using Clocked and Non-clocked Logic Styles

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PART-I

Motivation

- Fast data processing – Processor's ALU Adder Speed.
- Main instructions performed while processing is ADDITION.
- Many adders' architectures have been researched, analyzed and proposed for speed improvement and power reduction.
- Never ending demand for high processing capabilities.
- Scope to propose novel approaches for high performance and energy efficient implementations.
- All these depends on the type of "logic style".

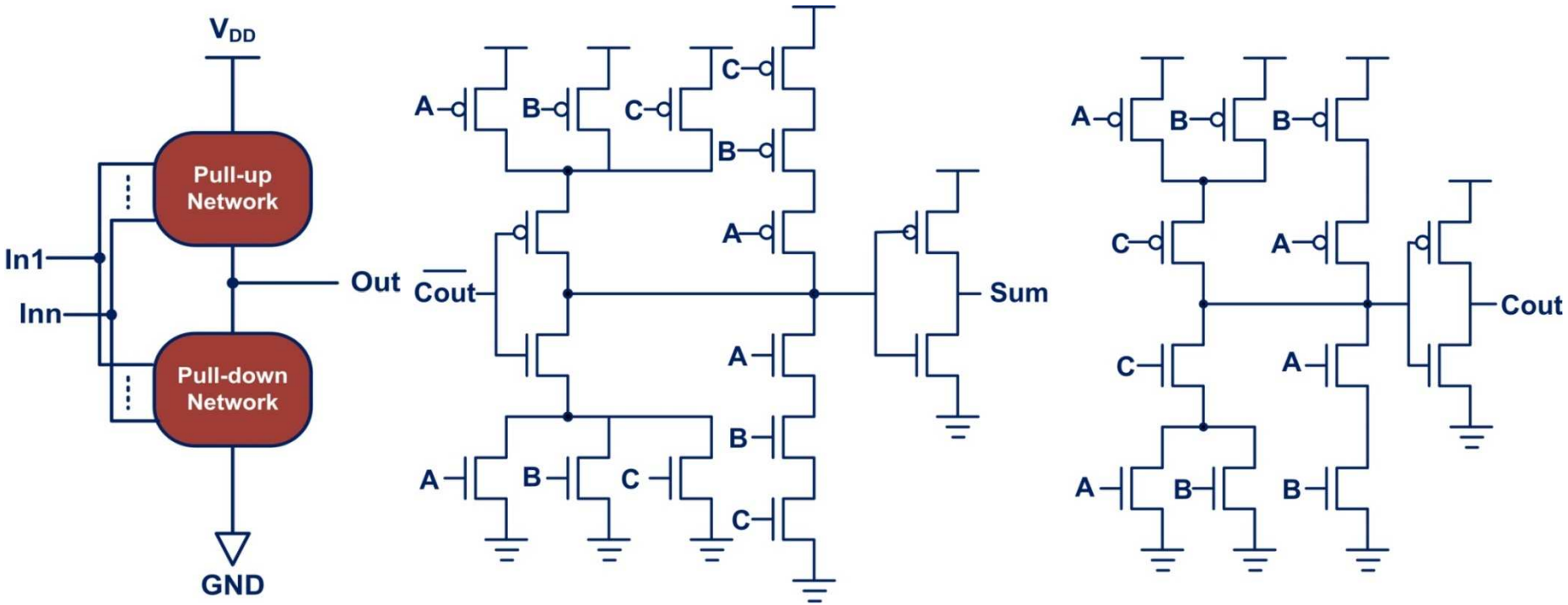
Literature Review

- Adders with various logic styles are proposed in the literature and their performance is compared using different technologies.
- Logic styles are classified into two classes:
  - Non-Clocked Logic Styles
    - Static CMOS, CPL, SR-CPL, DPL etc.
  - Clocked Logic Styles
    - Dynamic, FTL, CD etc.
- The above logic styles are implemented using Cadence Virtuoso with 180nm and 45nm technology nodes and simulated using Spectre Simulator.
- Propose the modified SR-CPL, Modified DPL with the changes in the carry generator logic.

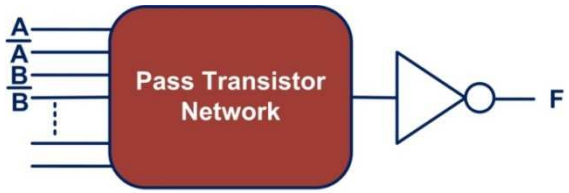
Literature Review Contd…

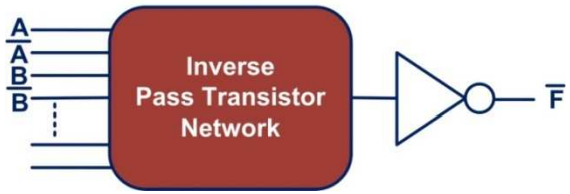
- **Non-Clocked Logic Styles:**
  - Static CMOS – 28T, Low Power, High Noise Tolerance, Lower Speed, High Fan-out Load.
  - CPL – 30T, Low Power, High Speed, Poor Fan-in, Reduced Noise Immunity
  - DPL – 28T, High Speed, No Level Restoration, Limited Logic Depth and Load Capability
  - SR-CPL - 26T, Low Power, More Logic Depth, Poor Performance, Limited Output Drive.
- **Clocked Logic Styles:**
  - Dynamic – 22T, High Speed, Fast Evaluation Time, Low Area, High Power.
  - FTL – 20T, High Speed, Long Logic Depth, Fast Evaluation, High Power, Reduced Noise Immunity.
  - CD – 36T, High Speed, Better Energy Efficient, Reduced Noise Immunity, Little Complex.

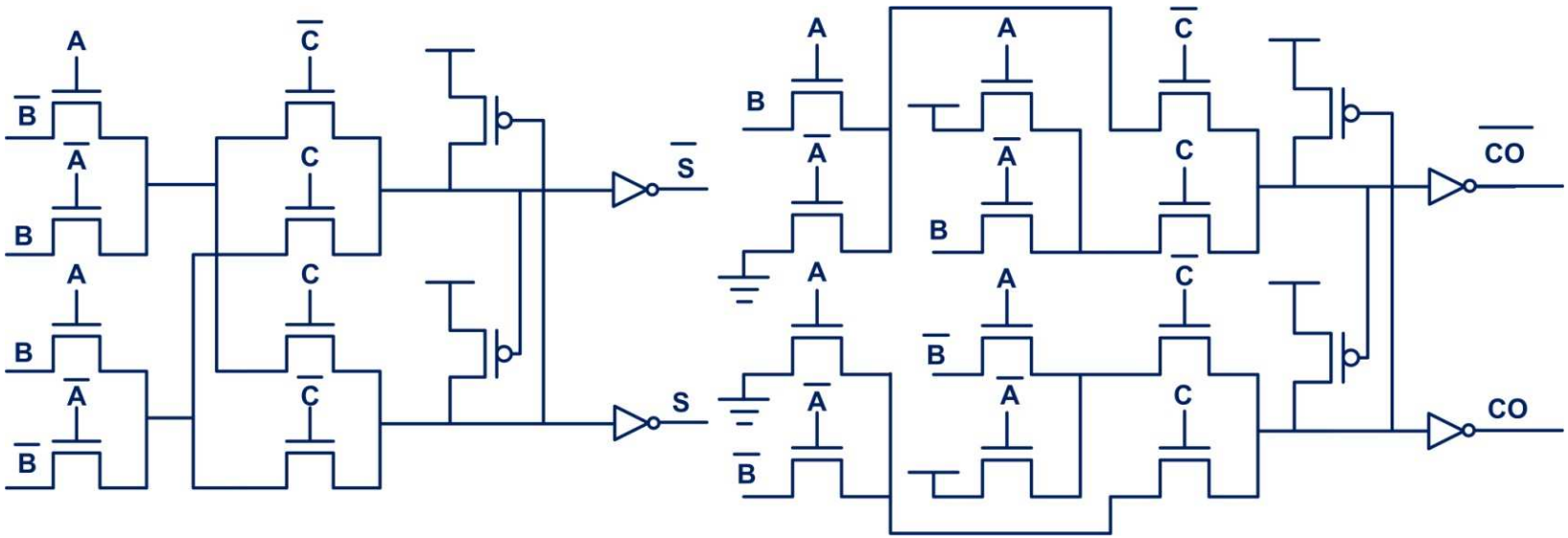
1. Static Logic



2. Pass Transistor Logic / Complementary Pass Transistor Logic



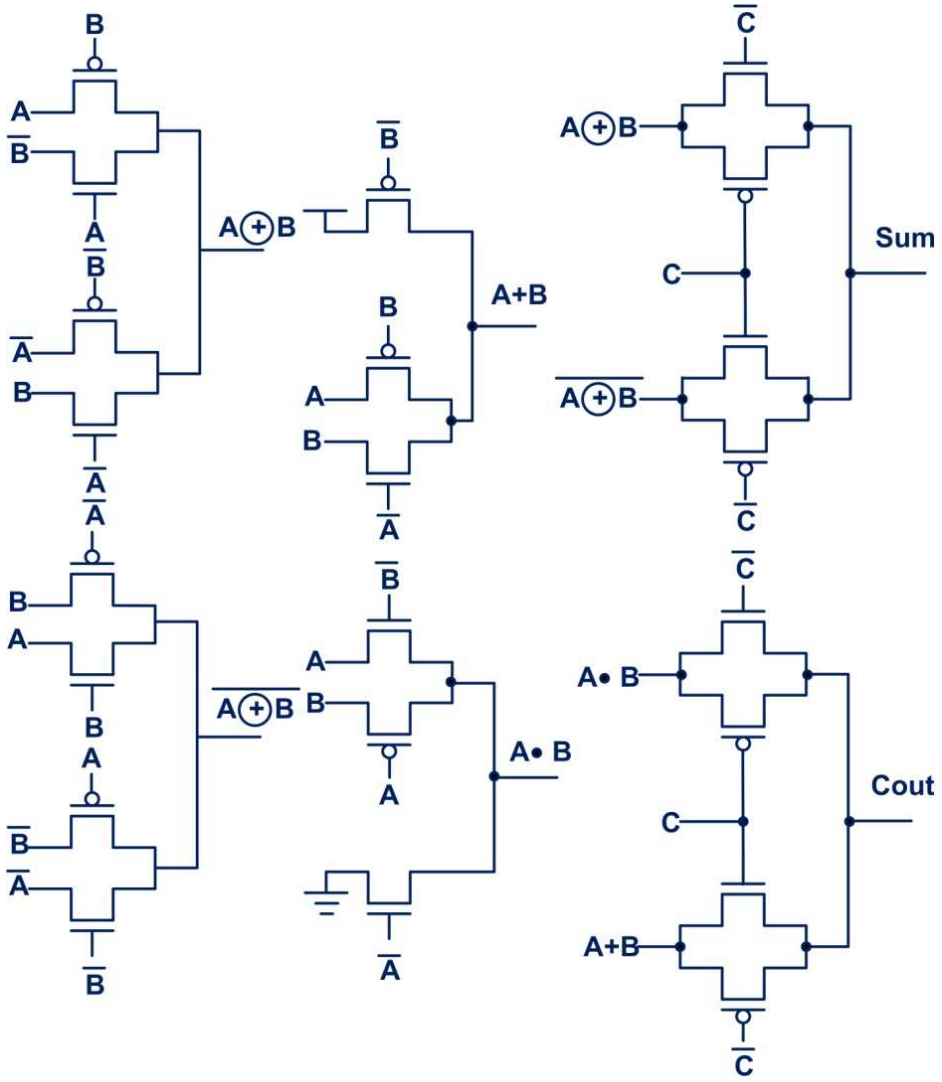




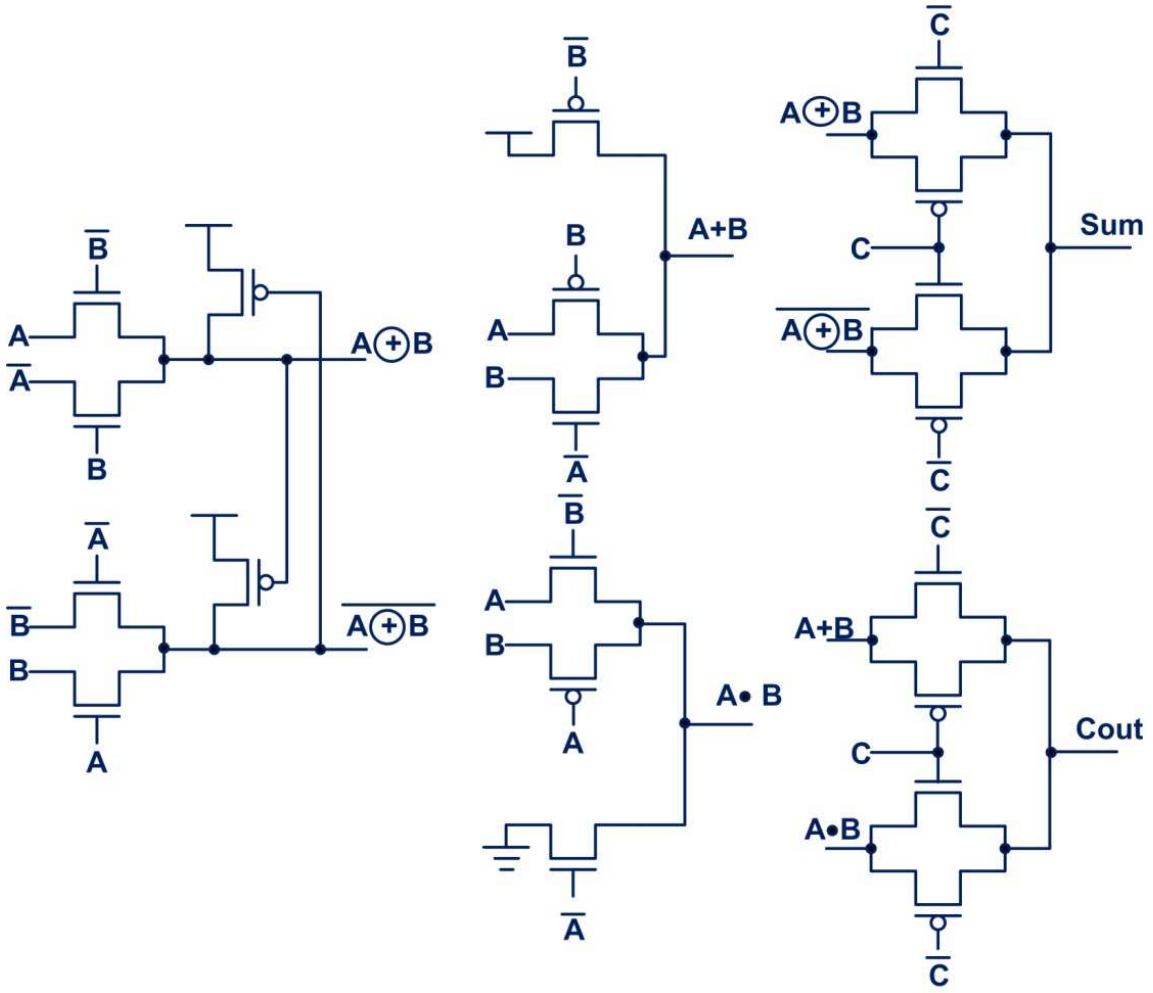
3. Double Pass Transistor Logic (DPL)

$$SUM = (A \oplus B)\overline{C} + (A \odot B)C$$

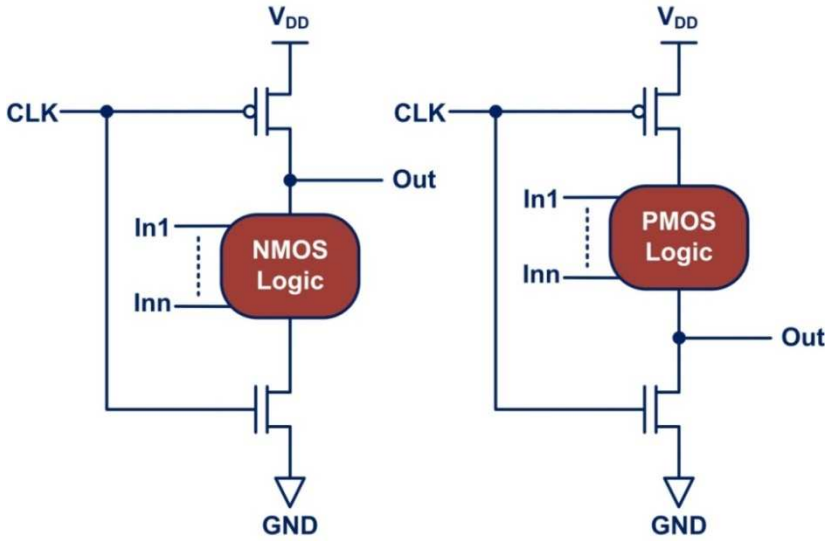
$$CARRY = (A \cdot B)\overline{C} + (A + B)C$$

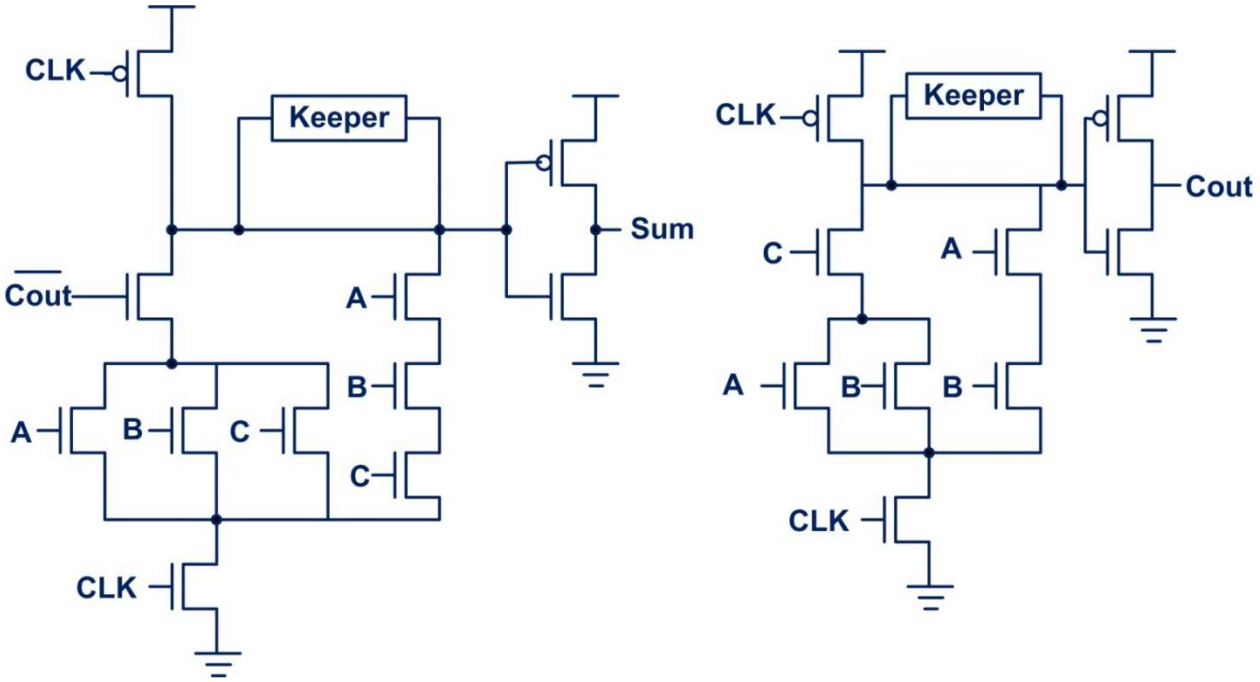


4. Swing Restored CPL (SR-CPL)

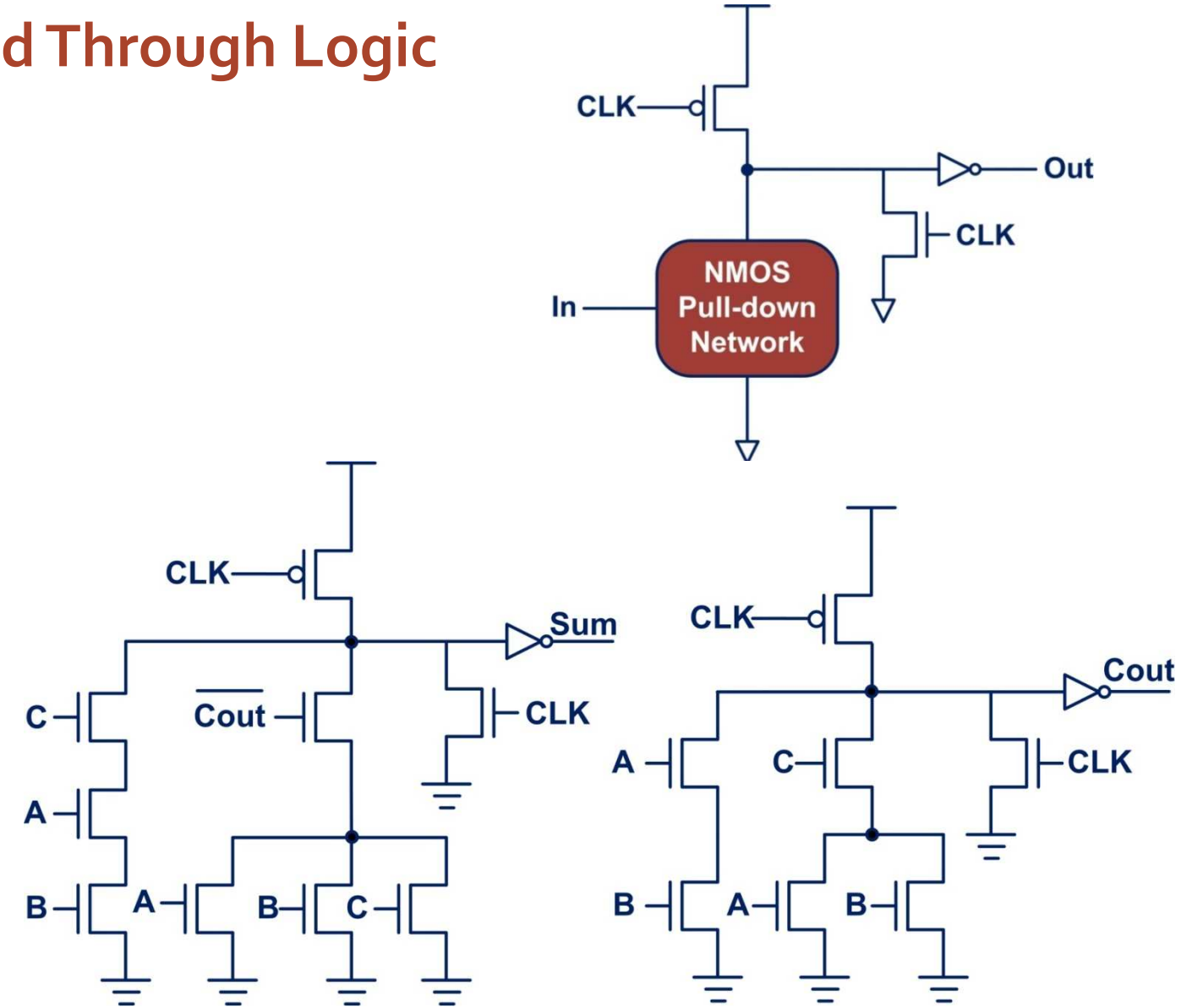


5. Dynamic Logic

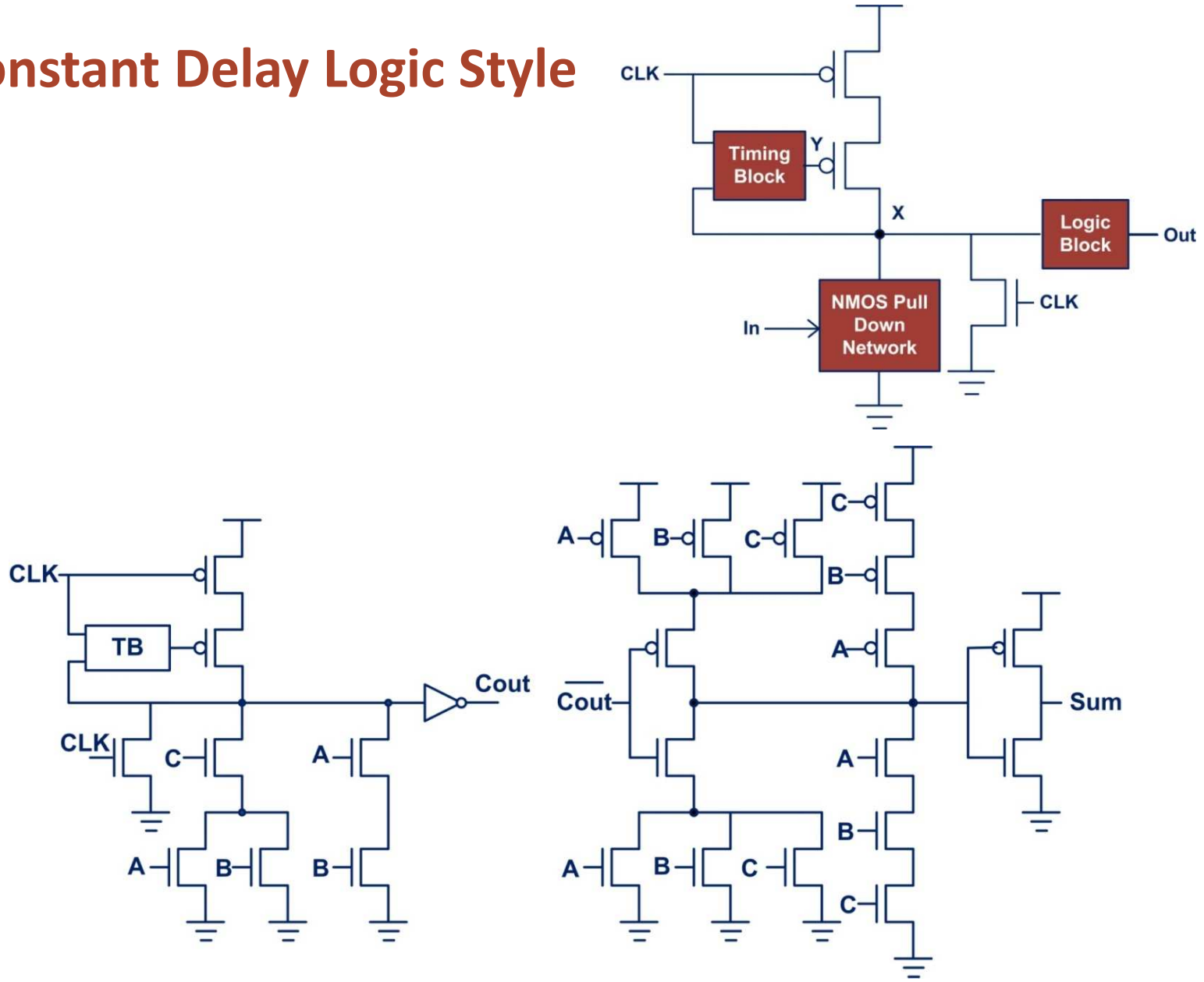




6. Feed Through Logic



7. Constant Delay Logic Style



Comparisons of Existing Adders

Logic Style	Power (uW)	Delay (pS)	PDP (uW*nS)
Static	243.2	198.4	48.25
CPL	424.9	126.3	53.66
DPL	352.2	45.1	15.88
SR-CPL	325.7	57.9	18.85
Dynamic	398.1	177.1	70.50
FTL	402.8	134.6	54.21
CD	418.1	109.5	45.78

Table 1: Performance Metrics Comparison of Various Adder Cells using Cadence Virtuoso with 180nm Technology node

Objectives

- To propose a novel logic style which is power efficient and high performance.
- Design a 1-bit full adder using new logic style.
- Compare power, delay and power-delay product for the proposed design with various technology nodes (180nm and 45nm).
- To perform parametric analysis for supply voltage variation and temperature variations.

PART-II

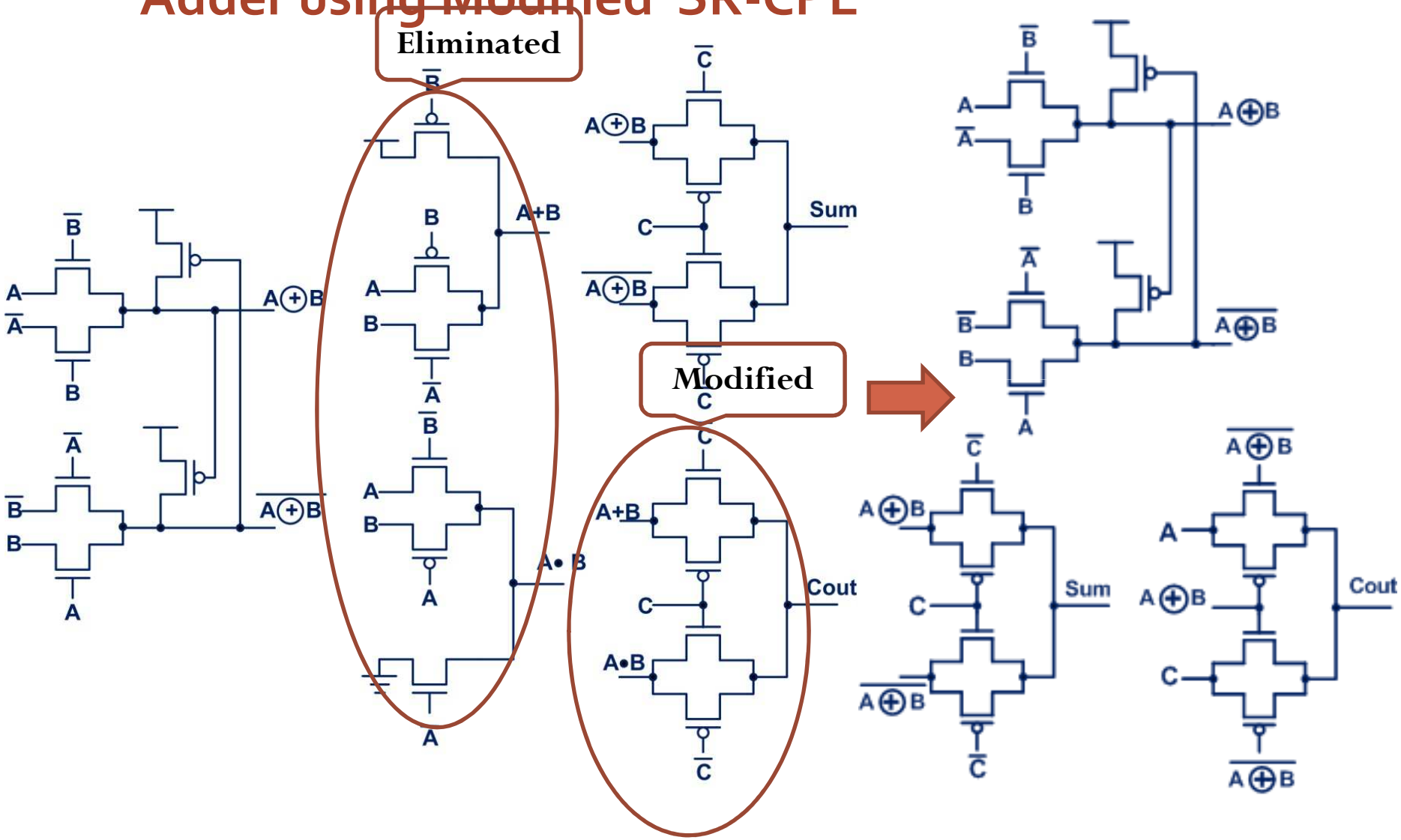
Proposed Modified SR-CPL

- The Carry Equation can be rewritten as

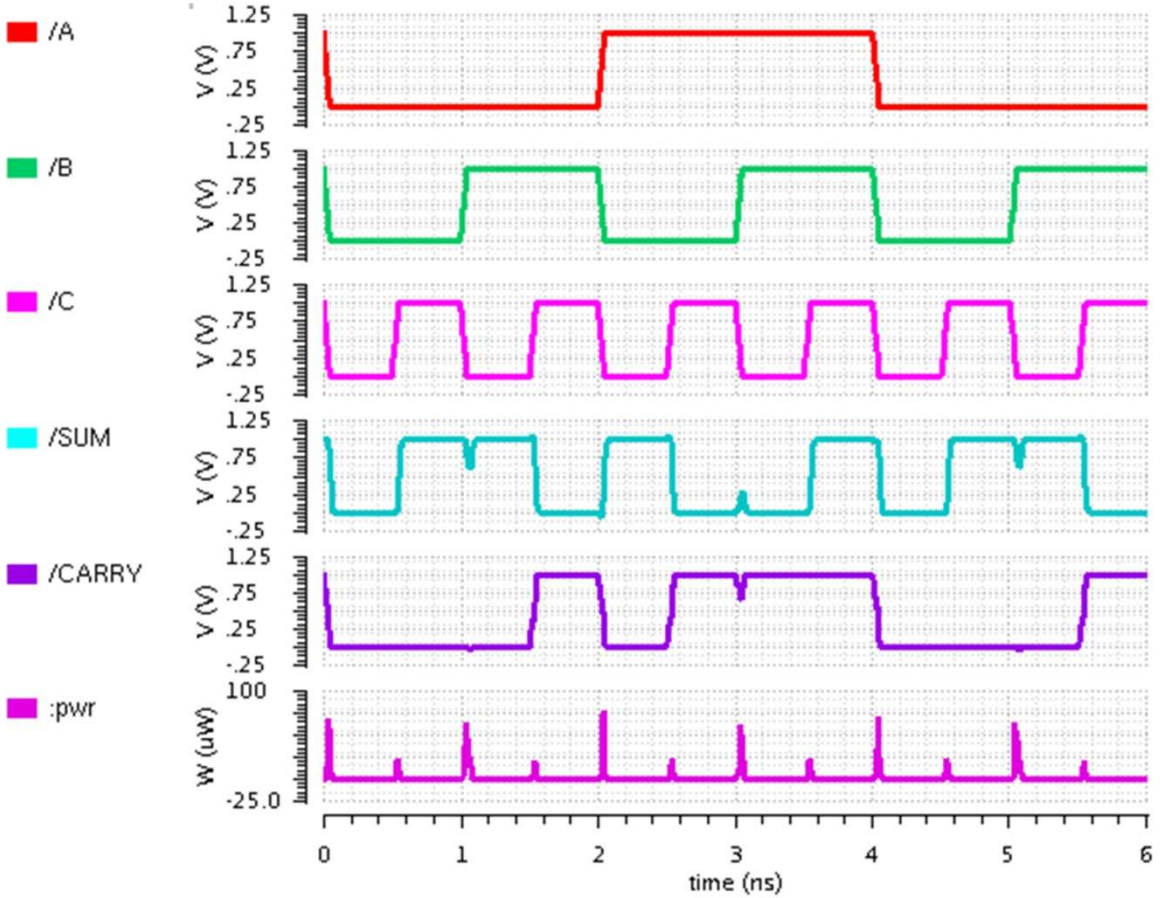
$$CARRY = (A \odot B)A + (A \oplus B)C$$

- The Sum is same as in Conventional SR-CPL.
- The Transistor Count is reduced in the Carry Generator.
- Hence power, delay reduced in the modified logic style when compared with the SR-CPL.

Adder using Modified SR-CPL



Simulation Waveforms of Modified SR-CPL Full Adder



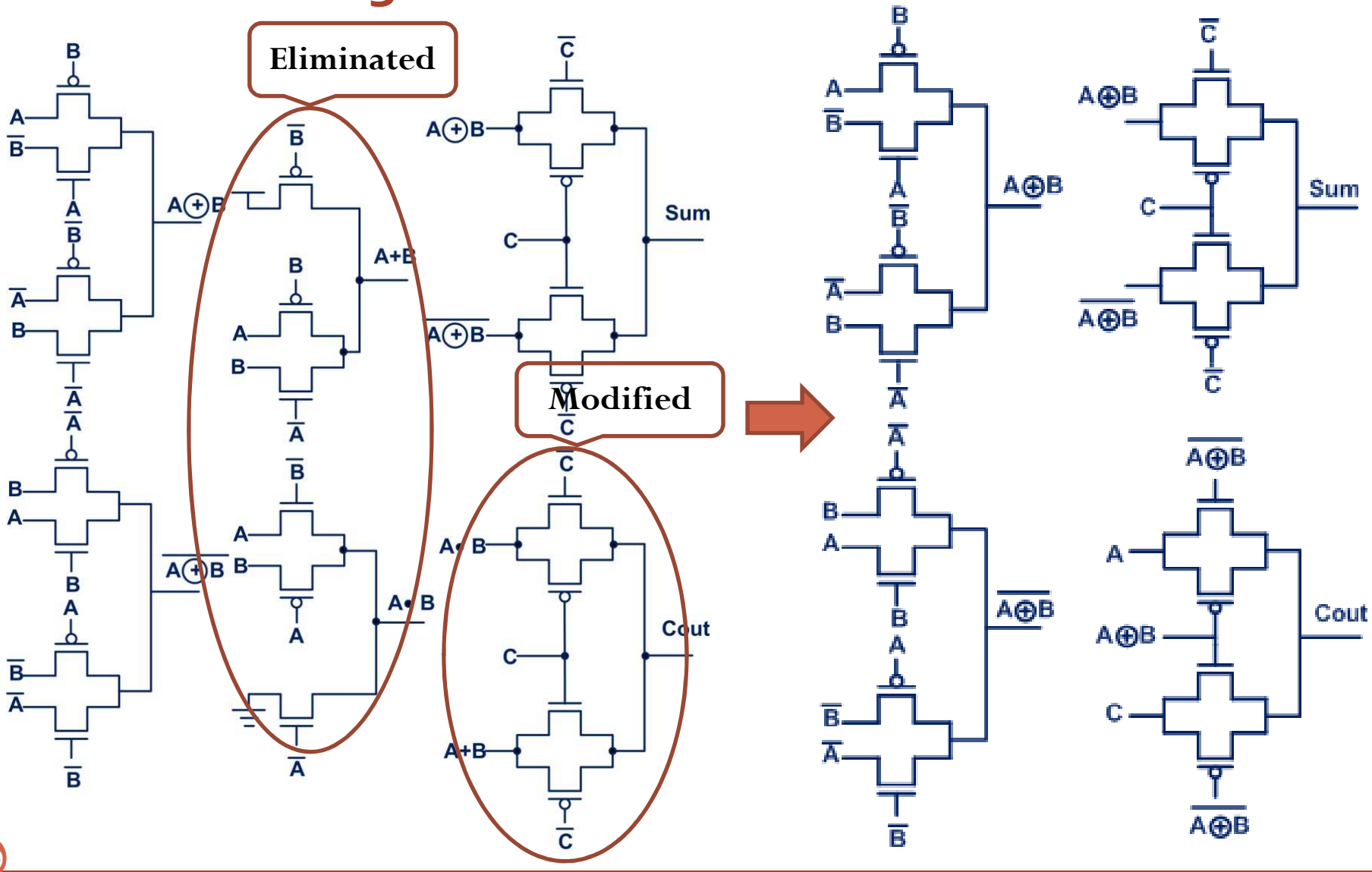
Proposed Modified DPL

- The Carry Equation can be rewritten as

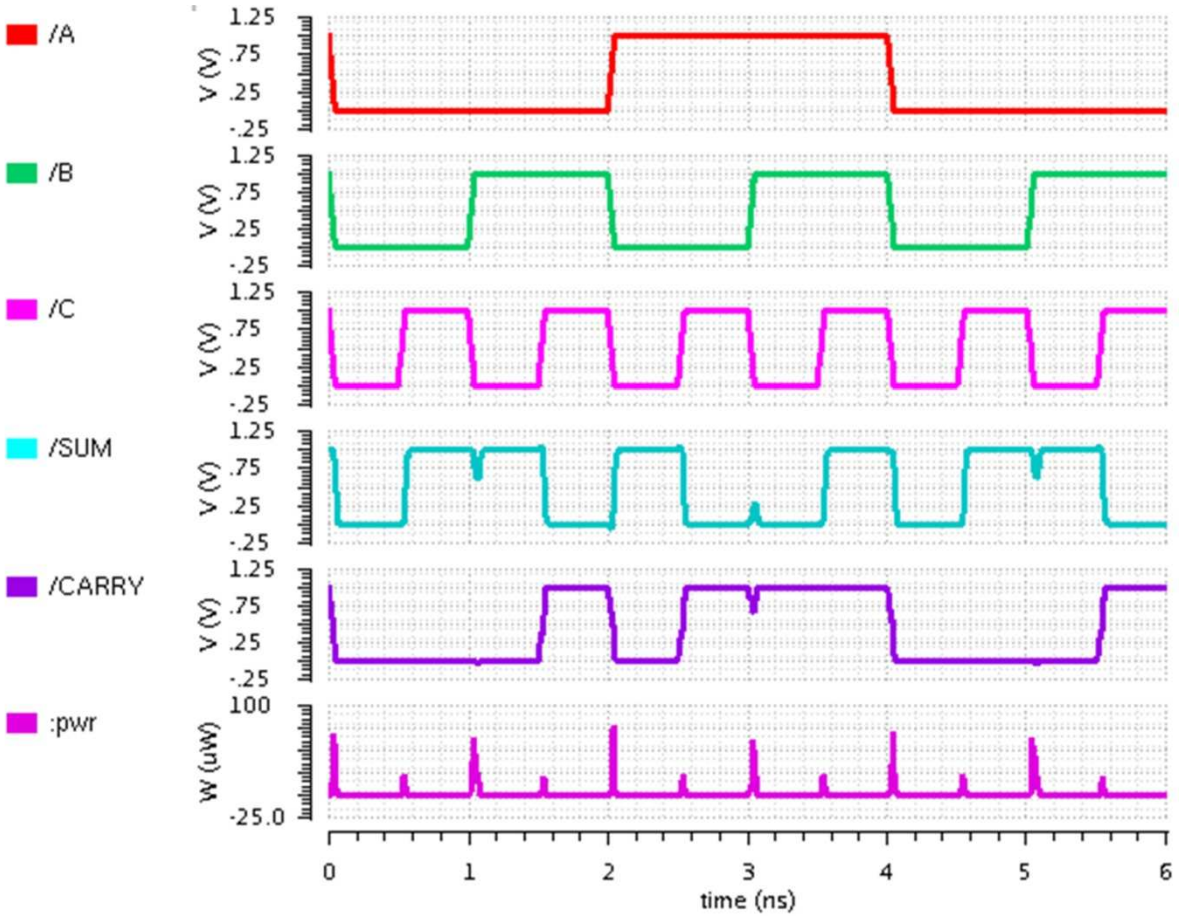
$$CARRY = (A \odot B)A + (A \oplus B)C$$

- The Sum is same as in Conventional DPL.
- The Transistor Count is reduced in the Carry Generator.
- Hence power and delay reduced in the modified logic style when compared with the DPL.

Adder using Modified DPL



Simulation Waveforms of Modified DPL Full Adder



Comparison of Proposed Adders (180nm)

Logic Style	Transistor Count	Power (uW)	Delay (pS)	PDP (uW*nS)
Static CMOS	28	243.2	198	48.15
CPL	30	524.9	126	66.13
DPL	28	352.2	45	15.84
SR-CPL	26	325.7	47	15.30
Modified DPL	22	315.5	45	14.19
Modified SR-CPL	20	245.7	47	11.54

Table 2: Performance Metrics Comparison of Various Adder Cells using Cadence Virtuoso with 180nm Technology node

Comparison of Proposed Adders (45nm)

Logic Style	Transistor Count	Power (uW)	Delay (pS)	PDP (uW*pS)
Static CMOS	28	1.75	68.25	119.787
CPL	30	4.10	62.01	246.36
DPL	28	2.48	28.15	69.812
SR-CPL	26	2.29	29.92	68.516
Modified DPL	22	2.17	27.09	58.785
Modified SR-CPL	20	1.76	28.08	49.42

Table 3: Performance Metrics Comparison of Various Adder Cells using Cadence Virtuoso with 45nm Technology node

Power Consumption Comparison (45nm)

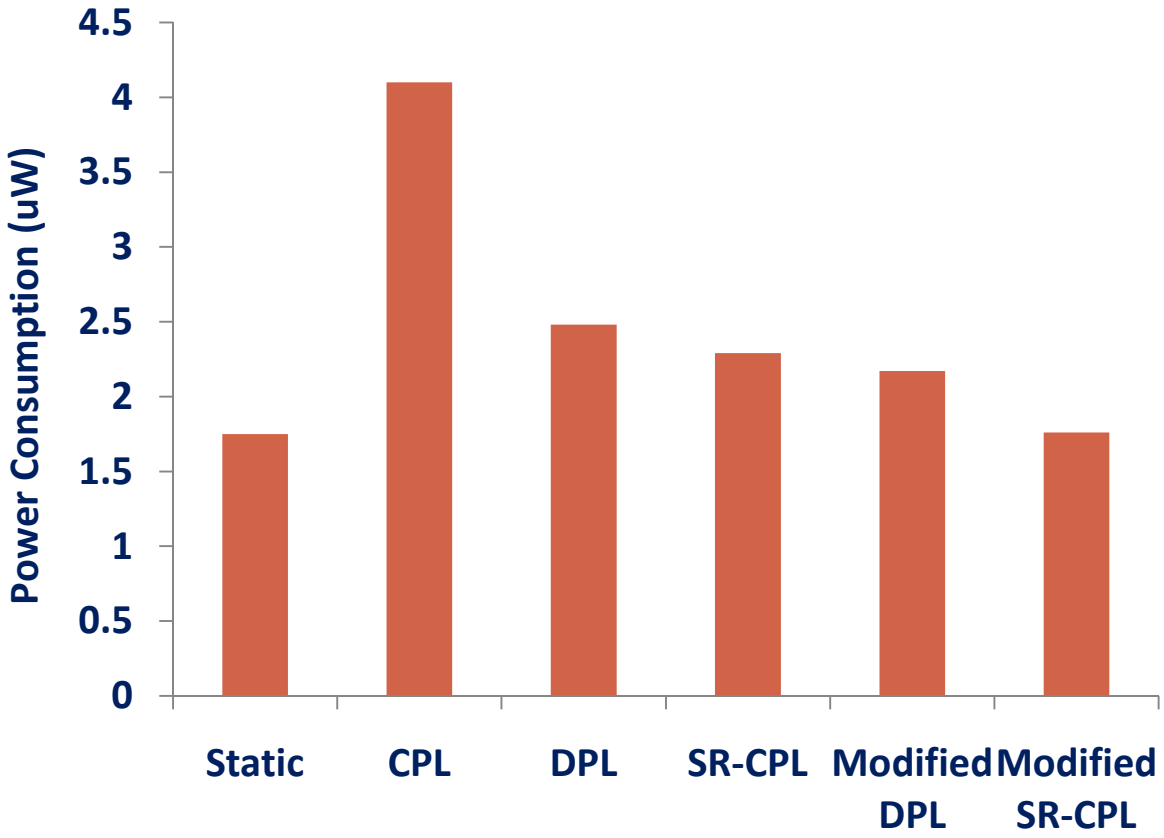


Fig.: Power Consumption of Various Adder Cells

Propagation Delay Comparison (45nm)

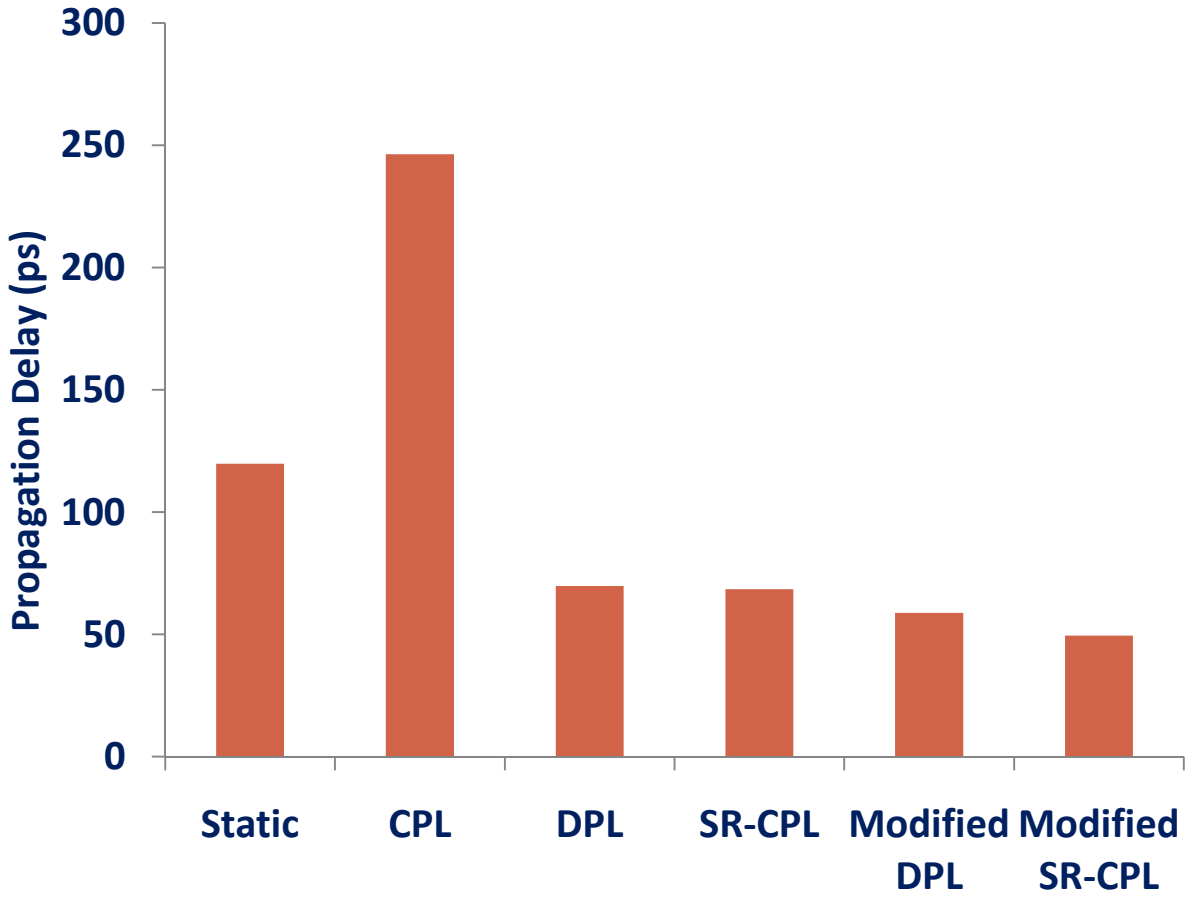


Fig. : Propagation Delay Comparison of Various Adder Cells

PDP Comparison (45nm)

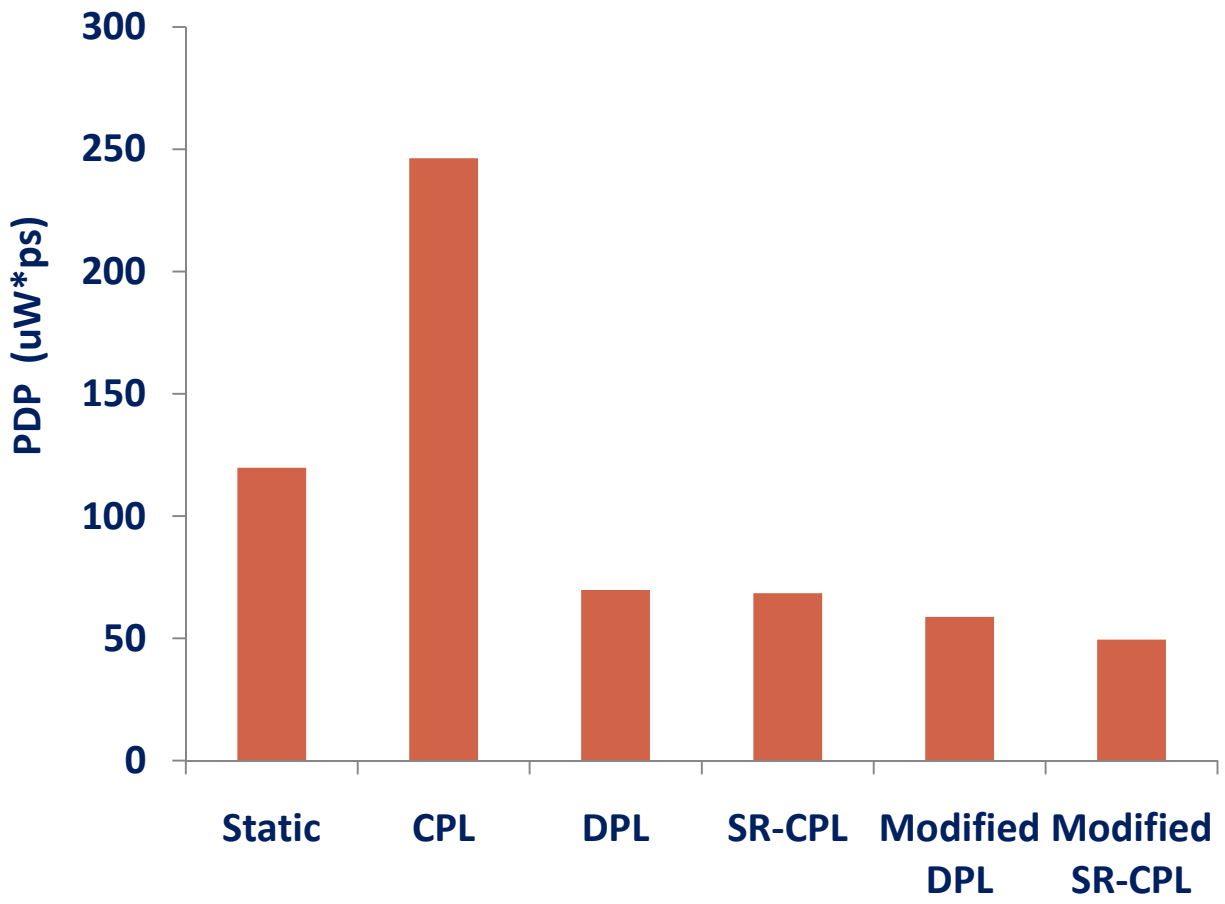


Fig. : PDP Comparison of Various Adder Cells

Supply Voltage Variations (45nm)

Logic Style	Supply Voltage (V)	Power (uW)	Delay (pS)	PDP (uW*pS)
Modified DPL	1.0V	2.203	27.09	59.67
	0.9V	1.832	34.01	62.30
	0.8V	1.596	41.12	65.62
Modified SR-CPL	1.0V	1.766	28.08	49.58
	0.9V	1.540	34.03	52.40
	0.8V	1.175	46.07	54.13

Table 4: Performance Metrics Comparison of Proposed Adder Cells for Supply Voltage Variation Using Cadence Virtuoso with 45nm Technology node

Temperature Variations (45nm)

Logic Style	Temperature (°C)	Power (uW)	Delay (pS)	PDP (uW*pS)
Modified DPL	27°C	2.20	27.18	59.79
	40°C	2.22	27.64	61.36
	70°C	2.28	28.74	65.52
Modified SR-CPL	27°C	1.56	28.12	43.86
	40°C	1.59	28.40	45.15
	70°C	1.65	29.03	47.89

Table 5: Performance Metrics Comparison of Proposed Adder Cells for Temperature Variation Using Cadence Virtuoso with 45nm Technology node

Conclusions

- High performance and energy efficient logic style has always been a popular research topic in the field of VLSI circuits.
- Novel Non-Clocked Logic Styles (Modified SR-CPL and Modified DPL) are proposed and their performance metrics were compared.
- The Modified DPL and Modified SR-CPL are Power Efficient than the other logic styles.

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