Abstract—The rising demand of computing power in mobile applications leads to the question how suitable FPGAs might be for usage in environments with limited energy resources. One of the most important benefits of FPGAs is their ability for reconfiguration and therefore adding a certain degree of flexibility in the field. In the recent years, various research groups investigated partial, dynamic reconfiguration capabilities of FPGAs and confirmed their applicability and suitability in systems with limited hardware and computing resources. However, dedicated power dissipation reduction measures are not featured by low-end designs as development and manufacturing costs take precedence over the extension of battery lifetime. In this paper, different, low-power optimized blocks are integrated into a partial slice and investigated upon the related static power consumption. Key components like LUTs, D-FFs, IO units and basic combinational circuitry are subject to power reduction and depict the baseline for further improvements in terms of extended battery runtime. These optimized blocks have been developed in past research work and enhanced by leakage current suppression measures at circuit level. The static power consumption and leakage currents of the newly implemented partial SLICE are evaluated and compared with a commercial baseline design.

I. INTRODUCTION

FPGAs are existing as commercial products in the market for many years already. A various number of vendors developed different variants of FPGAs for a wide range of applications. Some of these commercially available FPGAs already feature power saving mechanisms to make them more attractive for embedded applications in which a long battery lifetime is crucial. Keeping this in mind, for the purpose of this research it was important to highlight the FPGA types, which provide power dissipation reduction measures in order to check opportunities for even better implementations. Thus, selected FPGA types were chosen and are discussed in Section II. In parallel, the work of other research groups that dealt with low-power aspects of FPGAs was also evaluated and reviewed. In fact, many results were published about reconfigurable logic and low-power applications, which are also shortly introduced in Section II. Figure 1 depicts the internal structure of a FPGA and highlights the key elements which were subject for optimization. This basic principle of periodically allocated logic elements is valid for the majority of FPGAs.

It can be stated that two configurable logic blocks (CLBs) can be summarized to so a so called SLICE. Each CLB contains a Look-Up Table (LUT), a Data-FF (D-FF) and some basic logic gates. So, taking this circuitry and doubling it leads to the realization of a slice. Each slice contains one D-FF for storage of computed values prior to forwarding them to the next configurable logic block (CLB). All CLBs are cross connected to each other by programmable switch matrices (PSMs), which were not in scope of this research work.. Data exchange and in general communication to other devices is ensured by I/O blocks such as General Purpose Input Output (GPIO) units. Since even a low-cost FPGA, e.g. Xilinx Spartan 3A, contains up to 8320 CLBs [1], one can see the strong impact on area and energy consumption of these basic logic elements. Based on that, it is clear that transistor count and related area footprint might be a design constraint if costs take precedence over special characteristics like operation frequency or energy consumption.

In this paper, we investigate architectural elements of a selected baseline FPGA design on their low-power characteristics. In Section II, extracts of related academic research are presented. Section III and the related subsections describe the followed approach for implementing specific improvements in terms of power dissipation reduction for an entire SLICE and a GPIO. Lastly, Section IV concludes this paper.

II. RELATED WORK

Over the past years, various research activities have been carried out to explore different possibilities for decreasing power dissipation of reconfigurable logic [2] [3]. The Xilinx Spartan 3A has already served as reference architecture in an earlier research project [4]. In that specific research, the chosen method was to combine different, common power optimizations, e.g., voltage scaling, power gating, low-leakage
techniques for developing a new low-power FPGA. Different types of transistors with a different gate oxide thickness were selected to provide an efficient suppression of undesired leakage currents. If the selected manufacturing process supports these kinds of transistors, this method is very useful and should not be neglected when working on a design with decent static leakage current mitigation. Scaling down the supply voltage reduces power consumption and therefore a comparably low supply voltage was chosen [5]. This can be achieved either by implementing multiple, static supply voltages of different levels or by dynamically scaling down or up the supply voltage on demand of the target application. In general, dynamic voltage scaling was discussed multiple times, as it is the right choice to scale down dissipated power in an efficient and fast way [6]. The downside here is the amount of time spent on the implementation of a smart algorithm to trigger the power scaling in the right moment [7]. An alternative approach also takes advantage of the common power savings methods and combines these techniques with an operation of the FPGA in the subthreshold area [8]. This leads to ultra low-power operation of a FPGA, which might be of interest for internet of things (IoT) applications with very limited energy resources. Low-swing global interconnects, folded switch boxes and per path voltage scaling are also included. This approach delivers good results in terms of power savings, whilst slowing down maximum operation frequency of the chip. In another occasion, a different research group put their main focus on elaborating the minimum energy point of a new FPGA design. This energy point defines the lowest supply voltage provided to the FPGA, which still ensures reliable operation of the chip. For that purpose, a new FPGA design was presented based on a silicon-on-insulator (SOI) process [9]. Due to the low supply voltage, all memory cells used for configuration were replaced by latches for stable configuration data retention in subthreshold FPGAs. FPGAs, which are based on this special technique are qualified to be used in applications with a higher degree of environmental stress, e.g., electromagnetic radiation in space applications. For that reason, additional research work was published, introducing a low-power and radiation-tolerant FPGA [10] based on full depletion SOI technology. In direct comparison to existing commercial solutions for applications with high electrical stress, this chip consumes less power but this advantage goes back to a modified manufacturing process and not on improvements at circuit level.

In summary, it can be stated that FPGAs have entered the low-power market by featuring different mechanisms for extended battery lifetime. The most significant achievements in power savings rely on advancements in manufacturing technology as these designs take advantage of low-power benefits which come along with process shrinks. Second, integration of hard IP blocks for dedicated measures are listed as an efficient way to save both, battery power and logic resources as these blocks do not have to be developed by the customers but are ready to be used right after powering on the FPGA. Gating techniques, such as power gating and clock gating are mentioned as used design measures inside the fabric to keep static and dynamic power dissipation under control. At architectural level, the shift from 4-input to 6-input LUTs is described as meaningful step forward to minimize signal propagation delay and therefore to raise system through-put [11].

III. IMPROVEMENTS AT ARCHITECTURAL LEVEL

This research work started with a basic analysis of a low-budget FPGA architecture. All design and verification work was carried out by using a process design kit (PDK) consisting of Cadence Virtuoso and a TSMC 90nm technology. In general it can be also stated that elements of low-end FPGAs can be also found in their high-end counterparts like Xilinx Zync, but the downside of these products is usually the allocated costs. As already shown in Figure 1, all newly implemented blocks are highlighted in orange color. All PSMs are not highlighted as they have not been in focus of this work and will be addressed in future steps instead. So in the previous sections, selected circuits of a FPGA’s internal structure were analyzed, reworked and continuously improved to mitigate the power dissipation of each considered unit. These units were different Static Random Access Memory (SRAM) cells, various D-FFs designs and a number of selected tristate buffers. All circuits have been standalone tested and their correct function verified. Different measurements have been applied to check the achievements in terms of power dissipation reduction and leakage current suppression for both, static and dynamic behavior and several more, type-specific benchmarks. Despite the fact that it was not possible to implement a whole FPGA due to lack of PSMs, it was still interesting and necessary to analyze these circuits when integrated to a component at a higher hierarchy level of a FPGA. So the next steps led to the following activities:

- Integration of SRAM designs as Configuration Random Access Memory (CRAM) cells in a LUT
- Designing a SLICE by adding logic gates and D-FFs
- Implementing a GPIO by usage of the previously developed tristate buffer

These steps and the related results will be described and discussed in the following sections.

A. SLICE DESIGN

As each SLICE basically consists of two major blocks (separated by the dashed borderline in Figure 2) connected to each other, only one of these blocks was designed in this work.

This block and its modified components (highlighted in orange color) are displayed in Figure 2. It should be stated here that this illustration is a simplified of the real internal structure. For example, by taking a closer look on Figure 2, special
components like multiplexers without a dedicated Select input can be seen, shown in Figure 4. The modification of the partial SLICE in scope was done by a stepwise approach, starting by the replacement of the standard 6T LUT against an optimized Low-Power (LP) 4T LUT variant, which was based on a newly developed memory cell, shown in Figure 3.

This step was followed by replacing the logic gates and the D-FF by the newly developed, energy-saving counterparts.

These multiplexers in Figure 4 are usually configured by the toolchain in use, which means that the Select inputs are determined by the tool which streams the bitstream of the intended design into the FPGA. The upper MUX shown in that figure will forward either the upper or lower input, depending on whether Select will be configured to be HIGH or LOW. The lower MUX displayed in the same figure is another case: depending on the pre-configured Select input, either the static, pre-initialized ‘1’-input will be put through to the output of the MUX or the dynamic input. Depending on the configuration done by the toolchain, a vast number of different SLICE configurations is feasible. Based on that fact, measurements of leakage current and dissipated power during standby and power-off mode was determined and compared. The output curves of these simulations can be seen in Figure 5.

On the first glance, Figure 5 reveals a supposed delay in the transient response of the optimized SLICE while in idle state. It is not a real delay though as there are apparently different orders of magnitude between the standard and optimized design (µA vs. pA and µW vs. nW). The amplitude of the transition to be found in the output curve of $I_{\text{standby,L}}$ is smaller than of $I_{\text{standby}}$, so the alleged delay (which takes just approximately 1.5ns) is no one. Also, by having a closer look on the y-axes of the output curves, it is obvious that the scaling of the low-power outputs ($P_{\text{standby}}$ and $P_{\text{standby,L}}$) is different between both simulation. The same fact also applies to the consideration of leakage current in standby mode, which can be considered as an outlook on the overall results of this simulation. So, referring to more detailed numbers, Table I delivers the required information.

<table>
<thead>
<tr>
<th>SLICE type</th>
<th>$P_{\text{standby}}$</th>
<th>$I_{\text{standby}}$</th>
<th>$P_{\text{power,off}}$</th>
<th>N</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>48.65 µW</td>
<td>48.32 µA</td>
<td>2.878 nW</td>
<td>182</td>
</tr>
<tr>
<td>Low-power</td>
<td>1.722 nW</td>
<td>173.3 pA</td>
<td>934 pW</td>
<td>213</td>
</tr>
</tbody>
</table>

TABLE I. Summarized SLICE results in standby and power-off mode

Table I shows a massive improvement in terms of power savings by reducing power dissipation from 48.65µW down to 1.722nW during standby of the SLICE, which is a quite
considerable result. All previously applied improvements show their expected impact at this hierarchical level and lead to a tremendous reduction of current drain from limited energy resources. Going further by adding power gating to the supply voltage, further mitigation of undesired leakage currents are realized. This can be seen in Figure 6, where the effect of cutting off $V_{dd}$ from the circuit by setting $En$ to LOW is demonstrated. Table I also proves that this measure helps the partial standard SLICE to show up power savings in power off mode as well, but still can not beat the achievements of the optimized SLICE when completely turned off.

These achievements come at cost of a higher transistor count, leading to a difference of 17%. Beside the necessity of putting more attention to the layout of the design due to balancing out parasitic capacitances, the higher number of transistors is the most significant disadvantage of the newly implemented partial SLICE.

**B. GPIO design**

The step was to refer back to the introduced tristate buffer in earlier research work. As described in that section, a number of tristate buffers was analyzed upon their capabilities to, e.g., save as much battery power as possible in static and dynamic mode. In that sense, it was also of interest to explore the power savings capabilities when embedding a tristate buffer into a GPIO. This is shown in Figure 7.

At this point, it was beneficial to take advantage of the previous work steps, as a GPIO implies two CRAM cells to configure its internal multiplexers and three D-FFs, which are used to store input and output values, if necessary. Based on that fact, the consequent step was to use the low-power optimized parts from earlier research results and to integrate them into the GPIO architecture. Figure 7 features three D-FFs in total, hence the CR D-FF [12] was chosen to be applied in an energy saving GPIO. This newly developed CR D-FF is shown in Figure 8.

This new CR D-FF exploits the fact that D-FF are usually clocked devices, which enables the introduction of a precharge-evaluate mechanism. Basically, this design consists of a CR inverter (Master) and two cross-coupled NAND gates (Slave). Furthermore, inputs and outputs are differential, leading to very fast processing times as full swing voltage input / output is not required any more. Charge recycling is realized by exploiting the fact that only one of the differential Master-output nodes (Set/Reset) will be discharged during evaluation, whereas the other node will remain at a remarkably higher voltage. During the subsequent precharge phase, electron charge of the not-discharged output node is used to support $V_{dd}$ to charge the fully discharged node. This leads to measurable benefits in reduction of power consumption.

Next, two CRAM cells are required to configure the Select inputs of the multiplexers, so it was self-evident to implement the LP 4T CRAM [13] cell for this purpose. The main advantage of this implementation in comparison to a standard 6T CRAM cell is the modified precharge procedure. Instead of precharging both bitlines to $V_{dd}$, this circuit discharges both bitlines to $GND$. In addition to that, further power saving mechanisms were incorporated (transistor stacking in the pull-up network (PUN) and power gating transistor to
switch to a lower supply voltage in case the CRAM cell may enter an idle state). However, this new design requires modifications to auxiliary circuitry, e.g., the precharge circuit and sense amplifiers due to the discharge mechanisms (instead of precharging). Last but not least, the tristate buffer itself was realized by taking credit of one of the modified designs from previous design work, shown in Figure 9.

Fig. 9. Improved low-power tristate buffer with balanced highZ output [14]

The modified low-power tristate buffer with swapped output transistors shown in was chosen for the sake of power consumption reduction as it provides decent results, which were matching best to what was intended here. Similar to the previous section, the most interesting part was the standby and power off leakage current flow and power consumption. For the sake of a more detailed comparison, all simulations were done with all kinds of before developed tristate buffers. So for the first run, all GPIO variants were analyzed upon their capability to suppress leakage current and the related power dissipation during standby. The standard GPIO design is used as reference implementation and its leakage current and related power dissipation can be seen in Figure 10, followed by a comparison with the other designs.

Output curve of $I_{\text{standby}}$ in Figure 10 shows the expected transient response which goes back to internal capacities. One remarkable point at this is place is the order of magnitude of both, $I_{\text{standby}}$ and $P_{\text{standby}}$ which is in the order of $\mu A$ and $\mu W$, even after transient response has reached a stable value (from 1.8ns simulation time onwards). The reason for this relatively high order of magnitude is lacking of dedicated measure against the root cause of this outcome. In consequence, it was of high interest to see how the alternative, low-power designs would cut down leakage currents. The related results of $I_{\text{standby}}$ of all four investigated designs can be seen in Figure 11.

According to Figure 11 all alternative designs, the LP, Mod.

Fig. 10. Leakage current and dissipated power of the standard GPIO in standby mode

LP and AT GPIOs provide a decreased standby current when compared to the standard design. All of the alternative, low-power designs show a good performs in terms of leakage current reduction, but the Mod. LP GPIO is best though. Going further into detail, all related results during standby mode are summarized in Table II.

<table>
<thead>
<tr>
<th>GPIO type</th>
<th>$P_{\text{standby}}$</th>
<th>$I_{\text{standby}}$</th>
<th>$P_{\text{power off}}$</th>
<th>$N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>16.04 $\mu W$</td>
<td>16.32 $\mu A$</td>
<td>28.30 $p W$</td>
<td>78</td>
</tr>
<tr>
<td>LP</td>
<td>853.8 $n W$</td>
<td>64.73 $n A$</td>
<td>4.199 $p W$</td>
<td>87</td>
</tr>
<tr>
<td>Mod. LP</td>
<td>673.7 $n W$</td>
<td>51.64 $n A$</td>
<td>4.186 $p W$</td>
<td>87</td>
</tr>
<tr>
<td>AT</td>
<td>1.010 $\mu W$</td>
<td>287.0 $n A$</td>
<td>4.377 $p W$</td>
<td>87</td>
</tr>
</tbody>
</table>

TABLE II. Summarized GPIO results in standby and power-off mode

Referring to Table II, it can be seen that the modified LP GPIO offers the lowest average standby power dissipation $P_{\text{standby}}$ and average standby leakage current $I_{\text{standby}}$. The number of transistors $N$ is equal to the other, alternative designs and only makes a difference when taking the standard GPIO into consideration. Here, the more complex implementation of the integrated D-FFs, CRAM cells and tristate buffers leads to an increased number of transistors. The AT tristate buffer based GPIO falls behind the power reduction perfor-
mance of the other, newly implemented designs, but this result was expected according to the elaborated findings. Figure 12 illustrates the differences between the results in a graphical way, highlighting the effect of power loss mitigation after applying dedicated measures at circuit level. In addition to that, the average leakage current \( I_{\text{power, ff}} \) and the correlated, average power loss \( I_{\text{power, ff}} \) was measured and added to Table II. The respective numbers for \( I_{\text{power, ff}} \) and \( P_{\text{power, ff}} \) in this table underline the fact that the low-power optimized design outperform the standard design. It shall be stated here that other measures, e.g., clock-gating could be also applied in case that power gating is not an option due to the necessity to keep the data stored in the CRAM cells and D-FFs.

### IV. CONCLUSION

The integration of components, which have been developed with focus on low-power optimization, shows an overall positive effect in terms of power consumption reduction. All low-power components contribute successfully to considerable power savings. Despite the fact that these results are limited to the static behavior of the circuits in scope, it can be still stated that embedding power saving measures at the lowest hierarchical level is a reasonable decision. Each integrated component, the LUT and the partial SLICE take credit of their power-optimized subcomponents and provide smaller leakage currents. This fact has an immediate impact on the overall power dissipation and qualifies each integrated component for low-power applications. It also proves that it is reasonable to optimize even the most basic logic blocks of a design, as every contribution in low-power application counts. However, these improvements come at cost of additional transistors and dedicated manufacturing technologies. A higher number of transistors will subsequently lead to a lower yield after production as a penalty in the area footprint must be accepted. Furthermore, a special manufacturing technology might have an impact on the related costs of a chip. The benefits and drawbacks must be carefully measured in dependance of the targeted application, which should have an impact on the decision whether the mentioned drawbacks can neglected in comparison to the gained advantages. In future work, the Power-Delay-Product (PDP) shall be evaluated and compared with existing designs. The PDP was not in focus during this research work as highest priority was placed on achieving significant reductions of power consumption only. All measurements (also presented in the respective references) display either average or static power consumption. Dynamic power consumption can be calculated by subtracting static power consumption from average power consumption results. However, current research works investigates both PDP and EDP (Energy-Delay-Product) for all newly developed components as well as for the entire SLICE and will be made available in future publications.

### REFERENCES