Overcoming Bathtub Failure Curve for Dependable Flash Storage Through Exploiting RAID Protection

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Abstract—The advent of MLC/TLC/QLC and 3D/4D NAND flash memory technologies leads to increased capacity along with decreased reliability of SSDs. Flash storage is increasingly used in various fields such as mobile devices, internet of things (IoT) devices, home appliances, automobiles, etc. In such a system, the error handling techniques of the storage device have a great influence on the reliability of the system. Generally, failure rate of a storage device follows the bathtub curve. In particular, flash storage suffers from high bit error rate as flash memory undergoes P/E (Program/Erase) cycles. Though error rate of flash storage such as SSDs follows the bathtub curve, most of SSDs use the ECC scheme with fixed strength against failures. Hence, we propose Flexible Strength RAID (FS-RAID) scheme that employs RAID configuration and dynamically adjusts its strength against failures according to the typical failure rate of the device lifetime. In addition, we propose a method to greatly improve reliability by combining RAID parity and existing ECC. Through the evaluation using SSD simulator, we show that the proposed two techniques are quite effective.

I. INTRODUCTION

The advent of MLC (Multi-Level Cell)/TLC (Triple-Level Cell)/QLC (Quad-Level Cell) [12] and 3D/4D NAND flash memory technologies [4], [13] leads to increased capacity along with decreased reliability of SSDs. Flash memory has a feature that error rate increases greatly as the number of write operations increases. Basically, Error correction code (ECC) is used to detect and correct errors in flash memory based storage. Flash storage is increasingly used in various fields such as mobile devices, internet of things (IoT) devices, home appliances, automobiles, military equipment, data centers, etc. In such a system, the error handling technique of the storage device has a great influence on the reliability of the system.

Generally, failure rate of a storage device follows the bathtub curve shown in Figure 1 [7]. The curve can be divided into three regions according to lifetime stage, namely Early Failure Period (EFP), Constant Failure Period (CFP), and Wear-out Failure Period (WFP). In early stage of lifetime denoted as EFP in Figure 1, a device shows high failure rate. Then, the device shows low and stable error rate in CFP region. Finally, device error rate increases again in WFP region as its lifetime expires. Specifically, SSDs suffers from high bit error rate as flash memory undergoes P/E (Program/Erase) cycles. Though error rate of SSDs follow the bathtub curve, most of SSDs use the ECC scheme with fixed strength against failures. Hence, we propose Flexible Strength RAID (FS-RAID) scheme that employs redundant array of independent disks (RAID) configuration and dynamically adjusts its strength against failures according to the typical failure rate of the device lifetime.

In addition, we propose a novel method to greatly improve reliability by combining ability of RAID parity and ECC. Both ECC and RAID parity are a kind of additional redundancy for error detection and correction [14]. These two techniques deal with errors that occur in each layer independently of each other. However, if both techniques complement each other, reliability can be greatly improved.

The remainder of this paper is organized as follows. In the next section, we review flash based SSD and reliability of SSDs. Then, in Section III, we present the design of the FS-RAID and combining RAID parity and ECC. Then we describe the evaluation results in Section IV. Finally, we conclude the paper with a summary and conclusions in Section V.

II. BACKGROUND AND RELATED WORK

In this section, we first briefly describe flash memory and SSDs then explain the reliability of flash based SSDs.

A. Flash memory and SSDs

Today’s flash storage devices are mostly provided to users in the form of SSDs. SSDs are composed of many NAND flash memory chips connected through channels [3], [2], [8]. Such configuration allows SSDs to achieve high performance
through parallel access of those resources. NAND flash memory chips consists of multiple dies and planes, which has multiple blocks, and each block has multiple pages \([5], [11], [8]\). The basic operations on flash memory are the read and write operations, and these are done in page units. I/O requests from the host can be interleaved across multiple channels and the requests then, can be further interleaved with multiple dies. Requests arriving at the chip level can be processed on each plane simultaneously \([5], [8]\). A unique characteristic of flash memory is that data cannot be overwritten on a used page. In order to over-write a page, the block containing the page has to be erased first. This erase operation is another order of magnitude slower than a page write operation. Furthermore, the number of erasures after writing, generally termed the Program/Erasur (P/E) cycle, is limited depending on the manufacturing technology. Today, three types of technologies, namely, SLC, MLC, and TLC, are in wide use and their P/E cycles range roughly in the 100 thousand, 10 thousand, and 1 thousand range, respectively, but also depend heavily on the manufacturers \([9], [6]\). Clean pages will eventually run out as overwrites are not possible. To rid of invalid pages, which hold old data that were logically overwritten, and turn them back to clean pages, a process called garbage collection (GC) is performed. As erasures can happen only in block units, GC starts by selecting the block to be erased (victim selection). However, this victim block may possibly hold a mix of valid and invalid pages, so before the erase operation is performed on this block, valid pages in this block must first be moved to unused pages in other blocks. This moving of valid pages is called write amplification (WA) and is a major source of GC overhead.

B. Reliability of Flash memory

The flash memory has a limited number of P/E cycles depending on the process technology. The bit error rate of the flash memory increases in proportion to the cumulative P/E count. Due to these characteristics, the bit error rate is a representative measure of the reliability of the flash memory.

Figure 2 shows the configuration of ECC and RAID inside the SSD. ECC is stored in the out of band area of each page, and bit errors of page data is detected and corrected by ECC. RAID parity is used to recover from errors for a stripe.

III. DESIGN

In this section, we describe two proposed techniques, FS-RAID and combining RAID parity and ECC.

A. Architecture of FS-RAID

Most of existing data protection techniques use fixed protection strength to cope with errors during the entire lifespan of devices. However, most devices, including storage devices, follow the bathtub failure curve. As introduced in Section I, device failure periods are generally divided into three categories: Early Failure Period (EFP), Constant Failure Period (CFP), and Wear-out Failure Period (WFP). In this study, we also assume that flash memory storage follows the three failure phases. Moreover, flash memory has a feature that the error rate increases sharply as the amount of writes increases.

Therefore, we propose Flexible Strength RAID (FS-RAID) scheme that employs RAID protection and dynamically adjusts its strength against failures according to the each phase of device lifetime. In order to this, we employ RAID parity configuration in addition to ECC in flash memory to improve the reliability. Figure 3 shows an overall architecture of FS-RAID. A stripe consists of pages of the same number across chip 0-5. RAID enables recovery of errors in a single stripe unit. The number of parity in one stripe is the maximum number of concurrent errors that can be recovered by RAID schemes. In other words, if there are two parities in one stripe, RAID can recover the error and provide the corrected data to the user even if an error occurs simultaneously up to two pages in a stripe. Therefore, if the number of parities is increased, the error rate is greatly reduced. However, as parity increases, overhead is imposed on capacity, performance, and wear out. Therefore, a design considering reliability and parity overhead is needed by dynamically adjusting the number of parities according to the error occurrence rate.

Figure 3 shows the layout where parities are placed for each period. Specifically, to face high failure rate of the EFP/WFP period, FS-RAID employs RAID-6 configuration that writes two parities in a stripe. In CFP region, it uses RAID-5 configuration that writes one parity in a stripe. If
B. Combining an ability of RAID parity and ECC

We describe how to combine an ability of RAID parity and ECC and benefits from it. Through this proposed scheme, we can reduce a number of page writes that occurs during ECC error correction using RAID parity. A conventional method writes corrected data to a new page immediately after correction with ECC when an error is detected. In order to reduce the additional writes for corrected data from ECC, [10] proposed a technique that reduces the number of page writes by writing the corrected data to a new page only when an error of n bits or more is detected by ECC shown in Figure 4.

In this paper, we propose a method that can reduce page writing more than existing methods. Figure 5 shows the procedure for detecting the error and sending it to the user. In the Decision phase of Figure 5, the decision is made in three cases based on the number of error bits, the number of P/E, the data write time, and error rate of the page. Case #1 is selected when the number of P/E is small, data write time is recent, and the number of error bits is small. In this case, corrected data is transferred to the host, but writing corrected data to page is skipped. Case #2, if the number of P/E or the error rate is high, the page is written after error correction using ECC. Case #3, if errors exceed the correctable range with ECC, the page is written after error correction using parity.

IV. Evaluation

A. Environment

We implemented FS-RAID and combining RAID parity and ECC on DiskSim with SSD Extension to evaluate performance and reliability with other schemes. In the evaluation, we simulate an 128GB SSD with TLC NAND flash memory.

B. Analysis of Reliability

The comparison targets are ECC, RAID-5, and eSAP. All of those techniques support a fixed protection strength over the entire lifetime of the devices. RAID-5 is a traditional RAID technique where one parity per stripe is maintained. The elastic stripe anywhere parity (eSAP) adopts a log-structured write and the parity position can be placed anywhere within the stripe [9].

With analytic models derived in [9] and parameters obtained from simulation results of 128GB SSD with TLC chips under Financial workload [1], we calculate error rate of an SSD employing FS-RAID scheme and compare them with SSDs using three different schemes, namely, ECC-only, RAID-5, and eSAP. Particularly, eSAP scheme employs log-structured style RAID-5 configuration but does not change its configuration according to the error rate variation [9].

Figure 6 shows Uncorrectable Page Error Rate (UPER) and P/E cycles of four schemes, where X-axis denotes total amount of data written to the SSD in TB (Tera Byte) unit and names in the parentheses represent lifetime stage of the device shown in Figure 1.

In Figure 6(a), FS-RAID shows the lowest UPER in both EFP and WFP regions as it increases redundancy to cope with high failure rate in those regions. Also, though FS-RAID writes two parities in EFP and WFP regions, it shows longer lifetime than conventional RAID-5 due to its log-structured style RAID configuration and reduced number of parity updates as seen in Fig. 6(b) that presents average P/E cycles of flash memory.

C. Written Amount of Corrected Data

We compared the combing RAID parity and ECC technique with the existing technique [10] on the SSD simulator. We observed that the proposed scheme reduce page write by 12% compared to the existing technique for Financial workload [1].
V. Conclusion

We present two techniques namely FS-RAID and combining RAID parity and ECC. Using both of these proposed techniques, we significantly improve the reliability and lifespan of flash storage. In addition, we also reduce the amount of page writes due to error correction with ECC. We introduced a method to dynamically adjust the protection strength to solve the bathtub failure curve characteristic of the storage device. This is more efficient than the conventional fixed error coping technique. Particularly, it is more effective in a flash storage device in which the error rate increases sharply as the number of P/E increases. Moreover, combining an ability of RAID parity and ECC is effective in reducing the number of writes through delaying corrected data from ECC to new pages. We show that the proposed two techniques are quite effective through simulation based evaluation.

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