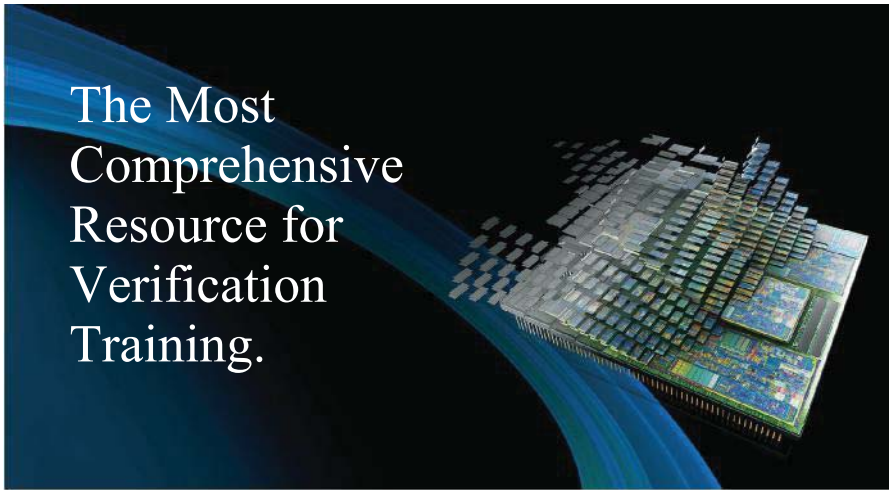
Evolving Verification Capabilities



Academy Format

The Verification Academy is organized into a collection of free online courses (modules) and resources, focusing on key aspects of advanced functional verification. Each course consists of multiple sessions—allowing the participant to pick and choose specific topics of interest, as well as revisit any specific topics for future reference. In addition, each session identifies its appropriate target audience, which includes:

Crawl: content is technical, but at an introductory level, and of interest to novice engineers.

Walk: content is of general interest, particularly to managers, but also engineers.

Run: content is technical in nature, and of interest to engineers.

The Verification Academy will provide you with a unique opportunity to develop an understanding of how to mature your organization's processes so that you can then reap the benefits that advanced functional verification offers.

Universal Verification Methodology (UVM)

The Verification Academy is the most complete UVM Online resource. You'll find everything you need to get up to speed on UVM, from downloading kit(s) to extensive documentation and explanations.

The UVM Online Methodology Cookbook is the only available authoritative UVM resource that is continually updated as new UVM versions are released. Easy to navigate and search, the Cookbook supplies in-depth articles and downloadable examples to explain UVM to engineers of all skill levels.

In addition to several online video training courses, the Verification Academy also includes lively discussion forums with over 54,000 members to quickly provide answers to your specific UVM and methodology questions.

Overview:

- Industry recognized subject matter expert commentary spanning multiple verification disciplines giving you a broad perspective and knowledge of the topic being covered.
- Thirty-two video courses providing over sixty hours of instructional material that can be applied immediately in your work environment.
- Video content downloadable and accessible in multiple formats including tablet and mobile devices for offline viewing.
- The Verification Methodology Cookbook features extensive documentation and code examples that are exclusively available for download on the Verification Academy.
- Verification Academy Patterns Library – a collection of solutions from specification to methodology to implementation across multiple verification engines including formal, simulation, and emulation.
- Discussion forums with over 10K topics and over 54,000 users.

Courses Available:

Introduction to DO-254
In this course you will learn basic understanding of the key concepts of DO-254.

UVM Framework - A Bite at a Time
In this course you will learn the architecture, flow, generation, and use of UVM Framework testbenches.

Handling Inconclusive Assertions in Formal Verification
In this course you will introduced to techniques to help formal tools solve inconclusive assertions.

Formal Coverage
In this course you will be introduced to simulation coverage, property debug, resolving inconclusives and over-constraint & reachability analysis.

Sequential Logic Equivalence Checking
In this course, you will be introduced to the concept of sequential logic equivalence checking and its common applications.

UVM Debug
In this course, we examine common UVM debug issues, and provide a systematic set of recommendations to effectively address them.

Portable Stimulus Basics
This course will provide an introduction to the upcoming Portable Stimulus standard.

SystemVerilog OOP for UVM Verification
This course is aimed at introducing the OOP features in SystemVerilo g most commonly used by the UVM in the simplest form.

Introduction to Unit Testing with SVUnit
SVUnit is an open-source test framework for ASIC and FPGA developers writing Verilog/SystemVerilog code.

Power Aware CDC Verification
This course describes the low power CDC methodology by discussing the low power CDC challenges and verification methodology.

Getting Started with Formal-Based Technology
This course introduces basic concepts and terminology that should be useful by any engineer wishing to mature their formal-based technology skills.

Formal Assertion-Based Verification
In this course the instructors will show how to get started with direct property checking.

Formal-Based Technology: Automatic Formal Solutions
After a brief introductory session outlining the general architecture of formal apps, each subsequent session will deep dive on a specific verification challenge and the corresponding formal application.

Introduction to UVM
This course will guide you from rudimentary SystemVerilog through a complete UVM testbench. You would then have knowledge with all of the major components of UVM as well as their concepts.

Power Aware Verification
This course introduces the IEEE Std 1801 Unified Power Format (UPF) for specification of active power management architectures.

VHDL-2008 Why It Matters
This course is designed to explain the value of the new VHDL-2008 improvements for both Design and Verification Engineers

Metrics in SoC Verification
In this course, we take a broader view of metrics—beyond traditional coverage measurements.

UVM Connect
This course discusses how to move your existing verification environments to UVM in an evolutionary step-by-step manner.

Advanced UVM
The goal of the Advanced UVM course is to improve your understanding so you can move beyond the basic block-level testbenches. This course builds upon the concepts and fundamentals discussed in the Basic UVM course.

Basic UVM
This course is for engineers that recognize they have a functional verification problem but have little or no experience with constrained-random verification or object-oriented programming.

SystemVerilog Testbench Acceleration
This course will give you the confidence required to start the process of investigating and creating a single testbench environment that can be used for both simulation as well as hardware-assisted acceleration.

AMS Design Verification: Configuration Schemes, Improving Performance and Quality
These courses will cover a general understanding of Mixed-Signal design types and design verification requirements with a high-level overview of verification choices and results.

Testbench Co-Emulation: SystemC & TLM 2.0
This course advocates that functional verification through modern SystemC testbenches paired with co-emulation enables further verification productivity improvements in terms of raw performance.

Verification Planning and Management
This course is an introduction towards creating a verification blueprint.

FPGA Verification Capabilities
This course introduces techniques for addressing complexity by evolving your organization's FPGA verification process capabilities.

Clock-Domain Crossing Verification (CDC)
This course introduces a set of steps for advancing an organization's clock-domain crossing verification skills, infrastructure, and metrics for measuring success while identifying process areas requiring improvement.

Assertion-Based Verification (ABV)
This course introduces a set of steps for advancing an organization's ABV skills, infrastructure, and metrics for measuring success while identifying process areas requiring improvement.

Evolving Verification Capabilities
This course provides a common framework for all advanced functional verification courses contained within the Verification Academy.

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To learn more about the Verification Academy, visit our website www.verificationacademy.org

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