PE
electrical and computer: computer engineering practice exam
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About NCEES
NCEES is a nonprofit organization made up of the U.S. engineering and surveying licensing boards in all 50 states, the U.S. territories, and the District of Columbia. We develop and score the exams used for engineering and surveying licensure in the United States. NCEES also promotes professional mobility through its services for licensees and its member boards.

Engineering licensure in the United States is regulated by licensing boards in each state and territory. These boards set and maintain the standards that protect the public they serve. As a result, licensing requirements and procedures vary by jurisdiction, so stay in touch with your board (ncees.org/licensing-boards).

Exam format
The PE Electrical and Computer: Computer Engineering exam is computer-based. It contains 85 questions and is administered year-round via computer at approved Pearson VUE test centers. A 9.5-hour appointment time includes a tutorial, the exam, and a break. You’ll have 8.5 hours to complete the actual exam.

In addition to traditional multiple-choice questions with one correct answer, the PE Computer Engineering exam uses common alternative item types such as

- Multiple correct options—allows multiple choices to be correct
- Point and click—requires examinees to click on part of a graphic to answer
- Drag and drop—requires examinees to click on and drag items to match, sort, rank, or label
- Fill in the blank—provides a space for examinees to enter a response to the question

To familiarize yourself with the format, style, and navigation of a computer-based exam, view the demo on ncees.org/ExamPrep.

Examinee Guide
The *NCEES Examinee Guide* is the official guide to policies and procedures for all NCEES exams. During exam registration and again on exam day, examinees must agree to abide by the conditions in the *Examinee Guide*, which includes the CBT Examinee Rules and Agreement. You can download the *Examinee Guide* at ncees.org/exams. It is your responsibility to make sure you have the current version.

Scoring and reporting
Results for computer-based exams are typically available 7–10 days after you take the exam. You will receive an email notification from NCEES with instructions to view your results in your MyNCEES account. All results are reported as pass or fail.

Updates on exam content and procedures
Visit us at [ncees.org/exams](http://ncees.org/exams) for updates on everything exam-related, including specifications, exam-day policies, scoring, and corrections to published exam preparation materials. This is also where you will register for the exam and find additional steps you should follow in your state to be approved for the exam.
NCEES Principles and Practice of Engineering Examination
ELECTRICAL AND COMPUTER—COMPUTER ENGINEERING
CBT Exam Specifications
Effective Beginning with the October 2021 Examination

• The exam topics have not changed since April 2018 when they were originally published.
• The PE Computer Engineering exam is computer-based. It is closed book with an electronic reference.
• Examinees have 9.5 hours to complete the exam, which contains 85 multiple-choice questions. The 9.5-hour time includes a tutorial and an optional scheduled break. Examinee works all questions.
• The exam uses both the International System of units (SI) and the US Customary System (USCS).
• The exam is developed with questions that will require a variety of approaches and methodologies, including design, analysis, and application. Some questions may require knowledge of engineering economics.
• The knowledge areas specified as examples of kinds of knowledge are not exclusive or exhaustive categories.

Number of Questions

1. Computer Systems  21–32
   A. Data Representation  5–8
      1. Number representation
      2. Character representation
      3. Encoding schemes
      4. Error detection and correction
      5. Data compression
      6. Encryption
   B. Computer Architecture  16–24
      1. Computer organization and processor design
      2. Embedded systems
      3. System architecture
      4. Memory systems
      5. System performance

2. Embedded System Software  14–21
   A. Systems Software  7–11
      1. Operating systems
      2. Real-time operating systems
      3. Computer security
      4. Device drivers
      5. Interrupts and exception handling
      6. Firmware (e.g., BIOS)
B. Application Development 7–11
   1. Software design
   2. Quality assurance
   3. Software fundamentals
   4. Development tools (e.g., debuggers, disassemblers, trace tools, emulators)

3. Hardware 21–32
   A. Digital Devices and Systems 9–14
      1. Memory devices
      2. Standard modular devices (e.g., multiplexers)
      3. Programmable devices
      4. Serialization and deserialization
      5. Combinational and sequential circuits
      6. Implementation technology (e.g., FPGA, ASIC)
      7. Arithmetic hardware (e.g., ALU, FPU)
      8. Synchronous
      9. Asynchronous
     10. Testability
     11. Tristate logic
     12. System design (datapath/control)
   B. Digital Electronics 5–8
      1. Basic solid-state devices
      2. Operating parameters
      3. Data conversion and instrumentation
      4. Circuit implementation
      5. Timing design and analysis
   C. Hardware Description Languages 7–11
      1. Testbench development
      2. Abstraction levels (RTL, structural, behavioral) and hierarchical design
      3. Synthesis issues
      4. Verification (e.g., assertions, coverage)

4. Computer Networks 14–21
   A. Protocols and Standards 2–3
   B. Configuration/Topology 4–6
      1. Wireless
      2. Wired and optical
   C. Hardware 3–5
   D. Safety, Security, Privacy 3–5
   E. Cyber Physical Systems 2–3
      1. Distributed sensing
      2. Self-configuration
      3. Mobile network systems
3. The 32-bit unsigned value \((12345678)_{16}\) is written to memory from a byte-addressable, big-endian processor. When this data is read back as four sequential bytes starting at the same lowest initial address, what will be the correct order of the data?

- A. \((12)_{16}, \ (34)_{16}, \ (56)_{16}, \ (78)_{16}\)
- B. \((78)_{16}, \ (56)_{16}, \ (34)_{16}, \ (12)_{16}\)
- C. \((48)_{16}, \ (2C)_{16}, \ (6A)_{16}, \ (1E)_{16}\)
- D. \((1E)_{16}, \ (6A)_{16}, \ (2C)_{16}, \ (48)_{16}\)

4. A cryptographic system is considered computationally secure. Which of the following events have the greatest potential to make the cryptographic system considered no longer computationally secure?

Select the **three** that apply.

- A. A new, more secure key distribution system is developed.
- B. A new generation of CPUs is released.
- C. A faster algorithm is developed for a basic mathematical function.
- D. An implementation of the system's algorithm is formally proved.
- E. A faster algorithm is developed for decrypting a message in the system.
13. In a computer program, 60% of the instructions must be executed sequentially and the remaining 40% can be parallelized among eight different processors. What speedup can be achieved when the program is recompiled to run on an 8-processor parallel computer?

The speedup that can be achieved is ___________.

Enter your answer in the blank to three decimal places.

14. A program runs on a single CPU in 3 seconds. A computer engineer determines that 40% of the instructions in the program can run in parallel. The smallest achievable new total runtime (sec) is most nearly:

- A. 0.6
- B. 1.2
- C. 1.7
- D. 1.8

15. A four-input (variables = PABC) combinational circuit that serves as an interface between components of a special-purpose digital system is to be designed. The most significant bit P is a parity bit, and the circuit output Z is to be a 0 (indicating error) if the parity is even. An input combination PABC for which the output Z should be 0 (low) is:

- A. (0010)₂
- B. (0100)₂
- C. (0101)₂
- D. (0111)₂
38. An FPGA's logic is implemented in 2-input lookup tables (LUTs). Each LUT has inputs $a_1a_0$ and output $y$. The FPGA must implement the following function:

$$D(A, B, C) = (A\bar{B})C$$

Assume the LUT on the right has been programmed as shown.

Match the required data values into the left LUT to complete the implementation.
71. In the structured design approach for software development, a chief tool is the structure chart. Which of the following is the most accurate description of the structure chart?

- A. The structure chart is nothing more than a flow chart.
- B. The structure chart shows the partitioning of software into modules, module organization, and what information modules pass back and forth.
- C. The structure chart concentrates on the internal aspects of all modules within the chart.
- D. The structure chart shows the partitioning of software into modules and module organization; however, it does not depict data movement between modules.

72. Software verification activities begin when software specifications are developed. At this point, the overall testing goals and approach are formulated. Listed below are steps in the software verification process.

- **Test cases**: Test cases are developed and test data to support them are generated.
- **Unit tests**: Unit testing, or module-level testing, is done with stubs and drivers used for support.
- **Interface tests**: Tests performed to check the interoperability of modules.
- **Regression tests**: Tests performed earlier are rerun as regression tests to make sure that any corrections implemented during the software verification process have not introduced new problems.

Assume top-down testing techniques are applied. List in order the steps that must be accomplished for software verification.

| First Step |  |
| Second Step |  |
| Third Step |  |
| Fourth Step |  |

- Test cases
- Unit tests
- Interface tests
- Regression tests
4. New CPU Generation: Correct. New faster generations of CPUs may allow the cryptographic system to be broken faster and thus no longer be computationally secure.

Faster decryption algorithm: Correct. The faster decryption algorithm may allow brute force key space exploration feasible.

Faster mathematical function algorithm: Correct. If the function is used in the system's algorithm, the faster algorithm may make the system no longer computationally secure.

New key distribution system: Incorrect. An improved key distribution system should not impact the computational security of the system and an improvement should make it more secure.

Formally proved implementation: Incorrect. Whether the algorithm is formally proved or not should not impact its computational security.

THE CORRECT ANSWERS ARE: B, C, E

5. The instruction is (AB6)\textsubscript{16} or (101010110110)\textsubscript{2}. Extracting the opcode yields (0101)\textsubscript{2}, which corresponds to \texttt{add}.

THE CORRECT ANSWER IS: B

6. The key feature of a Harvard architecture is separation of code and data spaces.

THE CORRECT ANSWER IS: B

7. The pipeline single clock cycle must be slow enough to accommodate the slowest pipeline stage latency. This fact contradicts Option B; therefore, Option B is false.

THE CORRECT ANSWER IS: B

8. Eliminate Option A: These are registers accessible to users, but others needed as an integral part of the architecture are missing.

Eliminate Option B: General-purpose registers are almost always available but are not actually necessary.

Eliminate Option C: Since the instruction register is not available to users, it is often ignored or forgotten.

THE CORRECT ANSWER IS: D
13. The speedup, $SU$, can be calculated using a version of Amdahl's law derived for parallel processors.

$$SU = \frac{1}{F_s + \frac{1 - F_s}{N}}$$

where $F_s$ is the fraction of code that must run serially. Thus,

$$SU = \frac{1}{0.6 + \frac{1 - 0.6}{8}} = 1.538$$

**THE CORRECT ANSWER RANGE IS $\geq 1.537$ and $\leq 1.539$.**

14. The maximum speedup, $SU$, can be calculated using Amdahl's law:

$$SU = \frac{1}{1 - p}$$

where $p$ is the percentage of code that is parallelizable. Thus,

$$SU = \frac{1}{1 - 0.4} = 1.667$$

Since $SU$ is the ratio of the runtime on the single processor and the runtime on the dual core, the time is:

$$SU = \frac{R_{1\text{core}}}{R_{2\text{core}}}$$

thus

$$R_{2\text{core}} = \frac{R_{1\text{core}}}{SU} = \frac{3}{1.667} = 1.8 \text{ sec}$$

**THE CORRECT ANSWER IS: D**

15. Even parity means that the number of set bits is even.

**THE CORRECT ANSWER IS: C**

16. It is the definition of rate monotonic.

Eliminate Options A, B, and C: Alternate scheduling techniques but not the definition.

**THE CORRECT ANSWER IS: D**
36. The state transitions for the circuit are 001, 100, 010, 101, 110, 111, 011, …

**THE CORRECT ANSWER IS: 7**


**THE CORRECT ANSWER IS: A**

38. Let the output of the left LUT be K. Then, the right LUT implements \( D = \overline{K}C = K + \overline{C} \).

Transforming \( D(A, B, C) = (A + B)C = (A + B) + \overline{C} \)

that leaves \( K(A, B) = A + B = \overline{AB} \) to be implemented by the left LUT.

The truth table (with A as the most significant bit) is

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A'B</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

which is what must entered in the left LUT data.

**THE CORRECT ANSWER IS SHOWN ABOVE.**
68. Autonegotiation is part of the IEEE 802.3 standard to allow compatibility.

**THE CORRECT ANSWER IS: D**

69. The diameter of a graph is defined as the maximum length between the shortest path of any two vertices (or in this case computers).

**THE CORRECT ANSWER IS: C**

70. TCP/IP is the only reliable transport protocol listed.

**THE CORRECT ANSWER IS: B**

71. The structure chart shows the partitioning of software into modules, module organization, and what information modules pass back and forth. This is the most accurate description of the structure chart. Options A, C, and D are incorrect definitions.

**THE CORRECT ANSWER IS: B**

72. Develop test cases (I), interface tests (III), unit tests (II), regression tests (IV).

<table>
<thead>
<tr>
<th>First Step</th>
<th>Test cases</th>
</tr>
</thead>
<tbody>
<tr>
<td>Second Step</td>
<td>Interface tests</td>
</tr>
<tr>
<td>Third Step</td>
<td>Unit tests</td>
</tr>
<tr>
<td>Fourth Step</td>
<td>Regression tests</td>
</tr>
</tbody>
</table>

**THE CORRECT ANSWER IS SHOWN ABOVE.**

73. In bus topology, a terminating resistor must be inserted to prevent the signal from echoing back when it reaches the end of the bus.

**THE CORRECT ANSWER IS: D**

74. Eliminate Option A: A repeater does not segregate networks; it extends their maximum distance.
   Eliminate Option C: A switch connects devices together; it does not segregate networks.
   Eliminate Option D: A gateway is used to convert between protocols.

**THE CORRECT ANSWER IS: B**