BKK19-325 Design your own custom co-processors and acceleration hardware with Ultra96

03.Apr.2019 Kevin Keryk
Avnet Public
Co-Processing History
Co-Processing History
Co-Processing History
Co-Processing History
Co-Processors and Acceleration Hardware

GPU

DSP

DPU

Linaro Connect BKK19-321 FPGAs for Highest Performance Inference
# Custom Co-Processors and Acceleration Hardware

<table>
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<tr>
<th>Metric</th>
<th>ASSP</th>
<th>2-Chips</th>
<th>ASIC</th>
<th>Zynq UltraScale+</th>
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<tr>
<td>Performance</td>
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<td>Power</td>
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<td>Time-to-Market</td>
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<tr>
<td>Scalability</td>
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<tr>
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<td>TCO</td>
<td>+</td>
<td>+</td>
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- **Positive**
- **Negative**
- **Neutral**
Programmable Logic - What is it?

- Functions as a ROM
- Constant electrical delay through LUT
- Limited only by number of inputs and outputs, not complexity

Look Up Table – LUT

Generates a deterministic output for a given set of inputs

Logic Block Resources

[Diagram of LUT and logic block resources]
Programmable Logic - What is it?

Logic Block Resources

Routing Resources
Programmable Logic - What is it?

Smallest Spartan-3A Device Mask Showing 1584 Logic Cells and 108 I/O Pins

Ultra96 ZU3EG Device Gives You 145K Logic Cells and 82 I/O Pins
What can YOU do with Programmable Logic?
A REAL Example

From Dan Rozwood’s Linaro Connect Presentation

YVR18-303: Managing customized FPGA accelerators with SDSoC!

https://connect.linaro.org/resources/yvr18/sessions/yvr18-303/
What is going on behind the curtain?

Vivado Block Diagram Generated from Ultra96 SDSoC Platform by SDSoC Tools

Any VHDL or Verilog is Auto Generated!
Real Measurements

- Functional accelerator designs tested, one for 100 MHz clock and then 300 MHz clock

1024 cycles of 32x32 matrix multiply:
- Processor takes 1,578,611 clocks @ 1200MHz
- Logic takes 65,476 PS clocks @ 100MHz
- Logic takes 40,918 PS clocks @ 300MHz

Logic@100MHz: 24x increase
Logic@300MHz: 39x increase

100MHz → 300MHz: 1.6x increase
Moving Data Across Between Systems

- When Programmable Logic has a 3x faster clock, why not a 3x improvement in our calculation?
- Remember data moves INTO logic AND data moves OUT of logic
- 100 MHz AXI clock NOT adjusted for test
Acceleration limitations?

Yes, there are diminishing returns

- Due to losses in efficiency of parallelism as well as limitations on the slowest part, an ever increasing number of processing units is needed to increase speedup

Amdahl's law can be formulated in the following way:

\[ S_{\text{latency}}(s) = \frac{1}{(1 - p) + \frac{p}{s}} \]

where

- \( S_{\text{latency}} \) is the theoretical speedup of the execution of the whole task;
- \( s \) is the speedup of the part of the task that benefits from improved system resources;
- \( p \) is the proportion of execution time that the part benefiting from improved resources originally occupied.

Source: https://en.wikipedia.org/wiki/Amdahl%27s_law
Parallel Execution - Programmable Logic Shines!

• In the case of Programmable Logic
  • Break the computational problem up into the smallest pieces
  • Create a customized, dedicated accelerator
  • Provide resources specifically to handle the problem

• In the SDSoC created Programmable Logic solution for matrix multiply
  • The tool evaluated the resources we had at hand and provided enough resources to get us down to ~40 – 64 processor clocks for each matrix multiply!

• Programmable Logic implementation compared to processor only implementation:
  • Processor on average takes ~1542 PS clocks per matrix multiply
  • Hardware acceleration requires additional resources (including power) but Programmable Logic performance per Watt for some math intensive calculations can be much better than a standalone processor
Top 5
Ultra96 Developer Resources
Top 5 Ultra96 Developer Resources

1. Avnet Technical Training Courses (TTCs)  
   http://avnet.me/TTC

2. Adam Taylor Blogs and Projects  
   https://www.hackster.io/adam-taylor/projects

3. Ultra96 Documentation and Reference Designs on Element14  
   http://avnet.me/ultra96-community

4. Ultra96 Support Forums on Element14  
   http://avnet.me/ultra96-forums

5. Xilinx Community Portal  
   https://www.xilinx.com/community.html
Avnet Technical Training Courses (TTCs)
Ultra96 Training Courses

• **Intro Courses (1 day each)**
  - Developing Zynq UltraScale+ MPSoC Software
  - Developing Zynq UltraScale+ MPSoC Hardware
  - PetaLinux Tools for Ultra96 Development

• **Advanced Courses (2 days each)**
  - Practical Guide to Getting Started with Xilinx SDSoC
  - Turbocharge Python with Ultra96 PYNQ
  - Introduction to Deep Learning with Xilinx SoCs

* All courses will be based on 2018.3

http://avnet.me/TTC
Target Hardware - Intro + Advanced Courses

• **Base platform for all courses**
  - Ultra96 or Ultra96 V2
  - Delkin 16GB microSD card
  - JTAG/UART Pod
  - 2A or 4A power supply

• **Intro courses**
  - MikroElektronika Click Mezzanine
  - ST Micro LSM6DSL Click Board

• **PYNQ course**
  - TBD

• **Deep learning course**
  - USB web camera
Training Schedule

• Announcement April 2019

• Ultra96-V2 availability is required

• On-line courses on Hackster.io
  • Intro courses available at launch
  • Advanced courses in June

• Live courses in select cities
  • Starting in June
  • Taught by local or regional FAEs
  • Contact your local Avnet FAE for more info
Adam Taylor
Blogs and Projects
Adam Taylor History

Chartered Engineer and Fellow of the Institute of Engineering and Technology

MicroZed Chronicles – 2013 to Present
• Over 200 articles and tutorials published into two books:
  www.amazon.com/MicroZed-Chronicles-Using-Zynq-101-ebook/dp/B015BJW0NO/

Ultra96 Blogs and Projects
• New materials posted weekly on Hackster.io community site

http://avnet.me/adam-taylor
Blogs and Projects

Currently over 20 Xilinx Programmable Logic related projects with easy-to-follow instructions

http://avnet.me/adam-taylor
Source Code

Adam makes his project source code Public on Github
Ultra96 Documentation and Reference Designs on Element14
Ultra96

Ultra96™ is an Arm-based, Xilinx Zynq UltraScale+™ MPSoC development board based on the Linaro 96Boards specification. The 96Boards' specifications are open and define a standard board layout for development platforms that can be used by software application, hardware device, kernel, and other system software developers. Ultra96 represents a unique position in the 96Boards community with a wide range of potential peripherals and acceleration engines in the programmable logic that is not available from other offerings. Ultra96 boots from the provided Delkin 16 GB MicroSD card, pre-loaded with PetaLinux. Engineers have options of connecting to Ultra96 through a Webserver using integrated wireless access point capability or to use the provided PetaLinux desktop environment which can be viewed on the integrated Mini DisplayPort video output. Multiple application examples and on-board development options are provided as examples.

Ultra96 provides four user-controllable LEDs. Engineers may also interact with the board through the 96Boards-compatible low-speed and high-speed expansion connectors by adding peripheral accessories such as those included in Seeed Studio’s Grove Starter Kit for 96Boards.

Micron LPDDR4 memory provides 2 GB of RAM in a 512M x 32 configuration. Wireless options include 802.11b/g/n Wi-Fi and Bluetooth 4.2 (provides both Bluetooth Classic and Low Energy (BLE)). UARTs are accessible on a header as well as through the expansion connector. JTAG is available through a header (external USB-JTAG required), I2C is available through the expansion connector.

Ultra96 provides one upstream (device) and two downstream (host) USB 3.0 connections. A USB 2.0 downstream (host) interface is provided on the high speed expansion bus. Two Microchip USB3320 USB 2.0 ULPI Transceivers and one Microchip USB5744 4-Port S3H13 USB Controller Hub are specified.

The integrated power supply generates all on-board voltages from an external 12V supply (available as an accessory).

Features
- Xilinx Zynq UltraScale+ MPSoC ZU9EG SBVA404
- Micron 2 GB (512M x 32) LPDDR4 Memory
- Delkin 16 GB MicroSD card + adapter
  - Pre-loaded with PetaLinux environment
- Wi-Fi / Bluetooth
- Mini DisplayPort (MiniDP or mDP)
- 1x USB 3.0 Type Micro-B upstream port
- 2x USB 2.0, 1x USB 2.0 Type A downstream ports
- 40-pin 96Boards Low-speed expansion header
- 60-pin 96Boards High speed expansion header
- 85mm x 54mm form factor
- Linaro 96Boards Consumer Edition compatible
All Avnet published documents for Ultra96

- Hardware User Guide
- Schematics
- Bill of Materials
- PCB Layout
- Net Length Report
- Getting Started Guide
- Assembly Drawing
- Drill Drawing
- 3D Step Model
- Board Definition Files
- XDC Pin Contraints
Reference Designs for Ultra96

- Factory SD Card Image
- SDSoc Platforms
- Base Technical Reference Design
- PYNQ Framework
- Basic Tutorials
- PetaLinux BSPs
- Many more coming soon…
Ultra96 Support Forums on Element14
Ultra96 Support Forums

Forums monitored by thousands of members of Element14 community

- Avnet engineers from my group answer member questions here

http://avnet.me/ultra96-forums

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**Forums**

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<td>Zynq Mini-ITX Hardware Design Forum</td>
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<tr>
<td>Zynq Mini-Module Plus (MMP) Hardware Design Forum</td>
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Xilinx Community Portal
Xilinx Community Portal

www.xilinx.com/community.html

Community based resources focused on Xilinx technology

• Projects – Including Ultra96
• Open Source
• Forums
• Wiki
• Github
• XUP
• AWS
• Videos
• Events

Welcome to Xilinx Community Portal

This is a Community page focusing on Xilinx technology. There will be designs and information shared from the community at large, including you, Xilinx and Xilinx’s partners. Feel free to browse, use the information, and add your own design.
Ultra96 V2
What is Ultra96-V2?

- $249 Single Board Computer (SBC)
  - Based on Xilinx Zynq UltraScale+
  - Replaces Ultra96

- Designed to 96Boards.org standard form-factor
  - Consumer Edition

- Applications
  - Artificial intelligence
  - Machine learning
  - Embedded processing
  - Robotics
Ultra96-V2 Kit Overview

- What’s included
  - Ultra96-V2 board
  - 16 GB MicroSD card
  - SDSoC license voucher
  - Quick start card
- Part number: AES-ULTRA96-V2-G
- Availability
  - Order entry available now
  - Board Definition on Github now
  - Boards available end of April
- Additional information available now
  - www.ultra96.org
  - www.96boards.org
What is Different: Ultra96 V2 vs V1

Ultra96-V2 has:
- Infineon power (not TI)
- Microchip Wi-Fi / Bluetooth (not TI)
- Micron memory upgraded to latest -053 (single-die)
- IDT clock chip (not SiLabs)
- Abracon crystal, Microchip oscillator
- Dialog On/Off controller (not ADI)
- TI SD Card controller (to save cost)
- TE and Molex connectors (not Wurth, Alps)
- All I-grade component options
  - Exception SD Card cage and barrel jack
### Microchip ATWILC3000 Pre-Certified Countries

- Algeria
- Argentina
- Armenia
- Aruba
- Australia
- Azerbaijan
- Bahamas
- Bahrain
- Belarus
- Benin
- Bolivia
- Botswana
- Brazil
- Cambodia
- Cameroon
- Canada
- Chile
- China
- Colombia
- Congo
- Costa Rica
- Cote D'ivoire
- Dominican Republic
- Ecuador
- Egypt
- EU
- Fiji
- Ghana
- Grenada
- Honduras
- India
- Israel
- Jamaica
- Japan
- Jordan
- Kenya
- Kuwait
- Lebanon
- Lesotho
- Madagascar
- Malawi
- Mauritius
- Mexico
- Moldova
- Morocco
- Mozambique
- Namibia
- Nepal
- New Zealand
- Nicaragua
- Nigeria
- Oman
- Pakistan
- Panama
- Papua New Guinea
- Paraguay
- Peru
- Qatar
- Russia
- Saudi Arabia
- Senegal
- Singapore
- South Africa
- South Korea
- Swaziland
- Taiwan
- Tanzania
- Thailand
- UAE (United Arab Emirates)
- Uganda
- Ukraine
- Uruguay
- USA
- Venezuela
- Zambia
- Zimbabwe
Almost There
Ultra96 - Xilinx Programmable Logic Advantage

Lower total cost of ownership with reconfigurable/renewable hardware
• Extend the life of your product with remote hardware upgrades, hardware bug fixes, and add additional hardware features with dynamic reconfiguration
• Reduce maintenance costs by eliminating deployment of repair technicians

Lowest cost custom hardware option for low-volume to medium-volume production
• Extensive IP library provided by Xilinx, majority of IP cores are provided for free
• Tools to quickly develop and protect your own custom Programmable Logic IP
• Xilinx IPs standardized on AXI which is an open ARM AMBA standard

Ready to Use Segment Solutions
• Differentiate your product faster
• Automotive, A&D, broadcast & pro A/V, consumer electronics, data center, emulation & prototyping, high performance computing, industrial, medical, test & measurement, wired and wireless communications
Summary

Still some hurdles along the way…
• Although you can make your hardware IP source code open source, the Xilinx EDA tools are not open source
• Co-processor and hardware accelerator design requires both hardware and software skills to achieve exceptional results

In the end, it is worth the effort!!!
• You have something custom that differentiates you from all your competitors and it is hard for them to catch up to you
• You get the exact hardware peripheral set that you need for your ARM based application
• Secure the smart hardware (your own Intellectual Property) deeply within the fabric of your next design
• Future proof your design by enabling you to update some of your hardware through just a downloadable update
Path to Programmable is an Element14 training project, NOT a Design Challenge
• Requirement to take training, start a new project, and blog your work on Element14
• Past graduates received some very useful design material and troubleshooting tools

Designing with Xilinx® FPGAs: Using Vivado
FLUKE 3000 FC - Wireless Digital Multimeter
Pro's Kit Electronic Tool Kit

Enrollment starts Summer 2019

http://avnet.me/path-to-programmable
Acknowledgements

Thank you to the following people for the knowledge, wisdom, and encouragement to put this course together in pursuit of a more hardware accelerated world:

- Thomas Keryk – Retired Electronics Engineer
- Ron Wright – Retired Software Engineer
- Adam Taylor – Electronics Engineer, ADIUVO Engineering
- Dan Rozwood – Electronics Engineer, Avnet
- Bryan Fletcher – Electronics Engineer, Avnet
Co-Processing History