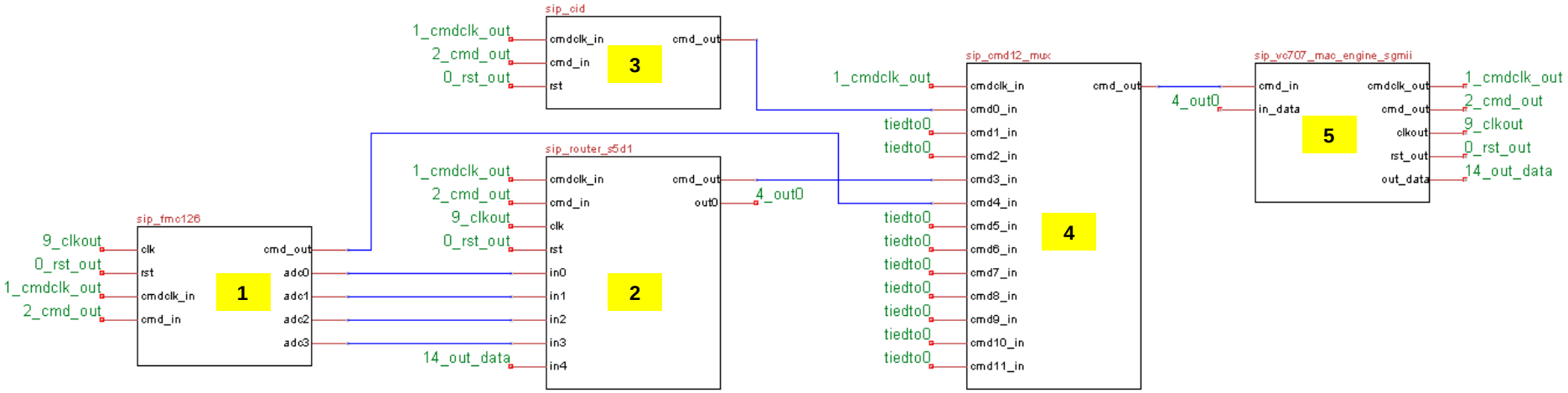
2015.01.05 ESSAI MODIF INDEX



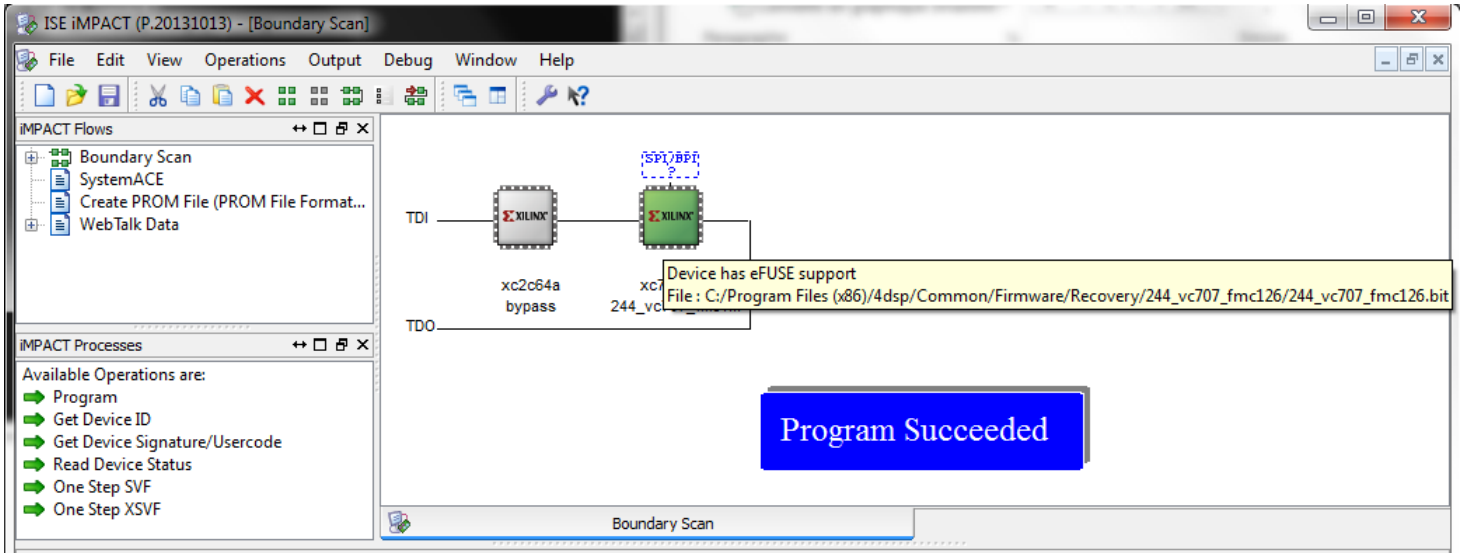
FICHIER XML D'ORIGINE

```
<?xml version="1.0" encoding="UTF-8"?>
<library>

  <wormholes>

    <sip_router_s5d1>cmdclk_in:cmdclk_in|cmd_in:cmd_in|cmd_out:cmd_out|clk:clkin|rst:rst_in|out0:wh_out|in0:
    wh_in|in1:wh_in|in2:wh_in|in3:wh_in|in4:wh_in|generic:generic_def</sip_router_s5d1>

    <sip_cid>cmdclk_in:cmdclk_in|cmd_in:cmd_in|rst:rst_in|cmd_out:cmd_out|generic:generic_def</sip_cid>

    <sip_cmd12_mux>cmdclk_in:cmdclk_in|cmd0_in:cmd_in|cmd1_in:cmd_in|cmd2_in:cmd_in|cmd3_in:cmd_in|cmd4_in:c
    md_in|cmd5_in:cmd_in|cmd6_in:cmd_in|cmd7_in:cmd_in|cmd8_in:cmd_in|cmd9_in:cmd_in|cmd10_in:cmd_in|cmd11_i
    n:cmd_in|cmd_out:cmd_out</sip_cmd12_mux>

    <sip_fmc126>clk:clkin|rst:rst_in|cmdclk_in:cmdclk_in|cmd_in:cmd_in|cmd_out:cmd_out|adc0:wh_out|adc1:wh_o
    ut|adc2:wh_out|adc3:wh_out|ext_i2c:ext_i2c|ext_fmc126:ext_fmc126|generic:generic_def</sip_fmc126>

    <sip_vc707_mac_engine_sgmii>cmdclk_out:cmdclk_out|cmd_out:cmd_out|cmd_in:cmd_in|clkout:clkout|rst_out:rs
    t_out|ext_mac_engine_sgmii:ext_mac_engine_sgmii|in_data:wh_in|out_data:wh_out</sip_vc707_mac_engine_sgmi
    i>

  <memmap>

        <sip_router_s5d1>nbr_registers:2</sip_router_s5d1>
        <sip_cid>nbr_registers:8</sip_cid>
        <sip_cmd12_mux>nbr_registers:0</sip_cmd12_mux>
        <sip_fmc126>nbr_registers:131072</sip_fmc126>
        <sip_vc707_mac_engine_sgmii>nbr_registers:0</sip_vc707_mac_engine_sgmii>

</memmap>

  <whattributes>
  </whattributes>

</library>
```

2015.01.05 ESSAI MODIF INDEX

Fichier .bit du BSP

Programmation du FPGA (version index = 0)



2015.01.05 ESSAI MODIF INDEX

Fichier .bit du BSP

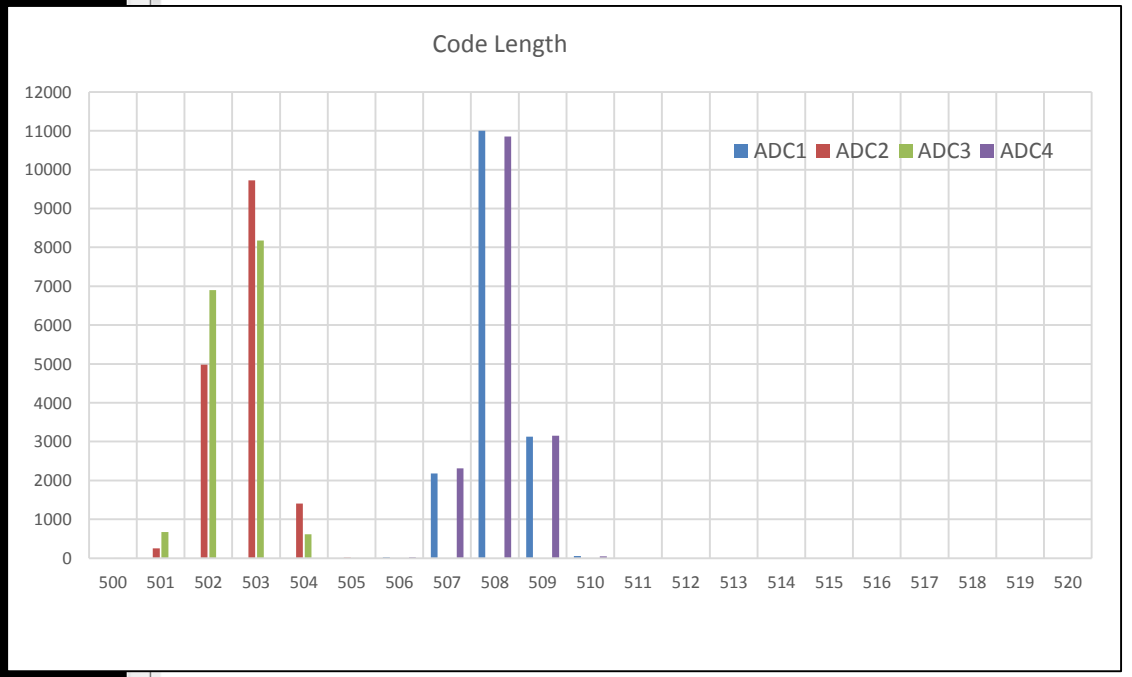
Lancement de l'exe Fmc12cAPP.exe

```
C:\Program Files (x86)\4dsp\FMC Board Support Package\Bins>Fmc12xAPP.exe 1 VC707 0 0 0
```

```
C:\windows\system32\cmd.exe - Fmc12xAPP.exe 1 VC707 0 0 0
(vco type) can be 0 (2500MHz default), 1 (2200MHz option), 2 (2000MHz option),
3 (1600 MHz option), 4 (Internal VCO option -C60)

 List of NDIS interfaces found in the system (device index):
 -----------------------------------------------------------
 Number of devices found : 1
  0. \Device\NPF_{747204A1-4A67-4A74-9C6A-73B142E35ADA}
     - Broadcom NetXtreme Gigabit Ethernet Driver

C:\Program Files (x86)\4dsp\FMC Board Support Package\Bins>Fmc12xAPP.exe 1 VC707
 0 0 0
 Number of devices found : 1
  0. \Device\NPF_{747204A1-4A67-4A74-9C6A-73B142E35ADA}
     - Broadcom NetXtreme Gigabit Ethernet Driver


Connected FPGA Device Type: XC7VX485T

Start of program
-------------------------------------
Constellation ID : 244
Number of Stars  : 5
Software Build   : 0x5074C736
Firmware Build   : 0x00000000
Firmware Version : 0.1
-------------------------------------

Found FMC126-VC707 hardware (Ethernet Firmware)


-------- Onboard Monitoring ---------
IIC Mon Dev ID  : OK (0x02)
IIC Man Dev ID  : OK (0x41)
IIC Mon Sil Rev : OK (0x05)
TEMP (  ADT   ) : OK (41.25C)
TEMP (  ADC   ) : OK (70.25C)
VDD  ( 3.3V   ) : OK ( 3.29V)
AIN3 ( VADJ   ) : OK ( 1.80V)
AIN4 ( 2.5Vclk) : OK ( 2.46V)
AIN5 ( 3.3Vdig) : OK ( 3.26V)
AIN6 ( 3.3Vadc) : OK ( 3.16V)
AIN7 ( 5.0Vcp ) : OK ( 0.00V)
AIN8 ( 1.8V   ) : OK ( 1.76V)
-------------------------------------


--------- Configuring FMC12x ----------
PLL locked!!!
Training status : Ready
Active channels : A B C D
Pattern check   : 3 seconds | ADC0: 0 | ADC1: 0 | ADC2: 0 | ADC3: 0
-------------------------------------
IDELAY Ch 0: 20 | 20 | 20 | 20 | 19 | 19 | 20 | 19 | 16 | 17 | 15
IDELAY Ch 1: 13 | 14 | 13 | 13 | 13 | 13 | 14 | 14 | 13 | 13 |  8
IDELAY Ch 2: 16 | 17 | 17 | 16 | 17 | 17 | 17 | 18 | 18 | 19 |  7
IDELAY Ch 3: 12 | 11 | 11 | 12 | 11 | 11 | 11 | 11 |  9 | 10 |  8
-------------------------------------


--- Measuring on-board frequencies ---
Stellar IP Clock  : 125.00 MHz
ADC A PHY Clock   : 156.25 MHz (Fs = 1250.00)
ADC B PHY Clock   : 156.23 MHz (Fs = 1249.88)
ADC C PHY Clock   : 156.23 MHz (Fs = 1249.88)
ADC D PHY Clock   : 156.23 MHz (Fs = 1249.88)
External Trigger  :   0.02 MHz
Clock Src Monitor : 312.48 MHz (Fc = 2499.88)
-------------------------------------

Running ramp pattern check on channel 0 and card 0......   Passed!
Acquiring 16384 samples on channel 0, card 0
Running ramp pattern check on channel 1 and card 0......   Passed!
Acquiring 16384 samples on channel 1, card 0
Running ramp pattern check on channel 2 and card 0......   Passed!
Acquiring 16384 samples on channel 2, card 0
Running ramp pattern check on channel 3 and card 0......   Passed!
Acquiring 16384 samples on channel 3, card 0

End of program.


Appuyez sur une touche pour continuer...
```

Ordinateur ▸ OSDisk (C:) ▸ Program Files (x86) ▸ 4dsp ▸ FMC Board Support Package ▸ Bins

Nom	Modifié le	Type	Taille
Fmc12xAPP.exe	13/06/2014 12:43	Application	29 Ko
adc0.txt	05/01/2015 10:19	Document texte	80 Ko
adc1.txt	05/01/2015 10:19	Document texte	80 Ko
adc2.txt	05/01/2015 10:19	Document texte	80 Ko
adc3.txt	05/01/2015 10:19	Document texte	80 Ko
EthAPI.dll	27/06/2014 10:25	Extension de l'app...	110 Ko
2011211-FMC126_HPC1.xlsx	11/12/2014 15:27	Feuille de calcul ...	522 Ko
adc0.bin	05/01/2015 10:19	Fichier BIN	32 Ko
adc1.bin	05/01/2015 10:19	Fichier BIN	32 Ko
adc2.bin	05/01/2015 10:19	Fichier BIN	32 Ko
adc3.bin	05/01/2015 10:19	Fichier BIN	32 Ko

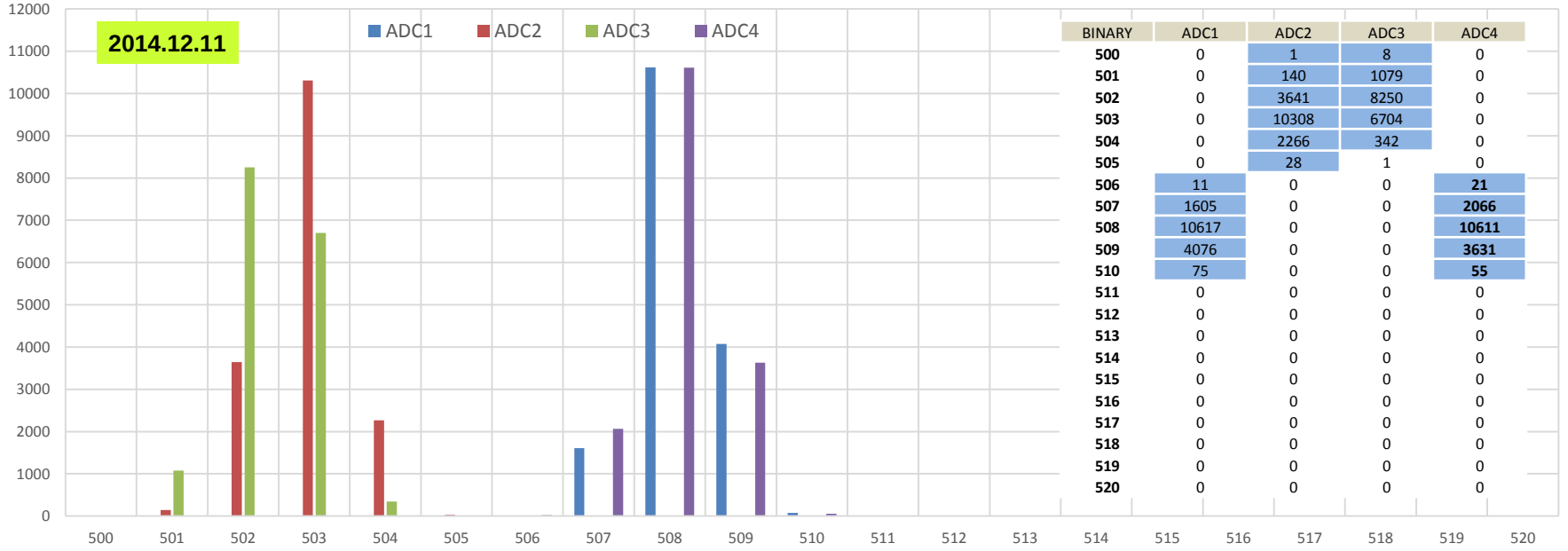


2015.01.05 ESSAI MODIF INDEX

Fichier .bit du BSP

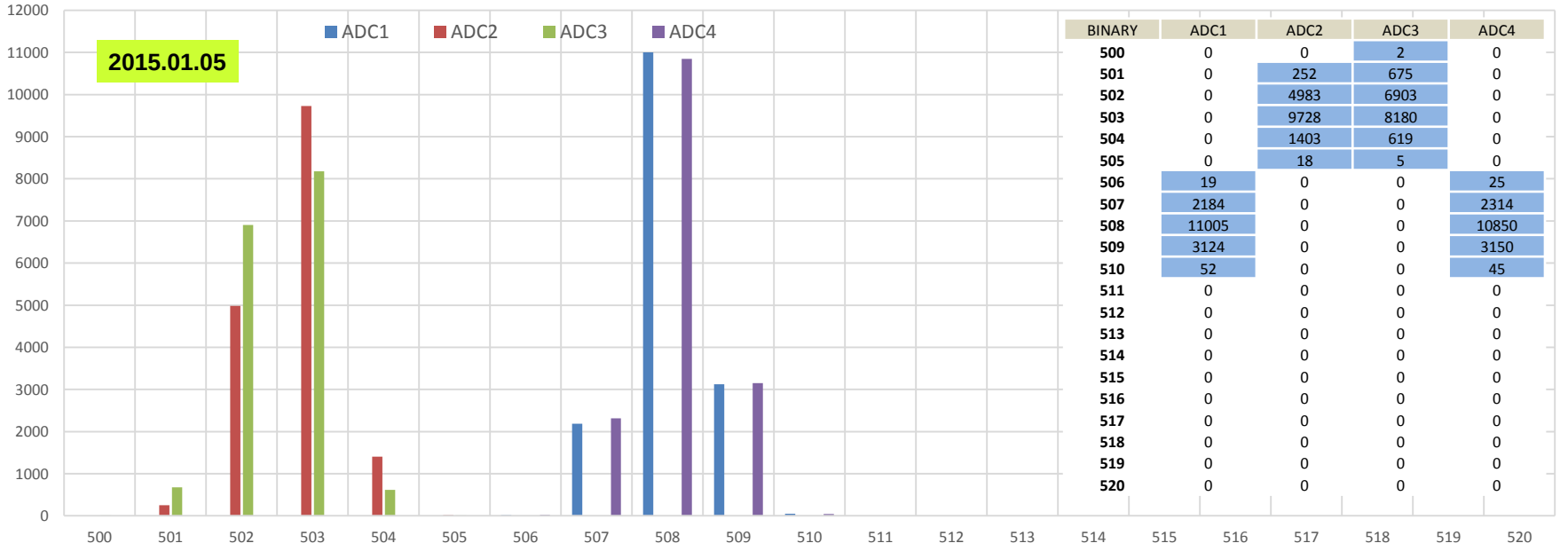
Lancement de l'exe Fmc12cAPP.exe

2014.12.11



BINARY	ADC1	ADC2	ADC3	ADC4
500	0	1	8	0
501	0	140	1079	0
502	0	3641	8250	0
503	0	10308	6704	0
504	0	2266	342	0
505	0	28	1	0
506	11	0	0	21
507	1605	0	0	2066
508	10617	0	0	10611
509	4076	0	0	3631
510	75	0	0	55
511	0	0	0	0
512	0	0	0	0
513	0	0	0	0
514	0	0	0	0
515	0	0	0	0
516	0	0	0	0
517	0	0	0	0
518	0	0	0	0
519	0	0	0	0
520	0	0	0	0

2015.01.05



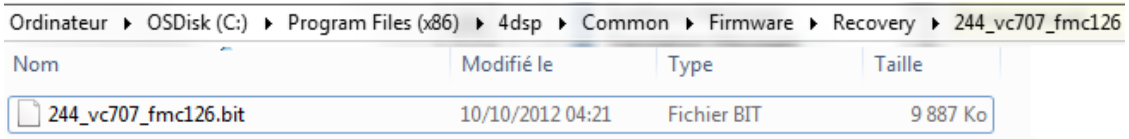
BINARY	ADC1	ADC2	ADC3	ADC4
500	0	0	2	0
501	0	252	675	0
502	0	4983	6903	0
503	0	9728	8180	0
504	0	1403	619	0
505	0	18	5	0
506	19	0	0	25
507	2184	0	0	2314
508	11005	0	0	10850
509	3124	0	0	3150
510	52	0	0	45
511	0	0	0	0
512	0	0	0	0
513	0	0	0	0
514	0	0	0	0
515	0	0	0	0
516	0	0	0	0
517	0	0	0	0
518	0	0	0	0
519	0	0	0	0
520	0	0	0	0

2015.01.05 ESSAI MODIF INDEX

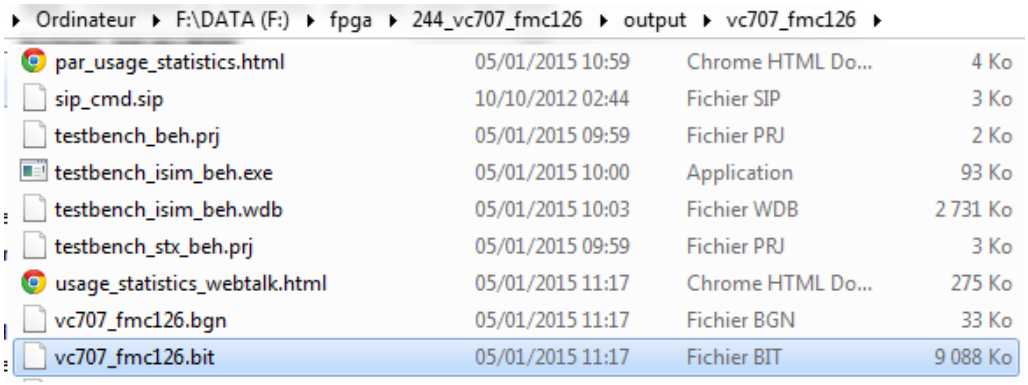
Synthèse avec ISE 14.7 de la constellation d'origine Index=0 (slot HPC#1)

But : comparer le nouveau .bit avec celui du BSP

Fichier .bit du BSP



Nouveau .bit



2015.01.05 ESSAI MODIF INDEX

Synthèse avec ISE 14.7 de la constellation d'origine Index=0 (slot HPC#1)

Fichier .bit du BSP

C:\Program Files (x86)\4dsp\Common\Firmware\Recovery\244_vc707_fmc126\244_vc707_fmc126.bit

```
C:\Program Files (x86)\4dsp\FMC Board Support Package\Bins>Fmc12xAPP.exe 1 VC707
 0 0 0
 Number of devices found : 1
  0. \Device\NPF_{747204A1-4A67-4A74-9C6A-73B142E35ADA}
     - Broadcom NetXtreme Gigabit Ethernet Driver


Connected FPGA Device Type: XC7VX485T

Start of program
-------------------------------------
Constellation ID : 244
Number of Stars  : 5
Software Build   : 0x5074C736
Firmware Build   : 0x00000000
Firmware Version : 0.1
-------------------------------------

Found FMC126-VC707 hardware (Ethernet Firmware)


-------- Onboard Monitoring ---------
IIC Mon Dev ID  : OK (0x02)
IIC Man Dev ID  : OK (0x41)
IIC Mon Sil Rev : OK (0x05)
TEMP (  ADT   ) : OK (41.25C)
TEMP (  ADC   ) : OK (70.25C)
VDD  ( 3.3V   ) : OK ( 3.29V)
AIN3 ( VADJ   ) : OK ( 1.80V)
AIN4 ( 2.5Vclk) : OK ( 2.46V)
AIN5 ( 3.3Vdig) : OK ( 3.26V)
AIN6 ( 3.3Vadc) : OK ( 3.16V)
AIN7 ( 5.0Vcp ) : OK ( 0.00V)
AIN8 ( 1.8V   ) : OK ( 1.76V)
-------------------------------------


--------- Configuring FMC12x ----------
PLL locked!!!
Training status : Ready
Active channels : A B C D
Pattern check   : 3 seconds | ADC0: 0 | ADC1: 0 | ADC2: 0 | ADC3: 0
-------------------------------------
IDELAY Ch 0: 20 | 20 | 20 | 20 | 19 | 19 | 20 | 19 | 16 | 17 | 15
IDELAY Ch 1: 13 | 14 | 13 | 13 | 13 | 14 | 14 | 13 | 13 |  8
IDELAY Ch 2: 16 | 17 | 17 | 16 | 17 | 17 | 17 | 18 | 18 | 19 |  7
IDELAY Ch 3: 12 | 11 | 11 | 12 | 11 | 11 | 11 | 11 |  9 | 10 |  8
-------------------------------------


--- Measuring on-board frequencies ---
Stellar IP Clock  : 125.00 MHz
ADC A PHY Clock   : 156.25 MHz (Fs = 1250.00)
ADC B PHY Clock   : 156.23 MHz (Fs = 1249.88)
ADC C PHY Clock   : 156.23 MHz (Fs = 1249.88)
ADC D PHY Clock   : 156.23 MHz (Fs = 1249.88)
External Trigger  :   0.02 MHz
Clock Src Monitor : 312.48 MHz (Fc = 2499.88)
-------------------------------------

Running ramp pattern check on channel 0 and card 0......   Passed!
Acquiring 16384 samples on channel 0, card 0
Running ramp pattern check on channel 1 and card 0......   Passed!
Acquiring 16384 samples on channel 1, card 0
Running ramp pattern check on channel 2 and card 0......   Passed!
Acquiring 16384 samples on channel 2, card 0
Running ramp pattern check on channel 3 and card 0......   Passed!
Acquiring 16384 samples on channel 3, card 0

End of program.
```

INDEX = 0

FMC126 Slot HPC1

Nouveau .bit

F:\fpga\244_vc707_fmc126\output\vc707_fmc126\vc707_fmc126.bit

```
C:\Program Files (x86)\4dsp\FMC Board Support Package\Bins>Fmc12xAPP.exe 1 VC707
 0 0 0
 Number of devices found : 1
  0. \Device\NPF_{747204A1-4A67-4A74-9C6A-73B142E35ADA}
     - Broadcom NetXtreme Gigabit Ethernet Driver


Connected FPGA Device Type: XC7VX485T

Start of program
-------------------------------------
Constellation ID : 244
Number of Stars  : 5
Software Build   : 0x54AA459D modifié
Firmware Build   : 0x00000000
Firmware Version : 0.1
-------------------------------------

Found FMC126-VC707 hardware (Ethernet Firmware)


-------- Onboard Monitoring ---------
IIC Mon Dev ID  : OK (0x02)
IIC Man Dev ID  : OK (0x41)
IIC Mon Sil Rev : OK (0x05)
TEMP (  ADT   ) : OK (44.25C)
TEMP (  ADC   ) : OK (72.25C)
VDD  ( 3.3V   ) : OK ( 3.29V)
AIN3 ( VADJ   ) : OK ( 1.80V)
AIN4 ( 2.5Vclk) : OK ( 2.48V)
AIN5 ( 3.3Vdig) : OK ( 3.24V)
AIN6 ( 3.3Vadc) : OK ( 3.16V)
AIN7 ( 5.0Vcp ) : OK ( 4.91V)
AIN8 ( 1.8V   ) : OK ( 1.76V)
-------------------------------------


--------- Configuring FMC12x ----------
PLL locked!!!
Training status : Ready
Active channels : A B C D
Pattern check   : 3 seconds | ADC0: 0 | ADC1: 0 | ADC2: 0 | ADC3: 0
-------------------------------------
IDELAY Ch 0: 20 | 20 | 20 | 20 | 19 | 19 | 20 | 19 | 16 | 17 | 15
IDELAY Ch 1: 13 | 14 | 13 | 13 | 13 | 14 | 14 | 13 | 14 |  8
IDELAY Ch 2: 16 | 17 | 18 | 17 | 17 | 17 | 18 | 18 | 18 | 19 |  8
IDELAY Ch 3: 12 | 11 | 11 | 12 | 11 | 12 | 11 | 11 |  9 | 10 |  8
-------------------------------------


--- Measuring on-board frequencies ---
Stellar IP Clock  : 125.00 MHz
ADC A PHY Clock   : 156.25 MHz (Fs = 1250.00)
ADC B PHY Clock   : 156.25 MHz (Fs = 1250.00)
ADC C PHY Clock   : 156.23 MHz (Fs = 1249.88)
ADC D PHY Clock   : 156.23 MHz (Fs = 1249.88)
External Trigger  :   0.02 MHz
Clock Src Monitor : 312.48 MHz (Fc = 2499.88)
-------------------------------------

Running ramp pattern check on channel 0 and card 0......   Passed!
Acquiring 16384 samples on channel 0, card 0
Running ramp pattern check on channel 1 and card 0......   Passed!
Acquiring 16384 samples on channel 1, card 0
Running ramp pattern check on channel 2 and card 0......   Passed!
Acquiring 16384 samples on channel 2, card 0
Running ramp pattern check on channel 3 and card 0......   Passed!
Acquiring 16384 samples on channel 3, card 0

End of program.
```

INDEX = 0 no change

FMC126 Slot HPC1