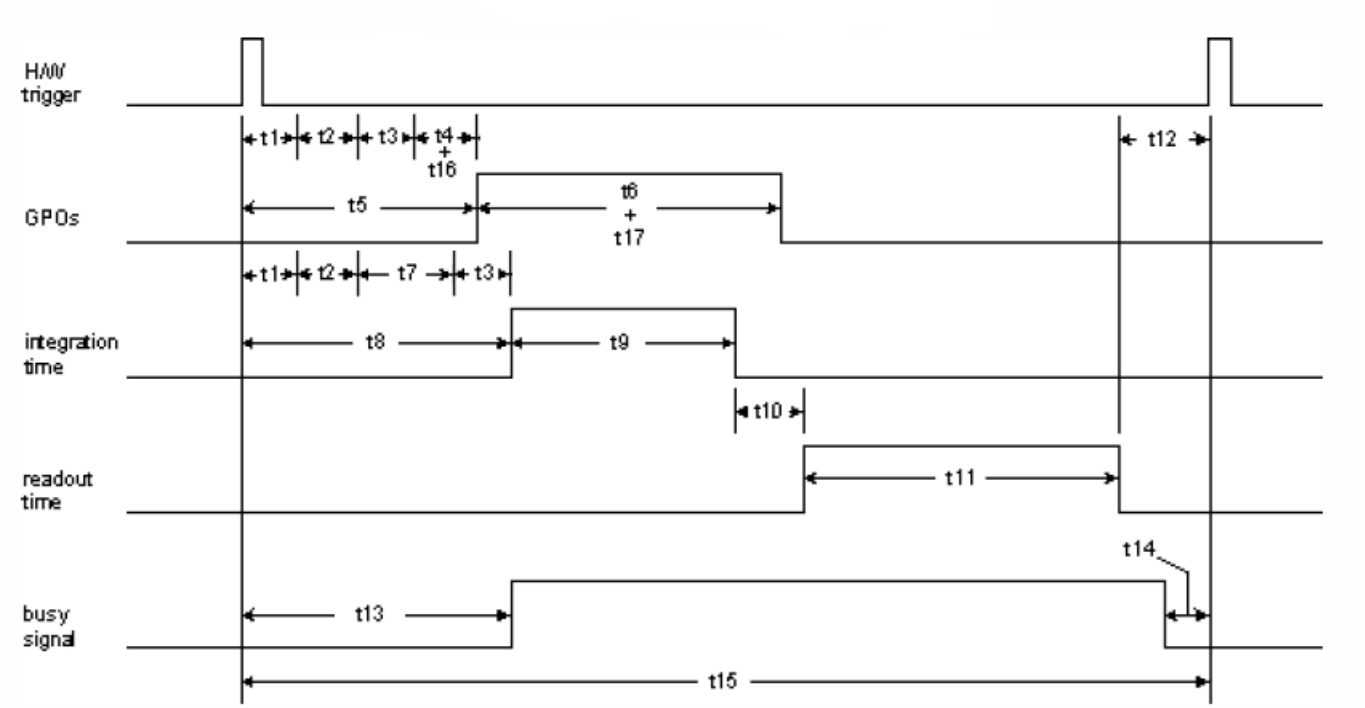
Normal Trigger Pulses



Picture 1. Timing diagram for normal trigger pulses.

Table 1.1 Signal Information

Signal	Description	Min	Typ	Max
t1	Board Level hardware propagation delay (3.3V HCMOS to trigger)		10 ns	
	Enclosed hardware propagation delay (5V to trigger optocoupler)		8 us ON 30 us OFF (Note 1)	
	Enclosed hardware propagation delay (12V to trigger optocoupler)		2.5 us ON 40 us OFF (Note 1)	
t2	Debounce time		1.0 us	
t3	1H period	0.0 us	varies between Min and Max	See Table 1.2
t4	Programmable GPO delay	0.0 us	in 10 us steps	2.5 sec
t5	Start of trigger to start of GPO (t1 + t2 + t3 + t4 + t16)			
t6	Programmable GPO time	10.0 us	in 10 us steps	2.5 sec
t7	Trigger mode 14 Programmable integration delay (Note 2)	0.0 us	in 10 us steps	2.5 sec
t8	Start of trigger to start of integration (t1 + t2 + t7 + t3)		(Note 3)	
t9	Integration time		See Integration Times	
t10	End of integration to start of read out		See Table 1.3	
t11	Read out time		See Readout Times	
t12	End of read out to start of trigger	$t14 + t3_{Max}$	t15 - t8 - t9 - t10 - t11	
t13	Start of trigger to start of busy		t1 + t2 + t3	
t14	End of busy to start of trigger	30.0 ns	$t15 - t8 - t9 - t10 - t11 - t3_{Max}$	
t15	Frame period		t8 + t9 + t10 + t11 + t12	
t16 & t17	Board Level hardware propagation delay (3.3V HCMOS From GPO)		20 ns	
	Enclosed hardware propagation delay (GPO optocoupler with 1K pullup to 5V)		3 us ON 70 us OFF (Note 1)	

Note:
1. “ON” refers to current flowing through the optocoupler and “OFF” refers to no current flowing through the optocoupler. Refer to interface schematics.
2. For minimum hardware trigger, the programmable integration delay (t7) should be set to 0 (minimum).
3. For a software trigger, t8 = 1.7 ms typical.

Table 1.2 Maximum of 1H period for PL-D cameras with Sony sensors

PL-D camera with Sony sensor	For 8-bit output in (us)	For 12-bit output in (us)
PL-D752	4.8480	6.2220
PL-D753	4.5522	5.3872
PL-D755	5.9259	6.9899
PL-D755MU-POL	5.9259	6.9899
PL-D757	7.2188	8.6195
PL-D759	9.4270	11.191
PL-D7512	9.4270	11.191
PL-D795	n/a	13.414
PL-D797	n/a	16.755
PL-D799	n/a	14.020
PL-D7912	n/a	14.020

Table 1.3 End of integration to start of read out

PL-D camera with Sony sensor	For 8-bit output in (us)		For 12-bit output in (us)	
	Normal	FFR*	Normal	FFR*
PL-D752	261.80	184.23	336.00	236.44
PL-D753	236.72	200.30	280.14	237.04
PL-D755	272.60	225.19	321.54	265.62
PL-D755MU-POL	272.60	225.19	321.54	265.62
PL-D757	375.38	317.63	448.22	379.26
PL-D759	659.90	509.06	783.37	604.32
PL-D7512	584.48	509.06	693.85	604.32
PL-D795	536.56	429.25	536.56	429.25
PL-D797	310.30	241.35	310.30	241.35
PL-D799	701.01	476.69	701.01	476.69
PL-D7912	588.85	476.69	588.85	476.69

*where: FFR is the Fixed Frame Rate mode.

Sequential Trigger Pulses (High FPS)

Sony sensors support Sequential Trigger mode or in other words they can be triggered with sequential trigger pulses. See the timing diagram below. In order to achieve the maximum frame rate for these cameras when using sequential trigger pulses, they must meet the following timing requirements

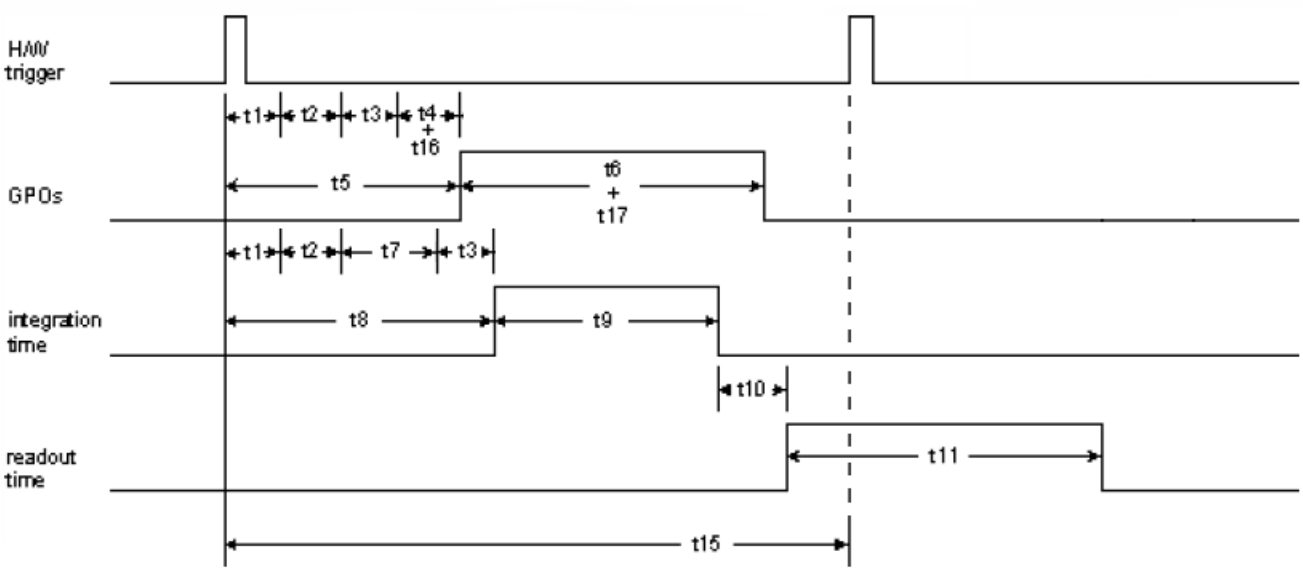
Timing requirements:

1. $t15 \geq t18$

2. $t15 \geq t19 + t1 + t2 + t3_{Max} + t9$

where: t18 is the time of the rising edge prohibited region (Table 1.4) and t19 is the time of the falling edge prohibited region (Table 1.5). See Table 1.1 for t1, t2, t3, and t9.

Note: If sequential trigger pulses do not meet these requirements, they get ignored and the cameras output a lower frame rate. Usually, it is half of the targeted frame rate.



Picture 2. Timing diagram for sequential trigger pulses.

Table 1.4 Rising edge prohibited region (t18)

PL-D camera with Sony sensor	For 8-bit output in (us)		For 12-bit output in (us)	
	Normal	FFR*	Normal	FFR*
PL-D752	6079.40	t11* + 184.23	7802.40	t11* + 236.44
PL-D753	6992.18	t11* + 291.35	8253.20	t11* + 323.24
PL-D755	12408.83	t11* + 225.19	14636.85	t11* + 265.62
PL-D755MU-POL	12408.83	t11* + 225.19	14636.85	t11* + 265.62
PL-D757	16458.86	t11* + 519.76	19617.98	t11* + 586.13
PL-D759	21003.36	t11* + 509.06	24933.55	t11* + 604.32
PL-D7512	28846.62	t11* + 509.06	34244.46	t11* + 604.32
PL-D795	n/a	n/a	28062.10	t11* + 429.25
PL-D797	n/a	n/a	37665.24	t11* + 670.20
PL-D799	n/a	n/a	30956.16	t11* + 476.68
PL-D7912	n/a	n/a	42732.96	t11* + 476.68

*where: FFR is the Fixed Frame Rate mode and t11 is the read out time from Table 1.1.

Table 1.5 Falling edge prohibited region (t19)

PL-D camera with Sony sensor	For 8-bit output in (us)	For 12-bit output in (us)
PL-D752	67.88	87.11
PL-D753	81.94	75.42
PL-D755	82.97	97.86
PL-D755MU-POL	82.97	97.86
PL-D757	158.82	155.15
PL-D759	226.25	268.59
PL-D7512	226.25	268.59
PL-D795	160.97	160.97
PL-D797	160.97	160.97
PL-D799	160.97	160.97
PL-D7912	168.24	168.24