LYNXTechnik **AG**®

Broadcast Television Equipment

Application Note

PVD - Total Delay and Fixed Processing Time

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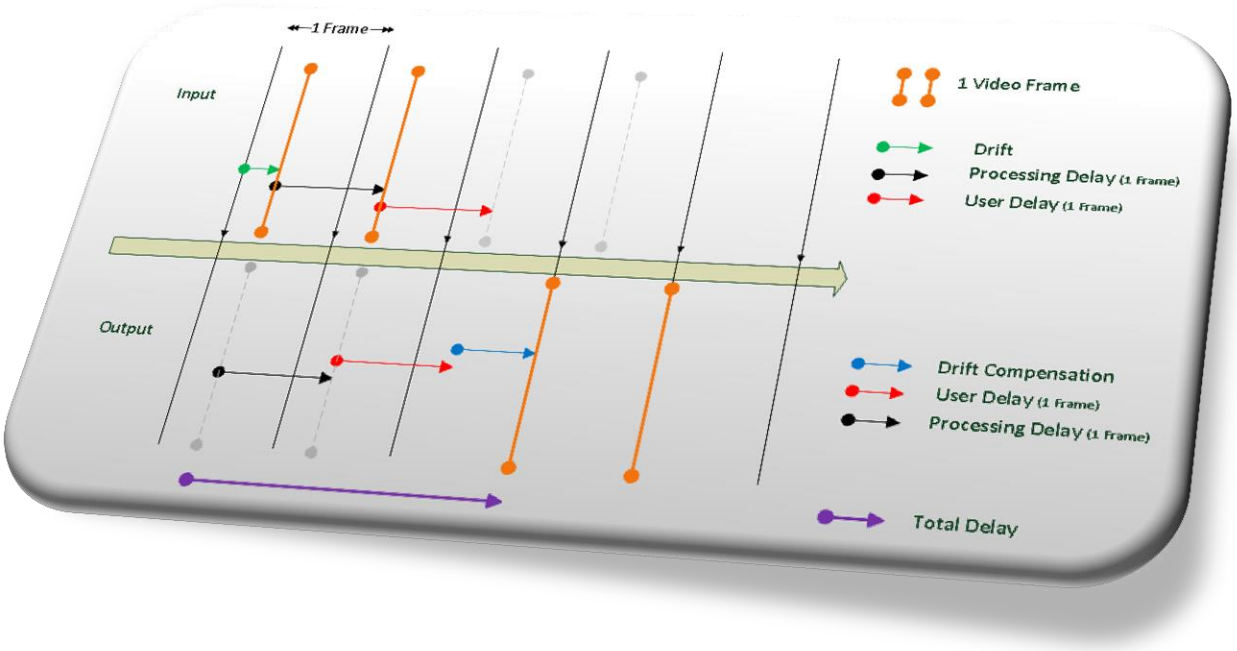

Contents

1 Total delay consists of which parts?

Total Delay = Processing Delay + User Delay + Drift Compensation

The Total Delay value in the APPolo Control GUI is displayed in the video timing section of our PVD products (PVD5840, PVD5810, PVD5660, …). Each video output has its own Total Delay value. Depending on the routing and settings the Processing Delay can be different for each video output, hence the individual Total Delay values for each output.

The Total Delay of each output is the sum of the Processing Delay, the Video Delay set by the user and the Drift Compensation. Drift Compensation is the compensation of the delay between the frame start positions of the reference signal and the video signal. If a module has more than one input, the drift compensation can vary between the different inputs. We will have a closer look at this topic in chapter 1.3 Drift Compensation (reference <> video).

Note: The Total Delay is displayed in milliseconds. There could be a little deviation in the rounding, so a 4 Frame (interlaced) delay can be displayed as 159.9xx ms instead of 160 ms.

Following figure shows an example with a Processing Delay of 1 Frame and a User Delay set to 1 Frame.

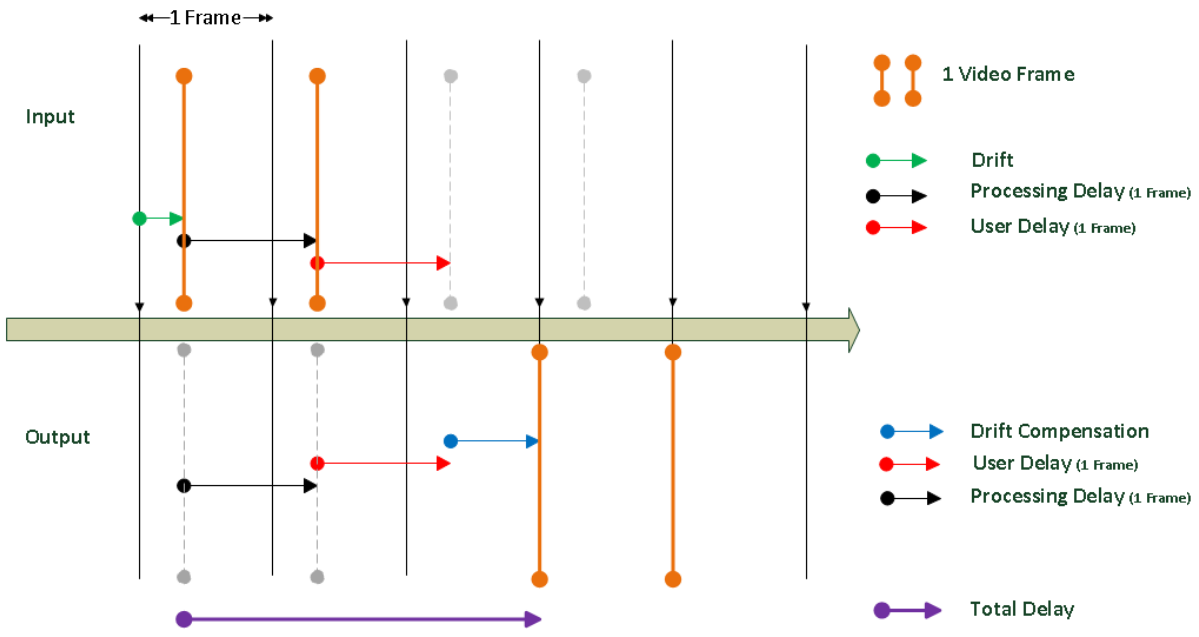

Figure 1: Total Delay example

1.1 Processing Delay

Processing Delay = Frame Sync Buffer + Converter Delay

The *Processing Delay* includes one video frame, needed for the frame sync functionality (following referred as Frame Sync Buffer), and the Converter Delay. The term “Converter Delay” represents the time which is required if the video is routed (processed) through an UPXD converter.

The Converter Delay depends on the input / output standard combination.

If the video signal is routed directly to an output (no converter in the path), the Converter Delay is 0, thus the Processing Delay is 1 Frame (Frame Sync Buffer).

1.2 User Delay

The User Delay is manually set by the user in the APPolo Control GUI in frames, lines, pixels or optionally in milliseconds for each output. This value will be added to the Total Delay of the related output.

1.3 Drift Compensation (reference <> video)

As the PVD’s are Frame Store Synchronizers they will synchronize the incoming video signal to the given reference, respective to the frequency and timing alignment.

This means that the frame start position of the synchronized video output signal is aligned to the frame start position of the given reference signal.

The (varying) Offset between the incoming video signal and the reference is in the following referred as Drift. As the incoming video signal being synchronized (normally) isn’t frequency aligned to the given reference, it will drift in relation to the reference over time.

The Frame Store Synchronizer will compensate this drift. However, the consequence is that the delay of the Drift Compensation will drift over time within one video frame. To not exceed the drift of one frame the module will drop or repeat a frame. In time values this is e.g. 0 ms - 40 ms for a 1080i50 output standard or 0 ms - 20 ms for a 720p50.

If the incoming video signal is frequency but not timing aligned, the offset won't drift in relation to the reference.
In other words, a so called synchronous input signal will have a fixed offset between the reference and the video signal (Figure 2).

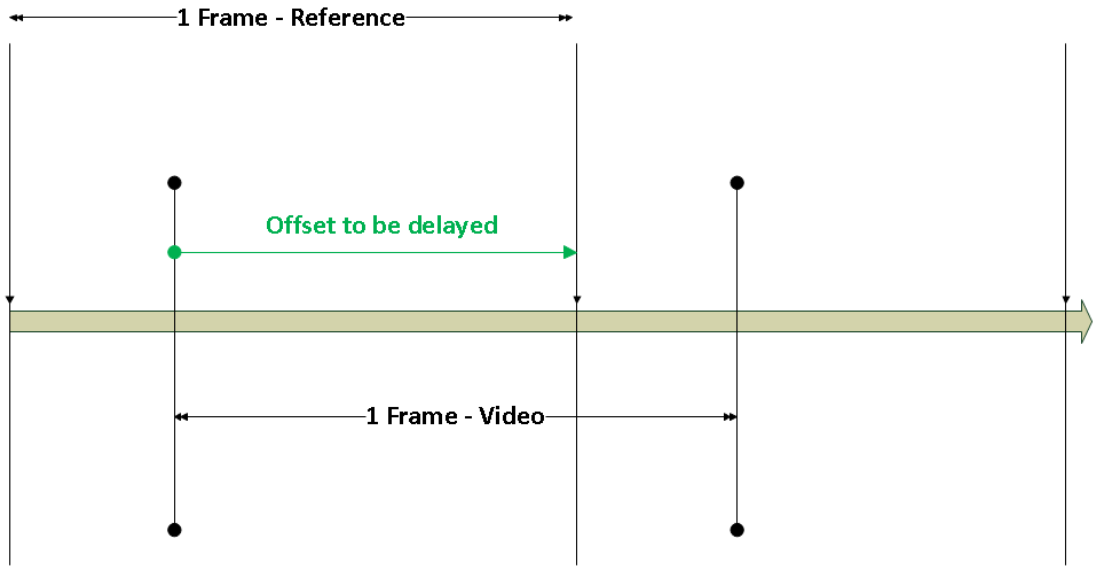

Figure 2: Offset of incoming video to reference signal

1.3.1 A very simplified but illustrative example to understand the difference between frequency and timing alignment

Imagine two cars, same model, driving on a circuit (for this example the distance of each lap for both cars is identical). You will have them "frequency and timing aligned" if both of them are driving with exactly the same constant speed and side-by-side. The cars will stay next to each other no matter how many laps they drive.

If they are not driving side-by-side but still with exactly the same constant speed they are "frequency aligned" but not "timing aligned". The distance between them will not change, they have a constant offset.

Now imagine the cars are driving with constant but different speeds. Take one car as the reference and from this perspective watch the other car. The distance is permanently changing between both cars, there is a drift.

2 Fixed Processing Time - Mode

As mentioned before, the Total Delay of each video output can be different. Now take a PVD5840 as an example:

- Input 1 is routed directly to **Output 1**, which means there is no Converter Delay (see chapter 1.1 Processing Delay). No User Delay set.
- Input 1 is routed via an UPXD converter to **Output 2.** In this case there will be a Converter Delay depending on the video input standard and the selected video output format of the converter. No User Delay set.

In this example both video outputs will have a different Total Delay. The Drift Compensation is the same as both are fed from the same video input. Also, both outputs don't have a User Delay set.

The difference is the Converter Delay which will add delay to the Total Delay of output 2.

If you do not want the Total Delay values of the individual outputs to differ regardless of the signal routing, you can use the "Fixed Processing Time".

This function will result in a Converter Delay of at least 3 Frames for the output, regardless if the source of the output is a converter or not. In other words it will add a virtual Converter Delay if no converter is used. Also, with Fixed Processing Time activated, the module will add a respective amount of full frames to the actual Converter Delay for it to be at least 3 Frames.
Therefore the resulting Processing delay (i.e. Frame Sync Buffer + Converter Delay) will be 4 or 4.5 Frames, depending on the input / output combination of the converter.

The virtual Converter Delay as well as the added delay to the actual Converter Delay that is smaller than 3 frames is deducted from the User Delay.

Hint: If you have mixed (slow and fast) video standards on the outputs (e.g. 720p50 and 1080i50) the Total Delay values will differ anyway as the frames have a different time base (20ms and 40ms).

3 Different Total Delay values after power up or unplugging / plugging a signal

It is possible that you can observe two different (in some special cases 3 different) Total Delay values of the same setup. This can either happen after unplugging / plugging, switching the input standard back and forth or power cycling the module.
The reason as to why this can happen will be explained in the following chapters.

3.1 Slow video standard (1080i50) and fast reference (720p50)

The PVD's internally always work with a slow (interlaced) clock interval locked to the given reference signal. Even a connected fast (20ms e.g. 720p50) reference signal to a PVD will result in an internal slow (40ms e.g. 1080i50) frame interval with a frame start at every second frame of the connected reference (see figures below). In other words, take the fast reference interval and ignore every second frame.

As there are (usually) no frame markers present (first frame, second frame), the decision which frame of the reference signal is used as the first frame for the internal reference is taken by chance (see Figure 3 and Figure 4).

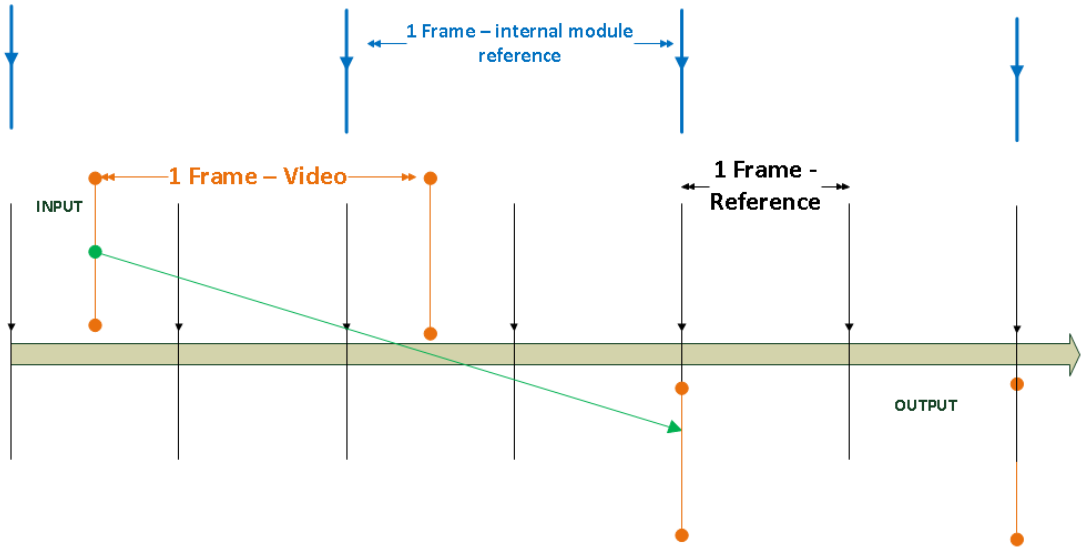

Figure 3: 720p50 ref with 1080i50 video - first possible internal clock interval

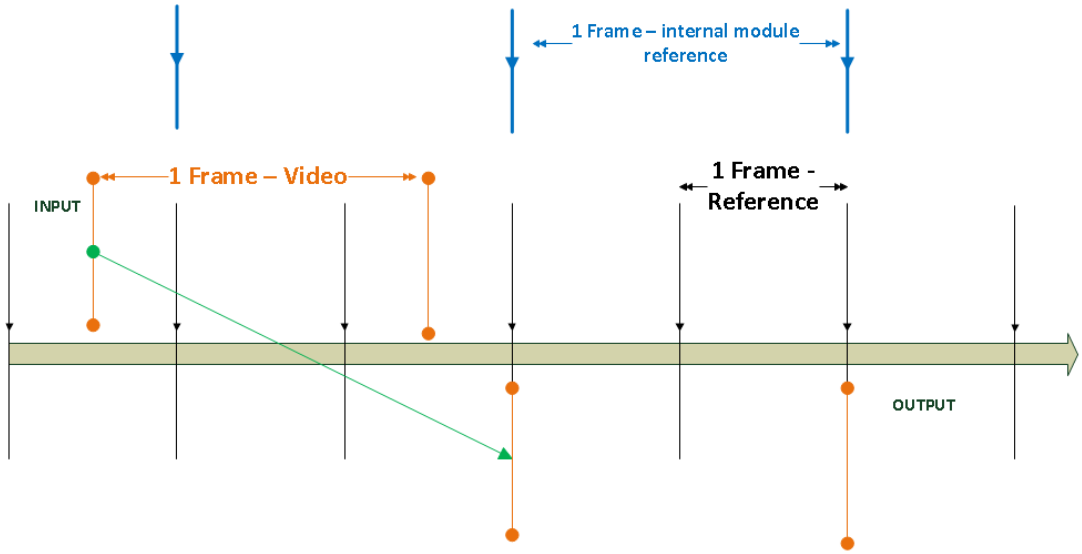

Figure 4: 720p50 ref with 1080i50 video - second possible internal clock interval

The above figures illustrate how a power cycle or unplugging / plugging of the reference signal can result in two different Total Delays, when using a fast reference and a slow video output standard.
As the slow internal clock interval is determined by chance, the Total Delay can differ by 20 ms.

3.2 Converting a fast video standard (720p50) to a slow video standard (1080i50)

The reasoning for this use case is very similar to the one in the previous chapter. When converting a 720p50 signal to a 1080i50 signal, the module has to select one of the two fast frames to be the first of the new converted slow frame.

As mentioned in chapter 3.1 Slow video standard (1080i50) and fast reference (720p50), there are no markers for the progressive frame. Therefore the first progressive frame is chosen by chance.

This can lead to a variation of the Total Delay of 20ms (one progressive frame) when unplugging / plugging the video input signal or power cycling the module.

3.3 Converting a 720p50 signal to a 1080i50 output signal with fast reference

The following setup is the special case that can result in three different Total Delay values after a power cycle or unplugging / plugging the signal.

A 720p50 signal is connected to the video input. The signal is routed via an UPXD converter and is converted to a 1080i50 which is routed to output 1. The internal clock in this case isn't taken from an external reference source but is locked to the 720p50 video input signal.

720p50 on Input => UPXD converter => 1080i50 on Output 1

The setup described in this example will result in a combination of chapter 3.1 and chapter 3.2. This can be visualized in a 2 x 2 matrix with 3 different possible results (as 2 are the same).

Total Delay	Variation of chapter 3.1	Variation of chapter 3.2
+ 0 ms	0ms	0ms
+ 20 ms	0ms	20ms
+ 20 ms	20ms	0ms
+ 40 ms	20ms	20ms

Figure 5: Possible results of delay values by combining chapter 3.1 and chapter 3.2

The Processing Delay to convert a 720p50 signal to a 1080i50 is 1.5 Frames (Frame buffer = 1 Frame, Conversion Delay = 0.5). There is no User Delay applied and because the PVD is locked to the input signal, there is also no Drift Compensation. As the output signal is a 1080i50 and therefore 40ms frame based, the Total Delay is 60ms.

Total Delay = **60 ms** Processing Delay + **0ms** User Delay + **0ms** Drift Compensation

However, as each setup explained in chapter 3.1 and chapter 3.2 also applies to this setup, each can add another 20ms of delay.Therefore the resulting Total Delay can also be **80ms** (60ms + 20ms) if either 3.1 or 3.2 add 20ms, or **100ms** (60ms + 20ms + 20ms) if both 3.1. and 3.2 add 20ms.
Resulting possible Total Delays are:
60ms, **80ms** or **100ms**.

Activating Fixed Processing Time will add another 3 Frames (120ms) to this calculation (see chapter 2 Fixed Processing Time - Mode).
Resulting possible Total Delays with Fixed Processing Time activated are:
180ms, **200ms** or **220ms**.

3.4 Signals with very small timing offset

It can happen that a seemingly frequency and timing aligned input signal of the PVD module requires an additional full frame delay. But why is this?

There are many factors that can introduce a very small delay to a video signal (long cables just to name one). The result of this is a very small timing offset between the video input signal and the reference. This small timing offset however will result in the output video frame being aligned to the next frame start position of the reference (see figure below).

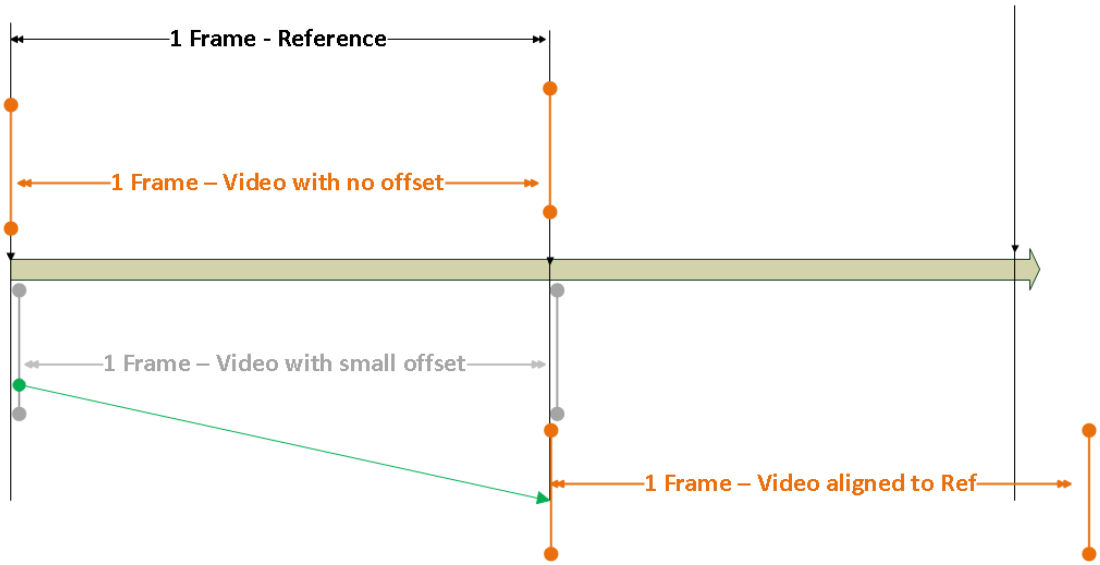

Figure 6: Synchronous video with small offset aligned

Hint: The PVD modules have an “InputToRefTolerance” parameter. With this you can add a tolerance window of up to 12µs to compensate very small timing offsets.

Please visit **support.lynx-technik.com** if you have further questions.