Application Note

74-0070-191120

Understanding Frequency-domain Level Trigger for ThinkRF Real-Time Spectrum Analyzer

This application note explains the frequency-domain level trigger engine used with capturing a signal in real-time using ThinkRF Real-Time Spectrum Analyser, as well as its usage, recommendations and constraints.

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Frequency-domain Level Trigger Mechanism

The digitizer hardware section of a ThinkRF Real-Time Spectrum Analyzer (RTSA), as seen in Figure 1, has an embedded real-time hardware trigger mechanism that provides for user-defined frequency-domain level triggering. The triggering mechanism enables the user's definition of frequency range and power level threshold in the frequency-domain. If a signal exceeds the user-defined power level within the user-defined frequency range, then the trigger mechanism begins storing the time-domain data to memory.

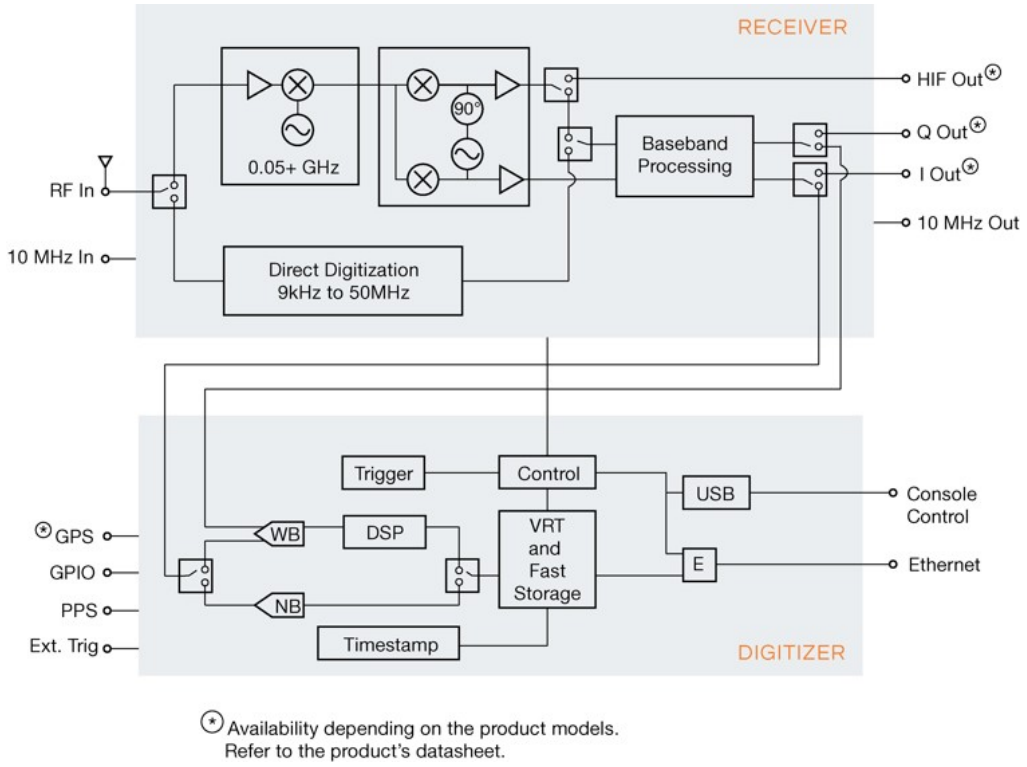

Figure 1: ThinkRF RTSA's Receiver and Digitizer Architecture

Figure 2 illustrates the sequence of steps involved in the triggering and capturing. These steps, as high lighted in the diagram, are:

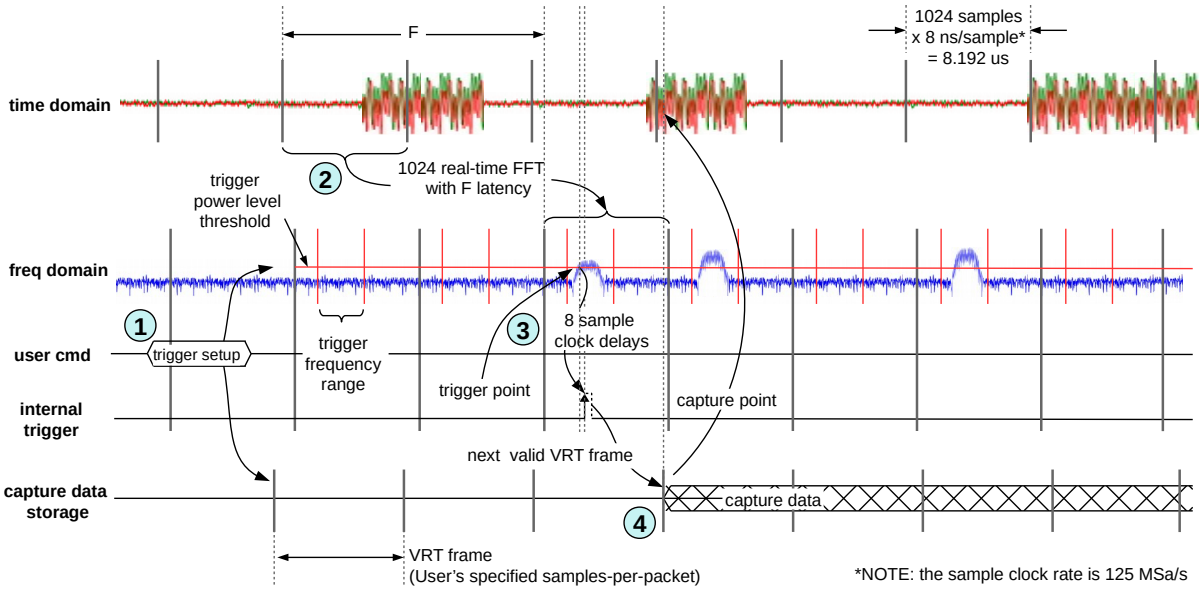

Figure 2: Step Sequence of RTSA's Trigger and Capture

1. Trigger setup is done either through an application or SCPI commands, including defining the amount of data to be captured.
2. Once trigger is enabled, the FFT engine takes sequential frames of 1024 time-domain waveform data and transforms that data to sequential frames of frequency-domain waveform data. The FFT engine is provided with time-domain data at the rate of the 125 MHz sample clock (8 nsec sample-clock period). The time-domain input and FFT frequency-domain output data are pipelined and tightly coupled by a fixed latency ***F*** (17.312 µs) associated with the FFT processing time.
3. The frequency-domain signal is analyzed and, in this example, satisfies the trigger threshold and range; thus, after further 8 clock delays, the trigger-to-capture logic activates the capture flag.
4. The capture flag signals the capture engine to detect the next valid VRT frame and start saving data into the on-board memory for sending back to the user.

Since no storage memory is involved in the time spent during this sequence of events, *the data captured is, thus, of* ***post-triggered nature***.

Trigger SCPI Commands

The frequency level trigger could be used with trace block capture or in conjunction with the sweep capture. To use with a trace capture, issue the following commands:

```
:TRIGger:LEVel <fstart [unit]>,<fstop [unit]>,<level [dbm]>
TRIGger:TYPE LEVEL
```

where fstart and fstop are frequency bounds in unit of GHz, MHz or default Hz, and level the trigger threshold in dBm.

Similarly, to use with a sweep capture, issue these commands:

```
:SWEep:ENTRy:TRIGger:LEVel <fstart [unit]>,<fstop [unit]>,<level [dbm]>
:SWEep:ENTRy:TRIGger:TYPE LEVEL
```

See the *Programer's Guide* of your RTSA product for more information.

Trigger Responsiveness

Note: *The information provided in this section applies to firmware versions 1.6.0 or later for R55x0 and 1.1.0 or later for R57x0. It is recommended to update your device's firmware if the version is older than these.*

For a given trigger level, the trigger mechanism will response within ±3 dBm of that specified threshold. In other words, if the specified trigger level is -40 dBm for example, the trigger events would happen for signals occurred within a desired frequency range with power level within -43 to -37 dBm.

Table 1 shows the maximum and minimum trigger thresholds for different attenuation levels. The responsiveness of the trigger mechanism for trigger levels set outside these thresholds is saturated and, thus, might result in no or false trigger events.

Table 1: Max and Min Trigger Thresholds for Different Attenuation Levels for SH/SHN/ZIF

Attenuation (dB)	Max Threshold (dBm)	Min Threshold (dBm)
0	-15	Approximately 12 dBm above the noise floor (relative to 10 kHz RBW)
10	-5	
20	0	
30	5	

For best trigger performance, set the trigger level within these max and min thresholds. Also, for best trigger detection near the noise floor (of up to approximately -93 dBm), use 0 dB attenuation.

See Trigger Constraints section for some constraints affecting the trigger responsiveness.

Trigger Data Capture Setting Recommendation

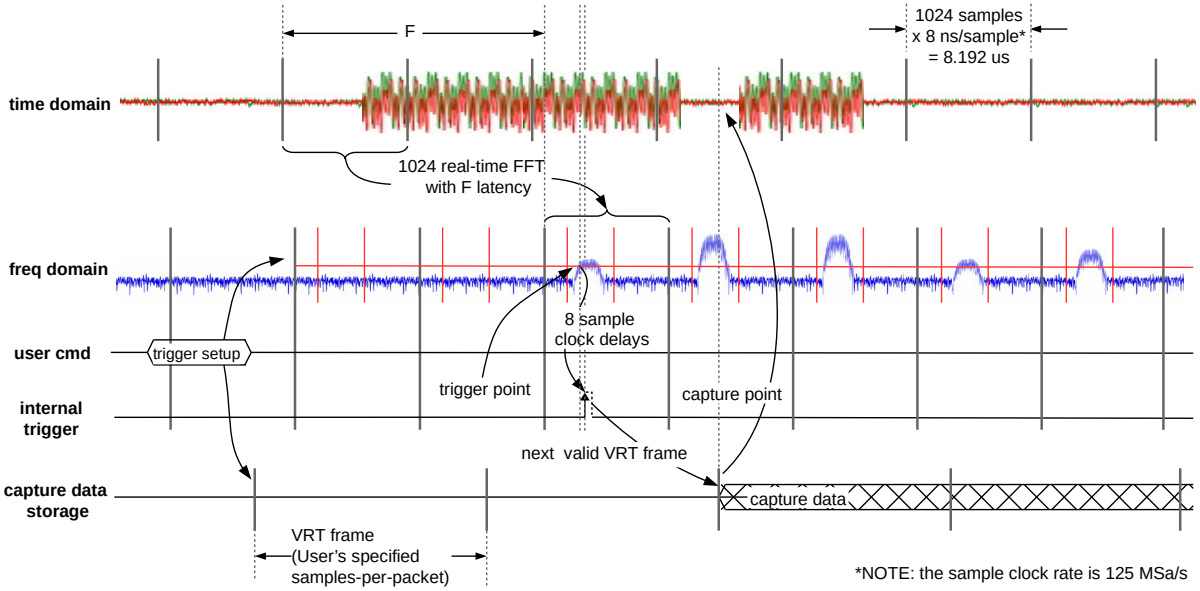

Figure 3: Trigger Capture Containing No Signal

In Figure 3 trigger example, notice the time gap from the trigger point to the capture point. This time gap is due to the capture engine waiting for the next valid VRT frame available to start the capturing. The gap varies depending on the size of the VRT frame size set and the

occurrence of the VRT frame starting point relative to the trigger point. A VRT capture frame is defined through the SCPI command :TRACe:SPPacket (or for sweep, :SWEep:ENTRy:SPPacket). If SPP (samples per VRT packet) is large (such as 1k or larger), the next valid VRT frame might occur at a long duration later (e.g. 32k / 125 MHz = 0.262 msec).

To minimize this time gap, a small SPP is recommended. The smallest SPP allowed is 256 (see your RTSA's *Programer's Guide* for more information). Then use :TRACe:BLOCk:PACKets (or for sweep, :SWEep:ENTRy:PPBlock) command to define how many SPP packets are needed. A block size of SPP * PPB (packets per block) is of continuous and contiguous data. For example, to capture 32k samples, instead of setting SPP to 32k, set:

:TRACe:SPPacket 512 (or for sweep, :SWEep:ENTRy:SPPacket 512)
:TRACe:BLOCk:PACKets 64 (or for sweep, :SWEep:ENTRy:PPBlock 64)

A point of consideration, by VRT protocol (see your RTSA's *Programer's Guide*), a VRT packet would have header and trailer words added to the data packet; thus, the smaller the SPP, the more header and trailer words added to the network transfer, this could affect the efficiency of the network throughput, but not substantially.

Trigger Constraints

The frequency-domain level trigger is recommended to use with SH/SHN modes as these modes have the best performance and are without IQ imbalance.

Due to resource limitations, the frequency-domain level trigger design makes use of a 1024-point FFT embedded within the RTSA's FPGA chip without windowing and any signal correction. This design method, therefore, results in the following constraints:

1. The trigger currently does not support DD (baseband) and HDR (100 kHz span) RFE modes.
2. In ZIF RFE mode, IQ imbalance image and DC offset are not corrected within the RTSA; thus, they might cause potential false triggering. The ZIF mode would work well if the trigger threshold is set to within 15 dB of the input signal.
3. Without windowing to improve signal clarity, the spectral leakage (side-skirt) of an input signal might also cause false triggering. The stronger an input signal is relative to the trigger threshold used, the wider the side-skirt leakage, causing a larger frequency error in the triggering range. The false trigger range is as characterized in Table 2. This error range refers to trigger frequency start *minus* the error value or trigger frequency stop *plus* the error value. For example, if trigger frequency range is 2310–2320 MHz with threshold at -55 dBm, attenuation is 10 dB, input signal is -30 dBm, then with the frequency error range of ~1 MHz for 25 dB difference, the actual triggered frequency range is 2309–2321 MHz.

Table 2: Input-to-Threshold Level Difference and Frequency Error Range

Input-to-Threshold Difference (dB)	Frequency Error Range (MHz)
15	0.2
20	0.5
25	1.0
30	1.5
35	3.2
40	6.5
45	15.0

To minimize the false trigger, it is recommended to adjust the trigger threshold level to ~30 dBm or less than the potential input signal.

4. With only 1024-point FFT (or 122 kHz RBW) used in the RTSA, the resolution of the triggered frequency range might not exactly matched the capture RBW (data capture size) used.
5. The captured trigger data is of ***post-triggerred capture***, this means the data might not include the triggered signal itself.

References

Related Documents

- Refer to https://www.thinkrf.com/documentation/#product-manuals for the appropriate ThinkRF RTSA Programmer's Guide.

Abbreviations

ADC	Analog-to-Digital Converter
DC	Direct Current
DD	Direct Digitizer (Baseband)
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
HDR	High Dynamic Range (100 kHz IBW)
IQ	In-phase and Quadrature
IBW	Instantaneous Bandwidth
RF	Radio Frequency
RFE	Receiver Front-End
RTSA	Real Time Spectrum Analyser
SCPI	Standard Commands for Programmable Instruments
SH	Super-Heterodyne (40 MHz IBW)
SHN	Super-Heterodyne with Narrower bandwidth (10 MHz IBW)
ZIF	Zero Intermediate Frequency (100 MHz IBW)

Document Revision History

This section summarizes document revision history.

Document Version	Release Date	Revisions and Notes
v1.0	Nov 20, 2019	First release.

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