

FOIA MARKER

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Semiconductor Industry Association (SIA) [2]

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October 11, 1993

Mr. Lionel S. Johns
Associate Director
Office of Science and Technology Policy
Old Executive Office Building, Room 426
Washington DC 20500

Dear Mr. Johns:

Thank you for participating in the industry/government meetings held on October 1, 1993. The Semiconductor Industry Association ("SIA") was pleased to have the opportunity to engage in a useful exchange of information regarding lithography R&D and SIA's proposed technology programs.

We believe these meetings were an important step in ensuring continued, successful collaboration between industry and government. As agreed upon at the meeting, SIA intends to do the following:

- ▶ Continue to evaluate SVGL's Micrascan technology;
- ▶ Review SVGL's proposed business plan and the potential relationship with Canon;
- ▶ Periodically update SVGL's market prospects for the Micrascan technology;
- ▶ Inform the U.S. government of any significant developments affecting SVGL and the extent of industry funding, if any, that can be usefully applied in this situation; and
- ▶ Provide the U.S. government with a detailed White Paper discussing each proposed technology program.

SIA looks forward to continued dialogue with the government regarding both the lithography issue and funding of other technology areas.

Sincerely,



George M. Scalise
Chairman
SIA Public Policy Committee


MOTOROLA
Semiconductor Products Sector

 6505 William Cannon Drive West
 Austin, TX 78735-8598

 To: **Amy Carlson**

 From: **Owen P. Williams**

 Date: **November 10, 1993**

Phone: 512 891 3749

Fax: 512 891 3785

Mail Drop: OE14

CC:

 Subject: **Associated White Paper Expenditures at SIA**

Amy, Please find attached the information on SRC and SEMATECH expenditures in 1994 associated with the seven white papers. Please note the SRC expenditures in the area of University Research Support

Technology Area	million \$*		Total
	SRC	SEMATECH	
Metrology	1.0	0.9	1.9
Modeling/Simulation	5.0	8.5	13.5
Lithography	2.2	17.8	20.0
Packaging	3.0	3.3	6.3
(SEDEC)	1.8	0.	1.8
Technology Evaluation Program	0.	6.7	6.7
(SETEC)	0.	<u>5.3</u>	<u>5.3</u>
Total	13.0	42.5	55.5

* - estimate round numbers


SEMICONDUCTOR INDUSTRY ASSOCIATION

4300 Stevens Creek Boulevard - Suite 271
San Jose - CA 95129 - (408) 246-2711

FAX (408) 246-2830

July 1, 1993

The Honorable John M. Deutch
Undersecretary of Defense for
Acquisition
Department of Defense
The Pentagon, Room 3E-933
Washington, DC 20301-3010
FAX: 703-696-4268

Dr. John H. Gibbons
Assistant to the President for
Science & Technology Policy and
Director, Office of Science & Technology Policy
Old Executive Office Building, Room 424
17th Street & Pennsylvania Avenue, NW
Washington, DC 20500
FAX: 202-395-3719

Dear Drs. Deutch and Gibbons:

In anticipation of an SIA delegation meeting with you at 2:00pm on 16 July at the Pentagon, I am writing to explain the purpose of our visit as well as to suggest objectives. A list of industry participants from SIA, SEMATECH and SRC is attached.

Following the advice of the National Advisory Committee on Semiconductors, the SIA sponsored a three-day conference last November to create a unified national technology strategy for semiconductors. The two objectives were (a) to achieve technological leadership in world competition and (b) to do so without increasing aggregate expenditures for semiconductor research. Nearly 200 technical experts were invited from industry, government, and academia to construct a series of semiconductor technology roadmaps to the year 2007. The participants also identified broad technical and economic challenges which cut across several technologies.

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Reports of the conference findings and recommendations have been broadly distributed. There is ample anecdotal evidence that these reports are being used as a baseline for research planning in labs throughout the nation. The conference reports have also formed the basis for a major new CRADA between SEMATECH and the Sandia National Labs as well as a broad new agreement between Sandia and NIST.

The SIA, SEMATECH and SRC have extensively revised their programs and priorities to address the national technology strategy for semiconductors. The SIA is prepared to monitor and update the roadmaps. SEMATECH and SRC have broadened their charters, e.g., SEMATECH is addressing the semiconductor packaging issue without increasing its budget.

SEMATECH and SRC are revamping their advisory board structures to accommodate the roadmaps and to provide increased synergy between the two consortia. Shortly, the two semiconductor consortia will be inviting government representatives to integrate into the revised advisory structures.

During the past several weeks, there has been a series of Washington roundtables bringing together the semiconductor industry and government (DOD, DOE, DOC, NSF, OSTP, and NEC) to discuss the structure and strategy for implementation of the technology strategy. Topics covered have included:

- o Formation of a new Semiconductor Technology Council to be co-chaired by industry and government (substitute for SEMATECH Oversight Committee) to provide broad policy guidelines for the program long term.
- o Creation of a model CRADA for the industry (5 CRADAs are now under negotiation between SRC and the Federal labs). Restrictions on foreign manufacturing have prevented closure thus far.
- o Obtaining a crosscut of U.S. government semiconductor research activity (OSTP FCCSET process) as a basis for realigning resources.
- o Setting technical priorities in lithography, semiconductor packaging, contamination free manufacturing, metrology and sensors, and modeling and simulation. (The establishment of a national lithography strategy is the foremost challenge).

With the above background, I would like to suggest the following objectives for the July 16 meeting:

- o Agreement on formation, composition, and mission of the Council. Schedule first meeting.
- o Approach to resolve remaining disincentives to private sector cooperative alliances with Federal labs, including CRADA restrictions.
- o Agreement to proceed with a FCCSET crosscut for semiconductors on a priority basis.
- o Mutual understanding of overarching technology and business issues.

If you have comments on any of the above, including the meeting objectives, please do not hesitate to contact me (Phone: 602-554-5977, FAX: 602-893-7755) or Clark McFadden, SIA counsel at Dewey Ballantine (Phone: 202-429-2333 or 2319, FAX: 202-862-1093).

My colleagues and I sincerely look forward to our upcoming discussions and to the beginning of a long term cooperative relationship.

Sincerely,



Craig R. Barrett
Executive Vice President &
Chief Operating Officer
Intel Corporation
and
Chairman
SIA Technology Strategy
Committee

cc: Clark McFadden, Dewey Ballantine
A. A. Procassini, SIA President

7/1/93

**GOVERNMENT/INDUSTRY MEETING
WITH UNDERSECRETARY DEUTCH (DOD) AND
PRESIDENT'S SCIENCE ADVISOR GIBBONS
THE PENTAGON
FRIDAY, JULY 16 1992, 2:00PM**

INDUSTRY REPRESENTATIVES

Chairman, SIA Technology Strategy Committee:

**Craig R. Barrett
Executive Vice President & Chief Operating Officer
Intel Corporation**

Colleagues:

**Dr. Gilbert F. Amelio
President & CEO
National Semiconductor Corporation
and
Chairman, Semiconductor Industry Association (SIA)**

**Dr. Michael J. Attardo
IBM VP & General Manager, Technology Products
IBM Corporation**

**Dr. William Siegle
VP & Chief Scientist
Advanced Micro Devices, Inc.**

**Dr. William J. Spencer
President & CEO
SEMATECH**

**Larry Sumney
President
Semiconductor Research Corporation (SRC)**

Staff:

**Dr. David Beecham
Industry Relations Director
AT&T Microelectronics
and
Technology Program Chairman, SIA Public Policy Committee**

**Clark McFadden
Partner
Dewey Ballantine**

Urgent:XX Routine:

SIA
Semiconductor Industry Association
4300 Stevens Creek Boulevard, Suite 271
San Jose, CA 95129
(408)246-2711

FAX TRANSMITTAL
Fax Number: (408)246-2830

Memorandum

Date: July 1, 1993

#Pages Including Cover: 5

To: Dr. John H. Gibbons
Office of Science &
Technology Policy
Old Executive Office Building, Room 424

FAX #: 202-395-3719

From: Craig R. Barrett, Intel Corporation

Henry K.
send c/c Kitty G.

SIA

SEMICONDUCTOR INDUSTRY ASSOCIATION

4300 Stevens Creek Boulevard • Suite 271
San Jose • CA 95129 • (408) 246-2711

FAX (408) 246-2830

October 29, 1993

Mr. Lionel S. Johns
Associate Director
Office of Science and Technology Policy
Old Executive Office Building, Room 426
Washington, DC 20500

Dear Skip:

Following an update on the current status of the negotiations between Silicon Valley Group ("SVG") and Canon, the SEMATECH Board of Directors unanimously confirmed their earlier position that a favorable agreement between SVG and Canon offers the better currently available course toward achieving a viable U.S. manufacturer of lithography systems.

In addition, the Board also resolved that in light of the pending licensing agreement between SVG and Canon, no further direct technology development funding from SEMATECH would be appropriate. Should the ultimate agreement be judged acceptable to SEMATECH and its members and in the best interests of the United States, the Board authorized SEMATECH to fund activities aimed at insuring that the execution of the agreement will indeed be beneficial to the country.

These activities might include funding of teams of SEMATECH engineers stationed at both the SVG Lithography site in the United States and at the Canon site in Japan plus the purchase of prototype step-and-scan machines for testing and evaluation, and other in-kind support such as light sources, metrology, resist and test wafers. SEMATECH's emphasis would be on evaluation of the prototype machine and facilitating the transfer of manufacturing technology from Canon to SVG.

Please do not hesitate to contact me if you have any questions.

Sincerely,



George M. Scalise
Chairman, SIA Public Policy Committee,
and
Senior Vice President and
Chief Administrative Officer,
National Semiconductor Corporation



SEMICONDUCTOR INDUSTRY ASSOCIATION

4300 Stevens Creek Boulevard • Suite 271
San Jose • CA 95129 • (408) 246-2711

FAX (408) 246-2830

January 6, 1994

Date Rec'd 1-11-94

ACTION to
INFO to Gibbons
Johns
Wales
Nanson

Gillman

Dr. John H. Gibbons
Assistant to the President for Science & Technology and
Director, Office of Science & Technology Policy
Old Executive Office Building
Room 424
Washington, D.C. 20500

SIG of _____
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Dear Dr. Gibbons:

Section 273 of the Defense Authorization Act of 1994 creates a new Semiconductor Technology Council. The Council is charged with an important mission that could significantly contribute to semiconductor technology development in both the public and private sectors.

In an effort to assist in the launching of this Council, the Semiconductor Industry Association (SIA), along with Semiconductor Equipment and Materials International (SEMI), the American Electronics Association (AEA), and the Computer Systems Policy Project (CSPP) have sought to develop a consensus slate of acknowledged industry leaders as candidates to fill the nine industry slots on the Council, as well as a distinguished professor to fill the academic slot.

The candidates set forth on the attached list have been approved by the relevant associations mentioned above. They all enjoy broad and enthusiastic support and reflect a cross section of the private sector, including both large and small firms.

We believe these candidates would enable the Council most effectively to achieve its objectives. On behalf of the SIA, we would greatly appreciate your consideration of these candidates as you prepare a recommendation to the President.

Sincerely,

A. A. Procassini
President

SEMICONDUCTOR TECHNOLOGY COUNCIL NOMINEES

Semiconductor Device Industry (SIA)

Craig R. Barrett (Co-Chairman)
Chief Operating Officer
Intel Corporation

Michael J. Attardo
IBM VP and General Manager Technology Products
IBM Corporation

Dr. Thomas D. George
President, Semiconductor Products Division
Motorola, Incorporated

William P. Weber
Vice Chairman
Texas Instruments, Incorporated

Semiconductor User Industry (AEA and CSPP)

James G. Treybig
President and CEO
Tandem Computers, Incorporated

Robert J. Paluck
Chairman, President and CEO
Convex Computer Corporation

Michael J. Birck
President
Tellabs, Incorporated

Semiconductor Equipment and Materials Industry (SEMI)

James C. Morgan
Chairman and CEO
Applied Materials, Incorporated

Kenneth Levy
President and CEO
KLA Instruments Corporation

Academic (SIA)

Dr. James D. Meindl
Joseph M. Pettit Chair Professor of Microelectronics
Georgia Institute of Technology



SEMICONDUCTOR INDUSTRY ASSOCIATION

4300 Stevens Creek Boulevard • Suite 271
San Jose • CA 95129 • (408) 246-2711

FAX (408) 246-2830

April 14, 1993

Date Rec'd 4/19/93

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JHG w/copy
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DATE DUE _____

Dr. John Gibbons
Assistant to the President
Science & Technology
Executive Office of the President
Old Executive Office Building, Room 358
17th St. & Pennsylvania Ave., NW
Washington DC 20500

Dear Dr. Gibbons:

Enclosed is a copy of a 1992 publication entitled, *Creating Advantage: Semiconductors and Government Industrial Policy in the 1990s*. This book provides an account of various governments' promotional policies for their domestic semiconductor industries.

U.S. Government policy actions have been instrumental in the U.S. semiconductor industry's current resurgence. In 1992, the U.S. industry regained worldwide market share, matching Japan. *Creating Advantage* is an analysis of not only foreign government targeting of the semiconductor industry, but also an account of how the U.S. Government can and does help an industry in trouble. The U.S. semiconductor industry is an excellent example of successful U.S. Government-industry cooperation.

I hope you find the material useful. If you have any questions, please call Warren Davis of SIA at (408) 246-2711 or Tom Howell of Dewey Ballantine at (202) 862-2354.

Sincerely,

A.A. Procassini
President

cc: Warren Davis
Tom Howell
Amy Carlson



SEMICONDUCTOR INDUSTRY ASSOCIATION

4300 Stevens Creek Boulevard • Suite 271
San Jose • CA 95129 • (408) 246-2711

FAX (408) 246-2830

April 14, 1993

Mr. Lionel S. Johns
Associate Director
Office of Science & Technology Policy
Old Executive Office Building
17th & Pennsylvania Ave., NW, Room 426
Washington, DC 20500

Dear Mr. Johns:

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U.S. Government policy actions have been instrumental in the U.S. semiconductor industry's current resurgence. In 1992, the U.S. industry regained worldwide market share, matching Japan. *Creating Advantage* is an analysis of not only foreign government targeting of the semiconductor industry, but also an account of how the U.S. Government can and does help an industry in trouble. The U.S. semiconductor industry is an excellent example of successful U.S. Government-industry cooperation.

I hope you find the material useful. If you have any questions, please call Warren Davis of SIA at (408) 246-2711 or Tom Howell of Dewey Ballantine at (202) 862-2354.

Sincerely,

A handwritten signature in black ink, appearing to read "A.A. Procassini", written over a horizontal line.

A.A. Procassini
President

cc: Warren Davis
Tom Howell
Amy Carlson

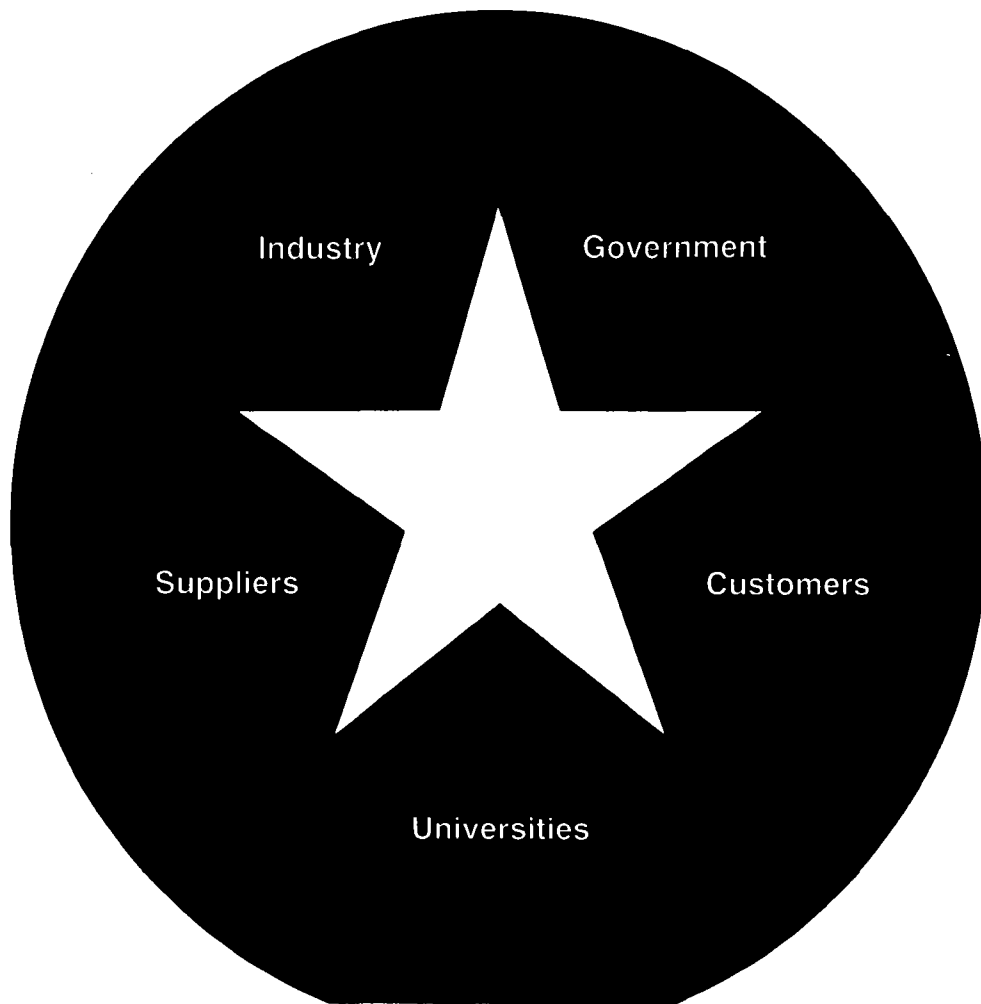
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SEMICONDUCTOR TECHNOLOGY



WORKSHOP CONCLUSIONS

EXECUTIVE OFFICE OF THE PRESIDENT
OFFICE OF SCIENCE AND TECHNOLOGY POLICY
WASHINGTON, D.C. 20506

July 16, 1993

MEMORANDUM FOR: **SKIP JOHNS, KITTY GILLMAN**

SUBJECT: **TALKING POINTS FOR SIA MEETING WITH DEUTCH**

FROM: **MARK HARTNEY** *mf*

SIA has proposed four topics for the agenda for this afternoon's meeting:

(1) **Semiconductor Technology Council:**

- OSTP supports the idea of the council and the mission of the group to bring industry and government together, where possible, to work towards implementation of the roadmap. Broadening the scope of the SEMATECH advisory council is the appropriate way to accomplish this.
- OSTP will not support a FACA exemption for the committee, since we are charged with reviewing the FACA legislation. We do not want to solve the problems with FACA by issuing exemptions in the interim while working on the broader problem.
- Despite industry's concerns, this administration will provide a more favorable environment than the Bush administration did for the NACS committee.
- There is a need for government-industry interaction at several levels - this committee is at the highest policy level, but discussions are needed at the laboratory division and program director level as well.

(2) **CRADA issues:**

- SIA's biggest concern is the restriction of CRADA's to firms which do a majority of their manufacturing in the U.S.
- They would also like to establish a "blanket CRADA" to work with the labs, much like the CSPP has.
- This is primarily a DOE concern - OSTP would like to see the process move more rapidly, but wants to insure that the benefit of laboratory technology accrues in the U.S.

(3) Semiconductor Crosscut:

- As they are aware, an Electronics Working Group has been established under the FCCSET PMES Committee and has begun meeting in the past two months.
- The industry associations, including SIA, recently sent a letter to Gibbons supporting an Electronics Cross-cut. We appreciate their interest and are considering how to best proceed with such an activity.
- The scope of the committee, and any cross-cut developed (formal or informal) will include electronics broadly, not just semiconductors.
- Electronics may be included as a sector called out in the manufacturing cross-cut and initiative.
- The Electronics Working Group has been meeting with a number of industry associations. The SIA has been an active participant, and has shown leadership in preparing their roadmap and developing priorities.

(4) Technology and Business Issues:

- SIA will present technology strategies in their five priority areas: lithography, packaging, modeling and simulation, metrology and sensors, and contamination-free manufacturing.
- The policy level committee (i.e. Johns/ Deutch) is not the appropriate group to consider these, so we need not comment on the technology issues presented.
- Consideration needs to be given to government's role not only in technology development, but in working with industry to achieve commercial success and viable businesses as well.
- The conference call two months ago did not produce an industry consensus that a complete domestic supplier base was essential - is this an accurate picture?

EXECUTIVE OFFICE OF THE PRESIDENT
OFFICE OF SCIENCE AND TECHNOLOGY POLICY
WASHINGTON, D.C. 20506

April 30, 1993

MEMORANDUM FOR: SKIP JOHNS

SUBJECT: COVER LETTER FOR SIA WORKSHOP

FROM: MARK HARTNEY *MH*

I've attached an updated draft for the letter to go out to agency and lab directors with the SIA workshop report. In addition, I developed a list from the Federal Labs Database of the appropriate addressees, and finally received a list from SIA of the people they have sent the workshop proceedings to already. These lists are attached, and I've selected the appropriate names off the SIA list.

Let me know what you think of the list and the cover letter so we can move forward with this.

DRAFT

April 30, 1993

MEMORANDUM FOR AGENCY AND LABORATORY DIRECTORS

SUBJECT: SEMICONDUCTOR TECHNOLOGY RESEARCH

FROM: DR. JOHN H. GIBBONS, DIRECTOR

Enclosed are the findings of a workshop held last November by the Semiconductor Industry Association to identify the technology needed over the next 15 years for continued progress in the semiconductor industry. The workshop participants were drawn from companies and universities, with participation from some of the relevant government laboratories and agencies as well.

The assessment maps out a common research vision which will be shared by the companies, collaborative organizations like SEMATECH and the Semiconductor Research Corporation (SRC), and universities. Government laboratory expertise can also be brought to bear on the problems identified, and can play a crucial role in solving challenges not only of mission-relevant needs but of the semiconductor industry as well.

A key component of the President's and Vice-President's Technology Proposal is the establishment of a closer working relationship between industry and federal governments. These closer relationships will lead to improved job creation, economic security, and social benefits. The participation of government employees in the workshop which developed this roadmap was a first step in that direction. Additionally, a new interagency working group on electronics has been formed as part of the FCCSET committee on Physical, Mathematical, and Engineering Sciences. This group, chaired by Dr. Lance Glasser from ARPA, will help to coordinate government efforts in developing electronic technology and will also work to identify areas of mutual benefit with industry where they can help to implement the technology roadmap.

I urge you to examine your own agency's or laboratory's activities in light of the roadmap developed by the SIA and to work with the interagency group to assess the areas where you can contribute to the government's and industry's efforts for continued success in microelectronics.

Facility: Advanced Integrated-Circuit Test Structure Metrology
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
B360 Technology
Gaithersburg, MD
20899 United States

Contact: Loren W. Linholm
Phone: (301) 975-2052
FAX:

Facility: Aerospace Controls Research Laboratory
Parent Mainlab: Langley Research Center
Parent Agency: National Aeronautics and Space Administration
Subelement Agency: None

Address: Mail Stop: MS200
Langley Research Center, (Industrial Applications Center)
Hampton, VA
23665-5225 United States

Contact: Mr. Harry J. Samos
Phone: (804) 864-5867
FAX: (804) 864-8314

Facility: Avionics Directorate
Parent Mainlab: Wright Laboratory
Parent Agency: Department of Defense
Subelement Agency: Department of the Air Force

Address: Air Force Wright Aeronautical Laboratories
Department of the Air Force
ORTA AFWAL/XP
Wright-Patterson AFB, OH
45443 United States

Contact: Cindy Ingalls or Dr. J.C. Ryles
Phone: (513) 255-3570
FAX: (513) 258-4424

Facility: Bulk Crystal Growth Facility
Parent Mainlab: Naval Research Laboratory, Washington, D. C.
Parent Agency: Department of Defense
Subelement Agency: Department of the Navy

Address: ORTA Code 1003.1
4555 Overlook Ave.
Washington, DC
20375 United States

Contact: Dr. Richard Rein
Phone: (202) 767-3744
FAX: (202) 404-7920

Facility: Center for Advanced Materials
Parent Mainlab: Lawrence Berkeley Laboratory
Parent Agency: Department of Energy
Subelement Agency: None

Address: Lawrence Berkeley Laboratory
Bldg. 66
One Cyclotron Road
Berkeley, CA
94720 United States

Contact: Dr. Mark Alper
Phone: (510) 486-4755
FAX: (510) 486-4995

Facility: Compound Semiconductors and Semiconductor
Microstructure
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
A305 Technology
Gaithersburg, MD
20899 United States

Contact: David G. Seiler
Phone: (301) 975-2081
FAX:

Facility: Electromagnetics and Reliability Directorate
Parent Mainlab: Rome Laboratory
Parent Agency: Department of Defense
Subelement Agency: Department of the Air Force

Address: Department of the Air Force
Rome Laboratory
XP
Griffiss AFB, NY
13441-5700 United States

Contact: Mr. Billy G. Oaks
Phone: (315) 330-3705
FAX: (315) 330-3022

Facility: Electronics and Electrical Engineering Laboratory
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
B358 Metrology
Gaithersburg, MD
20899 United States

Contact: Mr. Judson C. French
Phone: (301) 975-2220
FAX:

Facility: Laser Studies of Semiconductor Materials
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
JILA
Boulder, CO
80303 United States

Contact: Stephen R. Leone
Phone: (303) 492-5128
FAX:

Facility: Manufacturing Technology Directorate
Parent Mainlab: Wright Laboratory
Parent Agency: Department of Defense
Subelement Agency: Department of the Air Force

Address: Department of the Air Force
Manufacturing Technology Directorate
Wright-Patterson AFB, OH
45433-6533 United States

Contact: Cindy Ingalls or Mr. J. W. Schulz
Phone: (513) 255-2006
FAX: (513) 258-4424

Facility: Materials Directorate
Parent Mainlab: Wright Laboratory
Parent Agency: Department of Defense
Subelement Agency: Department of the Air Force

Address: Air Force Aeronautical Laboratories
ORTA AFWAL/XP
Wright-Patterson AFB, OH
45433 United States

Contact: Cindy Ingalls or Dr. H.M. Burte
Phone: (513) 255-3570
FAX: (513) 258-4424

Facility: Materials Science and Engineering Laboratory
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
B309 Materials
Gaithersburg, MD
20899 United States

Contact: Dr. Lyle H. Schwartz
Phone: (301) 975-5658
FAX:

Facility: Measuring Patterned Layers on Integrated Circuits
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
A347 Technology
Gaithersburg, MD
20899 United States

Contact: Robert D. Larrabee
Phone: (301) 975-2298
FAX:

Facility: Microelectric Programs
Parent Mainlab: Sandia National Laboratories
Parent Agency: Department of Energy
Subelement Agency: None

Address: Technology Transfer and Policy Department
P. O. Box 5800
Albuquerque, NM
87185 United States

Contact: Olen Thompson
Phone: (505) 845-9407
FAX: (505) 844-2363

Facility: Microelectronic Technology Center of Excellence
Parent Mainlab: Naval Weapons Support Center Crane
Parent Agency: Department of Defense
Subelement Agency: Department of the Navy

Address: Code PM1
Crane, IN
47522-5000 United States

Contact: Mr. Duane Embree
Phone: (812) 854-3667
FAX: (812) 854-1227

Facility: Microelectronics Laboratory
Parent Mainlab: Naval Command, Control & Ocean Surveillance
Center; RDT&E Division
Parent Agency: Department of Defense
Subelement Agency: Department of the Navy

Address: Solid State Electronics Division
NOSC Code 55
San Diego, CA
92152-5000 United States

Contact: Dr. Howard Rast
Phone: (619) 553-1032
FAX:

Facility: Molecular Beam Epitaxy
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
A357 Technology
Gaithersburg, MD
20899 United States

Contact: James Comas
Phone: (301) 975-2061
FAX:

Facility: Optical Electronics
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None
Address: National Institute of Standards and Technology (NIST)
Div. 814.02
Boulder, CO
80303 United States

Contact: Aaron A. Sanders
Phone: (303) 497-5341
FAX:

Facility: Optical Electronics Laboratory
Parent Mainlab: Naval Command, Control & Ocean Surveillance
Center; RDT&E Division
Parent Agency: Department of Defense
Subelement Agency: Department of the Navy

Address: Solid State Electronics Division
NOSC Code 55
San Diego, CA
92152-5000 United States

Contact: Dr. Howard Rast
Phone: (619) 553-1032
FAX:

Facility: Optical Fabrication, Coating and Testing Laboratory

Facility: Reliability Analysis Center (RAC)
Parent Mainlab: Rome Laboratory
Parent Agency: Department of Defense
Subelement Agency: Department of the Air Force

Address:
Griffiss AFB, NY
13441-5700 United States

Contact: Mr. Jack Bart
Phone: (315) 330-4114
FAX:

Facility: Resource for Biomedical Sensor Technology
Parent Mainlab: Biomedical Research Technology Program, NCRR
Parent Agency: Department of Health and Human Services
Subelement Agency: National Institutes of Health

Address: Bingham Building, Room 112
Case Western Reserve University
10900 Euclid Avenue
Cleveland, OH
44106 United States

Contact: Chung-Chiun Liu, Ph.D.
Phone: (216) 368-2935
FAX: (216) 368-8738

Facility: Semiconductor Detector Laboratory
Parent Mainlab: Brookhaven National Laboratory
Parent Agency: Department of Defense
Subelement Agency: Department of the Navy

Address: Instrumentation Division
535-B
Upton, NY
11973 United States

Contact: Hobart W. Kraner
Phone: (516) 282-4238
FAX: (516) 282-3729

Facility: Semiconductor Detector Technology Laboratory
Parent Mainlab: Lawrence Berkeley Laboratory
Parent Agency: Department of Energy
Subelement Agency: None

Address: Lawrence Berkeley Laboratory, Engineering Division
Number One Cyclotron Road
Mail Stop 29/100
Berkeley, CA
94720 United States

Contact: Dr. Richard H. Pehl
Phone: (510) 486-5660
FAX: (510) 486-4122

Facility: Semiconductor Devices
Parent Mainlab: National Institute of Standards and Technology
Parent Agency: Department of Commerce
Subelement Agency: None

Address: National Institute of Standards and Technology (NIST)
B310 Technology
Gaithersburg, MD
20899 United States

Contact: Herbert S. Bennett
Phone: (301) 975-2053
FAX:

**SIA TECHNOLOGY WORKSHOP DOCUMENT DISTRIBUTION
TO NATIONAL LABS AND AGENCIES**

DOCUMENTS: "Semiconductor Technology Workshop Conclusions"
"Semiconductor Technology Workshop Working
Group Reports"

KEY: C - Recipients of Conclusions only
B - Recipients of both documents
P - Recipients of document/s with Andrew A. Procassini
(SIA President) cover letter
W - Workshop participants - received both documents with
Gordon E. Moore (Chairman, Intel Corporation and
SIA Technology Committee Chairman in 1992) cover letter

National Labs (and DOE Affiliates):

- ✓ Ames Laboratory -
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- ✓ Ames Research Center -
Dale L. Compton (BP)
- ✓ Argonne National Laboratory -
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- ✓ Battelle Pacific Northwest Laboratory -
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- ~~✓~~ Bettis Atomic Power Laboratory -
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The Honorable Robert B. Reich (BP)

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- ✓ Ronald D. Larrabee (B)
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**SEMICONDUCTOR INDUSTRY ASSOCIATION**

4300 Stevens Creek Boulevard • Suite 271
San Jose • CA 95129 • (408) 246-2711

FAX (408) 246-2830

June 11, 1993

Date Rec'd 6/14

ACTION to _____

INFO to JohnNelsonBudjako

The Honorable John H. Gibbons
Assistant to the President for Science and Technology
Old Executive Office Building
Room 424
17th Street and Pennsylvania Avenue, N.W.
Washington, DC 20500

SIG of _____

Stationery _____

DATE DUE _____

Dear Dr. Gibbons:

On behalf of the Semiconductor Industry Association (SIA) we appreciate the opportunity to submit a nominee for the High Performance Computing Advisory Committee. His name is Justin R. Rattner, Director of Technology for Intel Corporation's Supercomputer Systems Division. Mr. Rattner's biography is attached.

Sincerely,

A handwritten signature in dark ink, appearing to read "A. A. Procassini", with a long horizontal flourish extending to the right.

A. A. Procassini
President

Justin R. Rattner

Justin Rattner, 45, is founder and Director of Technology of the Supercomputer Systems Division of Intel Corporation. He is also co-principal investigator for the Intel-ARPA TeraFLOPS research project. The expected result of this program is a technology base for affordable TeraFLOPS computing systems in the 1995-1996 timeframe. From 1989 through 1991, he was principal investigator for the Touchstone project, an earlier Intel-DARPA joint R&D project in scalable, high performance computing systems in 1991. The Touchstone DELTA system, the world's fastest computing system in 1991, was among the many technical achievements of this program.

In 1989 Mr. Rattner was named Scientist of the Year by R&D Magazine in recognition of his contributions to scalable, parallel computing systems design. He has been with Intel Corporation for 19 years. In 1988 he was named an Intel Fellow, the company's highest ranking technical position, for his pioneering work in microprocessor and supercomputer systems design. He is the fourth of only eight Fellows named in the Company's 25-year history.

Mr. Rattner received his B.S. and M.S. degrees in electrical engineering and computer science from Cornell University in 1970 and 1972, respectively.

6/93



SEMICONDUCTOR INDUSTRY ASSOCIATION

4300 Stevens Creek Boulevard • Suite 271
San Jose • CA 95129 • (408) 246-2711

FAX (408) 246-2830

facsimile

number of pages: 3

June 14, 1993

TO: The Honorable John H. Gibbons (202/395.3719)

cc: Mike Nelson

FR: Daryl G. Hatano

RE: High Performance Computing Advisory Committee

(3) Semiconductor Crosscut:

- **As they are aware, an Electronics Working Group has been established under the FCCSET PMES Committee and has begun meeting in the past two months.**
- **The industry associations, including SIA, recently sent a letter to Gibbons supporting an Electronics Cross-cut. We appreciate their interest and are considering how to best proceed with such an activity.**
- **The scope of the committee, and any cross-cut developed (formal or informal) will include electronics broadly, not just semiconductors.**
- **Electronics may be included as a sector called out in the manufacturing cross-cut and initiative.**
- **The Electronics Working Group has been meeting with a number of industry associations. The SIA has been an active participant, and has shown leadership in preparing their roadmap and developing priorities.**

(4) Technology and Business Issues:

- **SIA will present technology strategies in their five priority areas: lithography, packaging, modeling and simulation, metrology and sensors, and contamination-free manufacturing.**
- **The policy level committee (i.e. Johns/ Deutch) is not the appropriate group to consider these, so we need not comment on the technology issues presented.**
- **Consideration needs to be given to government's role not only in technology development, but in working with industry to achieve commercial success and viable businesses as well.**
- **The conference call two months ago did not produce an industry consensus that a complete domestic supplier base was essential - is this an accurate picture?**

DEWEY BALLANTINE

1775 PENNSYLVANIA AVENUE, N.W.

WASHINGTON, D.C. 20006-4605

TELEPHONE 202 862-1900 FACSIMILE 202 862-1098

Date Rec'd 6/22
ACTION to S. Johns
INFO to Nelson
SPB

6/21

This copy to JHG
via Mark Hartney.

W. CLARK MCFADDEN, II
202 459-2583

June 3, 1993

They are inviting

JHG =

it's on

Deutch's calendar = may be
held in his office.

SIG of _____
Stationery _____
DATE DUE 7/2

The Honorable John M. Deutch
Under Secretary of Defense for
Acquisition and Technology
The Pentagon, Room 3E933
Washington, D.C. 20301-8010

Dear Mr. Under Secretary:

Note: JHG will not do. Asking
Skip of ~~Mike~~ Mike N. to handle

As part of a new initiative growing out of the recommendations of the National Advisory Committee on Semiconductors, the semiconductor industry and the U.S. government are seeking new ways to work together in technology development. One such measure is the statutory creation of a new type of council that would include senior representatives from industry, government, and academia, and would be co-chaired by you and an individual designated by the Semiconductor Industry Association ("SIA").

The proposed council would provide a regular forum for exchanging information and would focus on the recently developed National Roadmap for Semiconductor Technology. When this subject was raised with Deputy Secretary Perry, he supported the concept of the council and recommended a meeting with you.

In order to discuss the proposed council legislation and begin a dialogue on technology issues, SIA would like to request a meeting with you at 2:00 p.m. on Friday, July 16, 1993. Attending the meeting would be several senior officials of U.S. semiconductor firms led by Craig Barrett, Chief Operating Officer of Intel Corporation and Chairman of SIA's Technology Strategy Committee.

Thank you for your attention. We look forward to hearing from you.

Sincerely,



W. Clark McFadden II
Counsel to the
Semiconductor Industry Association

POC: Lynn Chise
703-695-2381

River entrance
of Pentagon
courtesy

NEW YORK WASHINGTON LOS ANGELES

523-81
TO 93953719

EXECUTIVE OFFICE OF THE PRESIDENT
OFFICE OF SCIENCE AND TECHNOLOGY POLICY
WASHINGTON, D.C. 20506

*it'll go!
Thanks,
Skip*

June 16, 1993

MEMORANDUM FOR: SKIP JOHNS

SUBJECT: MEETING WITH JOHN DEUTCH AND SIA - JULY 16

FROM: MARK HARTNEY *mh*

The CEO-Under Secretary level meeting that the SIA is seeking has been set up as a meeting with John Deutch on July 16 from 2:00 to ~2:45 to discuss:

- The proposed Semiconductor Technology Council
- Issues related to model CRADA's
- The Electronics Crosscut Activities
- SIA Technology Recommendations in five areas:
 - Lithography, Packaging, Modeling, Sensors and Metrology, and Contamination-Free Manufacturing

The representatives from the SIA will include:

Gil Amelio, President of National Semiconductor, Chairman of SIA Board
Craig Barret, Exec. VP of Intel, Chairman of SIA Technology Comm.
Bill Spencer, CEO of SEMATECH
Larry Sumney, CEO of SRC
one or two other Industry CEO's who serve on the SIA Board.

Either you or Jack (or both) should attend this meeting if possible, since OSTP is to be represented on the Semiconductor Technology Council, we have been participating in developing the crosscuts, and we are trying to promote industry-government interaction of this type.

The SIA drafts of the technology recommendations were presented at a meeting this morning, and there were a number of issues which raised questions. They will continue to refine the proposals, working with government representation, prior to the meeting next month. The lithography proposal, in particular, has been somewhat contentious, even within the SIA Board.