National Semiconductor

G.F. Amelio
President and CEO

June 30, 1994

The Honorable Lionel S. Johns
Associate Director for Technology
Office of Science and Technology
17th Street and Pennsylvania Avenue, N.W.
Washington, D.C. 20500

Dear Skip:

Thank you for meeting with me on June 22, 1994 to discuss the Semiconductor Industry's (SIA) technology policy agenda. I enjoyed having the opportunity to share SIA's viewpoint on the issues that the industry believes are crucial to the nation's economic health and military preparedness.

I especially appreciated your sensitivity to the need for constant, longterm support by the U.S. Government for the Advanced Lithography program. As you know, SIA believes funding of this program at the historical levels of $75 million is a vital part of reaching the goal of maintaining a viable, world-class U.S producer of lithographic exposure equipment.

I also wanted to take this opportunity to express my gratitude for your contributions in helping to advance the formation of the Semiconductor Technology Council. SIA looks forward to having the opportunity to address future semiconductor technology issues in this industry-government forum.

If you have any additional questions regarding SIA's positions or would like to engage in further discussions, please do not hesitate to contact me.

Sincerely,

G.F. Amelio
President and CEO
Chairman, Semiconductor Industry Association (SIA)

cc: Kitty Gillman

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SIA SEMICONDUCTOR INDUSTRY ASSOCIATION

April 8, 1994

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Dr. John H. Gibbons
Director
Office of Science and Technology Policy
17th St. & Pennsylvania Ave., NW
OEOB, Room 424
Washington, DC 20500

Dear Dr. Gibbons:

On behalf of the Semiconductor Industry Association ("SIA"), I want to express my concern with the President's proposed fiscal 1995 funding for advanced lithography and recommend that funding for this program be restored to $75 million.

Advanced lithography is the key driver to each new generation of semiconductors and an area in which the United States continues to face intensive competitive pressure, particularly from the Japanese. In part because of the industry-government partnership that has developed over the past several years, the industry has made tremendous strides in restoring its competitive health with the U.S. semiconductor industry regaining worldwide market share leadership in 1993. However, the industry continues to lag in many critical aspects of lithography.

At stake is continued U.S. viability in a technology area that is vital to the United States' national security. The technological advantage of superior electronics enhances the performance of defense weapons and maximizes the efficiency of their application through sophisticated intelligence and command and control systems. Also, a strong domestic capability in advanced lithography and its associated infrastructure is essential to ensuring U.S. competitiveness across a wide range of industries and products, from automobiles to high-resolution displays to consumer electronics. In SIA's view, this capability will be necessary to realize the products and services that will constitute the now-emerging National Information Infrastructure.

The accompanying white paper entitled *Commercial Challenges In Microlithography* gives SIA's views in greater detail. These views are consistent with SIA's National Technology Roadmap for Semiconductors and the industry's historical support for ARPA's existing advanced lithography technology and infrastructure support programs. Further, the recently created Semiconductor Technology Council

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created in the National Defense Authorization Act for Fiscal Year 1994 serves as an immediate industry-government forum for addressing lithography issues in a cooperative manner.

A continued Advanced Lithography program is critical to the nation's economic health and military security. I strongly urge that funding for this program be restored to the historical level of $75 million.

SIA looks forward to working with you on this important effort. If you have any questions regarding SIA's position, please do not hesitate to contact me or SIA's Public Policy Chairman, George Scalise, at (408) 721-6539.

Sincerely,

GF Amelio

Gilbert F. Amelio
Chairman of the Board of Directors
Semiconductor Industry Association
and
President and Chief Executive Officer
National Semiconductor Corporation

COMMERCIAL CHALLENGES IN MICROLITHOGRAPHY

an industry perspective

by

The Semiconductor Industry Association

March 1994

SIA

COMMERCIAL CHALLENGES IN MICROLITHOGRAPHY
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Introduction

Electronics is the nation's largest and fastest growing manufacturing industry. By the end of the century revenues are expected to exceed $400 billion and this industry will employ more than 2.5 million Americans. This growth has, and will continue to be sustained through steady advancements in semiconductor manufacturing science and technology.

However, America's leadership position in this dynamic industry is not assured unless it achieves a leadership position in manufacturing technologies that control the pace in which future generations of electronic products emerge. Microlithography is one of the most essential of such technologies----one in which we are heavily dependent upon Japan.

While America was once the leading supplier of microlithography technology and equipment, supplying over 80 percent of the world's needs, this leadership position eroded rapidly following Japan's aggressive entry into world markets in the mid 1970s. By 1986, Japan was the world leader in semiconductors. Moreover, its markets were substantially closed to foreign suppliers of semiconductors.

It was in this environment that nine of 11 U.S. memory chip manufacturers were driven from the commodity memory market, capital spending by U.S. chip manufactures was sharply reduced, and our domestic semiconductor manufacturing equipment and materials suppliers suffered substantial, and often irreversible financial losses. It was in this period that we virtually lost our domestic microlithography industry.

Regaining leadership in microlithography will require investments by both the public and private sectors and the continued innovation of academia. Historically, both industry and defense have relied upon the Advanced Research Projects Agency (ARPA) for support of the most advanced research and development programs in microlithography, those that are beyond the capabilities of individual companies.

Today this support is threatened by the precipitous reduction in ARPA's 1995 budget for microlithography. The SIA urges Congress to restore this budget to at least $75 million annually. Industry needs this support to regain leadership in one of the most vital of electronics technologies---microlithography.

Background

Microlithography---the process by which circuits are printed on semiconductors---is the most costly and technically challenging of all semiconductor manufacturing processes. U.S. industry spends over $1 billion annually on lithography materials, equipment, and research and development.

The growth of the electronics industry is paced by advancements in circuit density and integration. Circuit density is determined by the size of the features that can be "printed" with the lithography process---smaller features mean higher density, higher performance and lower power consumption.

Historically, industry has been able to achieve a four fold increase in the number of transistors on a single chip approximately every three years. The cost of this progress has been high. Today, over 35 percent of the manufacturing cost of the chip results from the lithography process alone.

While this investment has succeeded in lowering the cost per function on the chip, and in fueling the explosive growth of the electronics industry, lithography costs are escalating rapidly. Unless present technologies are refined and new cost effective technologies developed in the future, industry's growth will be slowed.

In addition to the technical and economic challenges already outlined, the U.S. semiconductor and electronics industries face a strategic threat as well. **This threat is a result of the almost total dependency upon Japan for our lithography steppers, and our increasing reliance on that country for lithography support in areas of resists, resist processing equipment, metrology, and application development.**

To remove this dependency and once again achieve a leadership position in microlithography, U.S. industry must work with government and academia to maintain the momentum in technology development and adopt strategies that will lead to a U.S manufacturing base for future generations of this vital technology.

Trends in Lithography Technology

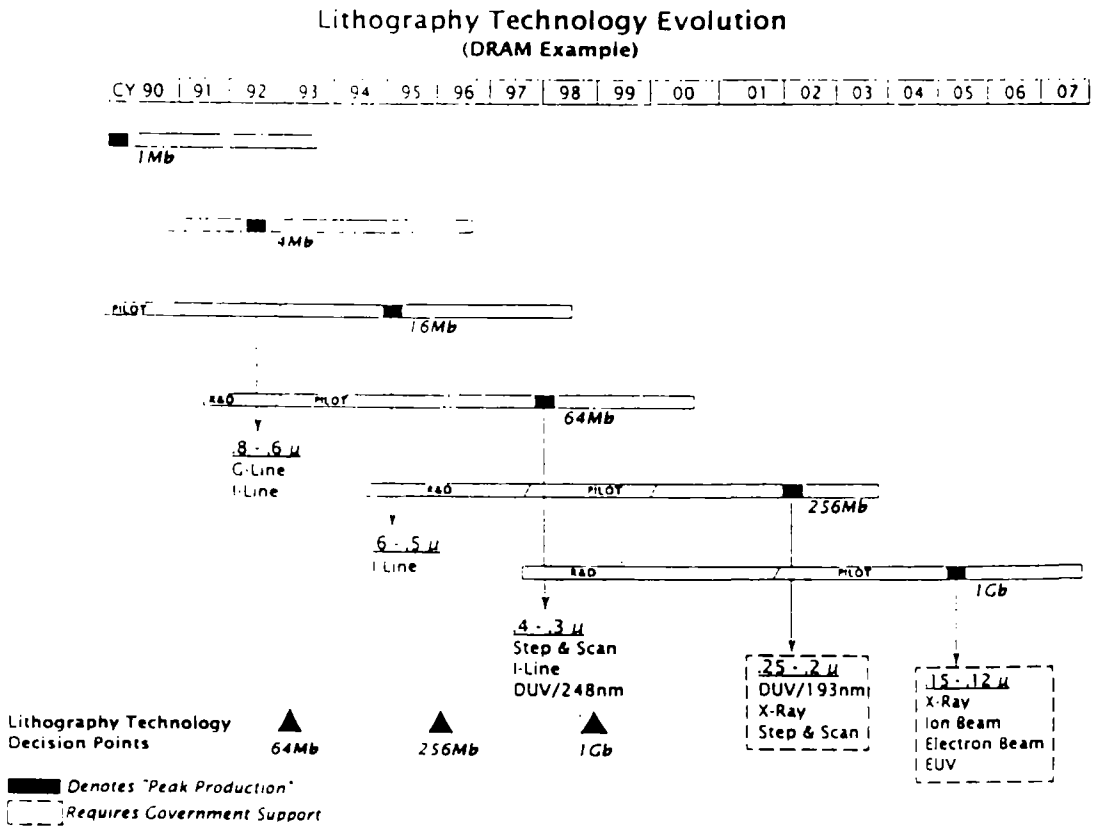
The factors that determine the lithography process are varied and complex. Optical lithography is the technology of choice today. However, the increasingly smaller print feature which is required is approaching the wavelength of the illuminating source---a limit that can be exceeded only with added complexity in optics and process. To keep this technology viable, industry is developing systems using shorter optical wavelengths.

Non-optical technologies seek to go beyond that which can be cost effectively achieved with optical systems. However, there exists both controversy and uncertainty regarding the specific product generation for which these non-optical approaches will find application.

To guide the industry in its choice of technology and to serve as a tool for making investment decisions in all areas of semiconductor manufacturing technology, the Semiconductor Industry Association has sponsored the development of a 15-year roadmap ---The **National Technology Roadmap for Semiconductors.**

The "roadmap" provides a framework to be used as part of an ongoing, iterative process to evaluate, in an objective manner, different lithography approaches. Using this strategy, a number of promising lithography technologies have been identified along with an estimate of the time frame and product generation for which they will find application.

Figure 1 relates identified lithography technologies with the time evolution of specific (memory) product generations. Starting at the beginning of this decade and extending past the turn of the century, chips with over 1 million transistors today will evolve to ones with over 1 billion transistors by 2005, providing lithography solutions become available on the time scale shown.



Using data from the roadmap Figure 1 provides an estimate of when each new

generation of chip will reach its production peak. (Note that respective generations are identified by the number of transistors on a single chip in millions. Mb. or in billions. Gb.) Also shown are the feature sizes that each generation will embody and candidate lithography technologies for achieving these feature sizes. The dotted boxes denote technologies having substantial uncertainty and risk and ones requiring public support at the pre-competitive level.

Optical technology is expected to prevail as the present 4Mb generation advances to 64Mb later in this decade. Today both G-Line and I-Line optical systems from Japan and Europe supply industry's needs. and will continue to do so through 1995.

The 64 Mb device which will achieve peak production levels in about 1998 will require substantial extensions of current I-Line technology or will require new advanced Step & Scan systems from SVG Lithography (SVGL) using a 248 nanometer optical source.

Beyond the 64 Mb generation, very advanced Deep Ultra-Violet (DUV) optical systems utilizing the 248-nanometer or 193-nanometer emission from the excimer laser. perhaps on an SVGL Step & Scan platform, or a non-optical source such as X-ray will be required. Extreme Ultra-Violet (EUV), or Electron and Ion beam technologies may be required past the turn of the century.

Also indicated in Figure 1 are the respective technology decision points that must be reached if a given technology is to find application in production. Typically, decisions concerning a specific lithography technology must be made almost five years before peak production levels occur. The decision point occurs during the R&D phase and prior to pilot line studies leading to full production qualification.

Implementation of the product roadmap as shown in Figure 1 requires that multiple lithography paths be pursued simultaneously. These paths range from the lower risk extensions of present day optical technology to high risk technologies that represent a complete paradigm shift from current practice. Failure to pursue these parallel R&D paths will place future product generations at risk. The economic impact of each product generation to the electronics industry is immense. While lithography research is expensive and complex, the leverage that it provides will be returned many times as each generation reaches fruition.

Optical Lithography: Current Industry Focus

Industry, in cooperation with Sematech, will maintain its primary focus during the next five years on extending optical lithography to 0.25 microns. In support of this goal, the Semiconductor Research Corporation (SRC) will sponsor research in advanced imaging materials with academia.

This extension will first be accomplished by improving the pattern transfer characteristics of I-Line systems through the use of phase-shift mask technology, off-axis illumination systems and multilayer resist processes. It is anticipated that these advancements will meet industry's needs through 0.35 microns.

Industry and government will also work to insure the successful completion of SVGL's Micrascan system including its adaptation to 248 nanometer and 193 nanometer excimer laser optical sources (DUV). This effort will include supporting programs in resist and mask development. It is anticipated that Micrascan, with its adaptation to DUV optical sources, will meet industry's needs through 0.25 microns.

Funding for the above programs will primarily be provided by industry and Sematech. Government support for 193 nanometer research, currently underway at MIT's Lincoln Laboratories, is appropriate to insure that this technology is successfully transferred to industry.

It is estimated that U.S. industry and Sematech will invest more than $180 million annually in lithography research and development during the next five years.

Advanced Lithography: ARPA Focus

ARPA's focus must include substantial support for high risk "**cross-cutting**" technologies that are common to all lithography approaches. In addition, it must continue strong support of **proximity X-ray** lithography and should provide research funding for long range (innovative) programs in **Electron and Ion beam** technologies.

Support of the cross-cutting technologies is essential to insure a strong U.S. infrastructure capable of sustaining a future domestic lithography industry. Mask development, repair and inspection are essential elements of this infrastructure. In addition, new resist formulations will be required to support all advanced lithography approaches. Finally, advanced precision stages and alignment systems must be developed to meet demanding alignment and pattern overlay requirements.

Proximity X-ray lithography holds the highest promise of near term success when industry makes the transition from an optical to a non-optical technology. Proximity X-ray utilizing the synchrotron x- ray source is being used today to fabricate VLSI integrated circuits. The anticipated industrial alliance of IBM - Motorola - AT&T represents an industry commitment to further this technology and insure that it will be ready for insertion into commercial manufacturing when required.

For manufacturing environments in which the synchrotron is poorly matched, such as those having low production volume requirements, Point-Source X-ray lithography offers a "granular" approach to meeting this need. Much of the infrastructure being developed in support of the synchrotron solution applies equally to point source technology. However, resources are required to continue the development of both laser-based and plasma- pinch point x-ray sources.

Finally, resources should be committed to further research on innovative long range lithography solutions such as Projection Electron Beam and Projection Ion Beam technologies. Should these technologies prove to be successful in the laboratory during the next several years, they would be candidates for manufacturing applications by the end of this decade.

Funding Priorities

The SIA recommends that ARPA's 1995 budget for advanced lithography be reinstated to the level of **$75 million**. Listed below, and in order of priority, are the programs and budget allocations that SIA believes will best serve its member companies and their suppliers. These programs, and the investments by industry and Sematech, offer the best approach to re-establishing world leadership in lithography technology and developing a secure U.S. manufacturing base.

1 Cross Cutting technologies: **$37M**
- * mask development, inspection, repair
- * mask writing
- * resist and processes
- * precision stages and alignment systems
- * mask shop
- * supporting 193 nm technologies

2 Proximity X-Ray Lithography / Synchrotron: **$25M**
- * device fabrication
- * support of industrial alliance
- * infrastructure

3 X-Ray Point Source Development: **$ 7M**
- * laser plasma sources
- * plasma pinch source
- * collimator

4 Advanced Technologies: **$ 6M**
- * electron beam
- * ion beam
- * EUV

Program Total **$75M**

45

Not included in the above listing are the EUV programs currently sponsored by the Department of Energy and metrology programs planned at NIST. The SIA supports these programs as outlined in its previous summary position paper.

Commercial Strategies: Industry Commitment

The SIA and its affiliates Sematech and SRC, are committed to working with U.S. semiconductor equipment and materials suppliers to achieve a viable long term U.S. source of advanced lithography processes and equipment and insure the creation of the infrastructure required to support this objective.

The industry realizes that it is unrealistic to set as a goal the attainment of U.S. self-sufficiency in lithography, at least during the present "optical era." At the same time it is unacceptable to fall behind in basic technology or to become totally dependent upon a single foreign country for either the technology or the manufacturing tools.

To meet its objectives, the semiconductor industry will adopt a phased approach, which will carefully consider the following realities:

* The lithography industry sector, while strategic, is small and will not support another entry using today's technology. Changing technology will provide the opportunity for future U.S. entry into world markets.

* The lithography industry is dependent upon large and on-going investments in R&D. These investments will exceed those which can be self-generated. Therefore external infusions of R&D support will be required. This backing should come from users, suppliers and government.

* A "stand-alone" domestic lithography industry must serve a world wide market to survive. This concept presently is not an option but it may be both desirable and necessary to enter into foreign alliances to achieve strategically meaningful level of participation. However, these alliances must be structured to preserve U.S investments and secure intellectual property rights in the event of dissolution of the alliance.

* Technology that has been funded by the public sector must be given special consideration to insure that it is not transferred to foreign entities under conditions that will provide enduring "advantage" to foreign competitors. However, technology sharing with foreign partners may be in the public interest as long as the United States' company receives at least as much benefit as its foreign partners. Under all circumstances, intellectual property developed under public sponsorship must benefit the United States.

Initial phase: In the initial phase, U.S. industry is committed to working with SVGL and assisting that company in implementing a domestic manufacturing base for serving both domestic and foreign markets for its Micrascan system, including receiving the transfer of manufacturing technology from Canon under the terms of the SVG-Canon joint licensing and distribution agreement.

This proposed agreement will provide SVGL with capital and manufacturing technology needed to manufacture and supply 50 percent of the world demand for all Micrascan systems including 248nm and 193nm embodiments. While this agreement will not provide entry to the Japanese market, it will achieve a very major objective—**removal of the United States' strategic dependency upon Japan for its optical lithography manufacturing equipment**.

Further, the agreement insures that the benefits of all improvements to Micrascan made by either SVGL or Canon flow equally to both partners and that machines manufactured in the U.S. and in Japan conform to a common standard. This will insure that U.S. companies with foreign operations will be able to adopt a uniform manufacturing process regardless of the source of their Micrascan machines.

Industry and Sematech will support SVGL by benchmarking advanced equipment, evaluating equipment and processes against critical technology milestones and capital productivity criteria and by purchasing equipment both for evaluation and for their production facilities. Moreover, industry will provide working capital in the form of advanced payments for delivery of equipment.

SIA member companies' R&D investments in SVGL and commitments to purchase Micrascan systems, to date, substantially exceed $100M. Further, SVGL has obtained equipment purchase commitments from foreign customers. It is anticipated that purchase commitments by both U.S. and foreign customers will grow in the near future.

In the event that the SVG alliance with Canon weakens, or a default occurs, industry is prepared to consider measures as appropriate to preserve this asset within the United States. Such measures may include loan guarantees, equity investment, progress payments, and other forms of support as long as SVG remains a U.S controlled corporation.

The SVG-Canon alliance awards no preemptory rights to Canon to either acquire equity in SVG, provide SVG with additional investment capital, or acquire exclusive rights to technology shared by the alliance or technologies that are beyond optical based Micrascan.

Later phase: In this phase the semicoductor industry and its users and suppliers will strive to achieve a U.S. solution to a domestic source of advanced lithography technology. Proximity X-ray is a candidate. SVGL, under ARPA sponsorship, is presently developing a stepper for this technology which will not be part of the Canon alliance.

Ultratech Stepper could also become a supplier of advanced platforms. This company is presently working with the national laboratories on the development of EUV lithography. Sandia National Laboratory is also working on the development of innovative magnetic stage technology.

Future lithography technologies such as electron and ion beam technologies, also outside of the Canon agreement, will benefit from these U.S. manufacturers' efforts to develop advanced stepper platforms.

Summary

Most industrialized countries place semiconductors high on their list of critical technologies for national security and economic growth. In order to establish and maintain leadership in the semiconductor industry, these countries will strive to achieve an independent manufacturing infrastructure with competitive domestic products, processes, equipment, and materials.

At this time only Japan has achieved this objective. The United States is the perennial technology leader but has been unable to sustain manufacturing leadership. This generality is particularly applicable to lithography. Japan currently enjoys more than 80 percent of the world market for steppers.

What are the lessons learned and strategies needed to win? Up to now the United States has been at a disadvantage competing with the well-orchestrated administrative guidance of MITI and the keiretsu structure of the Japanese industry in financing technology development and capital growth. The U.S. government and industry must do a more effective job of coordinating activity in high risk research, equipment development, and commercialization to enable timely insertion to meet market demand.

The actions set forth above are a first step in a deepening industry commitment to insure a long term and stable American presence in the most vital of semiconductor manufacturing technologies---microlithography.

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Strategy for lithography

Topic for TRP?
but it's cost share

masks, Risks, X-ray

Sia 75
others 50-75

SIA Ed. / Manuf / Quality / Tech / Taking Gordon Moore's place IBM Nat'l Semi C.

prediction Japan getting over to stop the reversal of of market share change

Japanese position no numbers

SIA believes 20% is the minimum number to

Trade issues

15 areas -
2 objectives - *1. on going forum to revise roadmap. -
2. Policy level - a council where academic / Govt / industry
Create council & meet periodically

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CPI ← Fellowships
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3YR

EXECUTIVE OFFICE OF THE PRESIDENT
OFFICE OF SCIENCE AND TECHNOLOGY POLICY
WASHINGTON, D.C. 20506

April 1, 1993

MEMORANDUM FOR: SKIP JOHNS

SUBJECT: SIA

FROM: MARK HARTNEY MH

The SIA Public Policy Committee is meeting next Tuesday in D.C. One of their agenda items is how to get a mechanism for industry and government interaction to implement their roadmap findings. At a meeting this morning, they proposed four different routes:

1. Establish an "Implementing Council" as opposed to an advisory council, comprised of government and industry members. If it is not an advisory council, it may be FACA exempt.

2. Take an existing council, most likely the **Advisory Council on Federal Participation in SEMATECH**, and recharter it to encompass a broader vision as outlined in the SIA roadmap. The **National Advisory Committee on Semiconductors** might also be a possibility but it has been disbanded, and may have been sunsetted.

3. Have OSTP establish a council on it's own.

4. Legislate a new council, potentially through CTI.

I informed them of the FCCSET Interagency Working Group on Electronics that was being formed, and suggested that might be a fifth option to work with. I believe that this could be done at SIA's invitation even on a regular basis and still be FACA exempt.

They would like to move beyond the advisory and reporting role and move towards an implementation approach. SIA members of the technology advisory board don't want to create another NACS, which they viewed as ineffective.

They have talked with Bingaman's staff about reworking the SEMATECH Advisory Council, and gotten a warm response. As you know, Bingaman is very supportive of the SIA's strategic approach. Nick Naclerio, who is the SEMATECH program manager for DARPA, and he seems to think that the scope of the advisory board could be broadened, and that it might be a natural thing to do as SEMATECH expands their technical scope.

Urgent: **XX** Routine:

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(408)246-2711

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Date: July 2, 1993 #Pages Including Cover: 5

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STATE: Ned Saums

Cc: Craig Barrett, Intel
John Deutch, DOD
John Gibbons, OSTP
Clark McFadden, Dewey Ballantine
Andy Procassini, SIA

From: Warren Davis

Subject: Craig Barrett Letter to John Deutch and John Gibbons

SIA SEMICONDUCTOR INDUSTRY ASSOCIATION
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July 1, 1993

The Honorable John M. Deutch
Undersecretary of Defense for
Acquisition
Department of Defense
The Pentagon, Room 3E-933
Washington, DC 20301-3010
FAX: 703-696-4268

Dr. John H. Gibbons
Assistant to the President for
Science & Technology Policy and
Director, Office of Science & Technology Policy
Old Executive Office Building, Room 424
17th Street & Pennsylvania Avenue, NW
Washington, DC 20500
FAX: 202-395-3719

Dear Drs. Deutch and Gibbons:

In anticipation of an SIA delegation meeting with you at 2:00pm on 16 July at the Pentagon, I am writing to explain the purpose of our visit as well as to suggest objectives. A list of industry participants from SIA, SEMATECH and SRC is attached.

Following the advice of the National Advisory Committee on Semiconductors, the SIA sponsored a three-day conference last November to create a unified national technology strategy for semiconductors. The two objectives were (a) to achieve technological leadership in world competition and (b) to do so without increasing aggregate expenditures for semiconductor research. Nearly 200 technical experts were invited from industry, government, and academia to construct a series of semiconductor technology roadmaps to the year 2007. The participants also identified broad technical and economic challenges which cut across several technologies.

Reports of the conference findings and recommendations have been broadly distributed. There is ample anecdotal evidence that these reports are being used as a baseline for research planning in labs throughout the nation. The conference reports have also formed the basis for a major new CRADA between SEMATECH and the Sandia National Labs as well as a broad new agreement between Sandia and NIST.

The SIA, SEMATECH and SRC have extensively revised their programs and priorities to address the national technology strategy for semiconductors. The SIA is prepared to monitor and update the roadmaps. SEMATECH and SRC have broadened their charters, e.g., SEMATECH is addressing the semiconductor packaging issue without increasing its budget.

SEMATECH and SRC are revamping their advisory board structures to accommodate the roadmaps and to provide increased synergy between the two consortia. Shortly, the two semiconductor consortia will be inviting government representatives to integrate into the revised advisory structures.

During the past several weeks, there has been a series of Washington roundtables bringing together the semiconductor industry and government (DOD, DOE, DOC, NSF, OSTP, and NEC) to discuss the structure and strategy for implementation of the technology strategy. Topics covered have included:

- Formation of a new Semiconductor Technology Council to be co-chaired by industry and government (substitute for SEMATECH Oversight Committee) to provide broad policy guidelines for the program long term.

- Creation of a model CRADA for the industry (5 CRADAs are now under negotiation between SRC and the Federal labs). Restrictions on foreign manufacturing have prevented closure thus far.

- Obtaining a crosscut of U.S. government semiconductor research activity (OSTP FCCSET process) as a basis for realigning resources.

- Setting technical priorities in lithography, semiconductor packaging, contamination free manufacturing, metrology and sensors, and modeling and simulation. (The establishment of a national lithography strategy is the foremost challenge).

With the above background, I would like to suggest the following objectives for the July 16 meeting:

- Agreement on formation, composition, and mission of the Council. Schedule first meeting.

- Approach to resolve remaining disincentives to private sector cooperative alliances with Federal labs, including CRADA restrictions.

- Agreement to proceed with a FCCSET crosscut for semiconductors on a priority basis.

- Mutual understanding of overarching technology and business issues.

If you have comments on any of the above, including the meeting objectives, please do not hesitate to contact me (Phone: 602-554-5977, FAX: 602-893-7755) or Clark McFadden, SIA counsel at Dewey Ballantine (Phone: 202-429-2333 or 2319, FAX: 202-862-1093).

My colleagues and I sincerely look forward to our upcoming discussions and to the beginning of a long term cooperative relationship.

Sincerely,

Craig R. Barrett
Executive Vice President &
Chief Operating Officer
Intel Corporation
and
Chairman
SIA Technology Strategy
Committee

cc: Clark McFadden, Dewey Ballantine
A. A. Procassini, SIA President

7/1/93

GOVERNMENT/INDUSTRY MEETING
WITH UNDERSECRETARY DEUTCH (DOD) AND
PRESIDENT'S SCIENCE ADVISOR GIBBONS
THE PENTAGON
FRIDAY, JULY 16 1992, 2:00PM

INDUSTRY REPRESENTATIVES

Chairman, SIA Technology Strategy Committee:

Craig R. Barrett
Executive Vice President & Chief Operating Officer
Intel Corporation

Colleagues:

Dr. Gilbert F. Amelio
President & CEO
National Semiconductor Corporation
and
Chairman, Semiconductor Industry Association (SIA)

Dr. Michael J. Attardo
IBM VP & General Manager, Technology Products
IBM Corporation

Dr. William Siegle
VP & Chief Scientist
Advanced Micro Devices, Inc.

Dr. William J. Spencer
President & CEO
SEMATECH

Larry Sumney
President
Semiconductor Research Corporation (SRC)

Staff:

Dr. David Beecham
Industry Relations Director
AT&T Microelectronics
and
Technology Program Chairman, SIA Public Policy Committee

Clark McFadden
Partner
Dewey Ballantine

EXECUTIVE OFFICE OF THE PRESIDENT
OFFICE OF SCIENCE AND TECHNOLOGY POLICY
WASHINGTON, D.C. 20506

July 16, 1993

MEMORANDUM FOR: SKIP JOHNS, KITTY GILLMAN

SUBJECT: TALKING POINTS FOR SIA MEETING WITH DEUTCH

FROM: MARK HARTNEY

SIA has proposed four topics for the agenda for this afternoon's meeting:

(1) Semiconductor Technology Council:

- OSTP supports the idea of the council and the mission of the group to bring industry and government together, where possible, to work towards implementation of the roadmap. Broadening the scope of the SEMATECH advisory council is the appropriate way to accomplish this.

- OSTP will not support a FACA exemption for the committee, since we are charged with reviewing the FACA legislation. We do not want to solve the problems with FACA by issuing exemptions in the interim while working on the broader problem.

- Despite industry's concerns, this administration will provide a more favorable environment than the Bush administration did for the NACS committee.

- There is a need for government-industry interaction at several levels - this committee is at the highest policy level, but discussions are needed at the laboratory division and program director level as well.

(2) CRADA issues:

- SIA's biggest concern is the restriction of CRADA's to firms which do a majority of their manufacturing in the U.S.

- They would also like to establish a "blanket CRADA" to work with the labs, much like the CSPP has.

- This is primarily a DOE concern - OSTP would like to see the process move more rapidly, but wants to insure that the benefit of laboratory technology accrues in the U.S.

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TECHNOLOGY POLICY:

LITHOGRAPHY

OCTOBER 1, 1993

TECHNOLOGY POLICY: LITHOGRAPHY

The successful development of semiconductor technology will greatly affect the competitiveness of the U.S. semiconductor industry and the prosperity and security of the nation.

Lithography, and more specifically exposure tools, is a technology challenge of overriding national importance.

A sound technology approach to this challenge should be based on the realities confronting exposure tools, especially the economic and international market requirements.

In the near term, a sound technology approach should also focus on the principal remaining leading edge U.S. technology for optical exposure tools--the Micrascan technology. This technology is currently undergoing production level evaluation by U.S. device companies and appears to be on the threshold of major commercial acceptance by the worldwide semiconductor industry.

Based on the commercially viable Micrascan technology, supplemented by its licensing arrangement with Canon, SVGL has reached a level of maturity which takes it well beyond the R&D phase to the market phase. SVGL can become a world leader in exposure tools and represent a major achievement for the U.S. industry and the nation.

Finally, a successful national technology policy should recognize the long-term uncertainties inherent in the development of alternatives to optical lithography. Because no clearly dominant technology has emerged, competing technologies should continue to be pursued and funded in a balanced program.

EXPOSURE TOOLS RELY ON OTHER TECHNOLOGY

Semiconductor technology spans a broad range from product design and manufacturing processes to production tools and equipment. Lithography is the central technology for the volume manufacturing of semiconductors, accounting for approximately 35% of the cost of a processed wafer.

The principle areas of lithography technology consist of exposure tools, masks, photoresist materials and processing, and metrology. While exposure tools represent the core capability, these areas are interdependent and hence should not be viewed in isolation.

The current funding of lithography by both government and SEMATECH reflects the significance of technology development in areas other than exposure tools. Optical exposure tool programs are well under half the total for related lithography areas. The success of any exposure tool development will be closely tied to developments in other lithography areas.

THE BUSINESS CONTEXT

The U.S. share of the world market for exposure tools has steadily dropped since 1987 and is now approximately 10%. High capital requirements, short product life cycles and entrenched competitors have led to a steady decline worldwide in the number of exposure tool manufacturers, Hitachi and GCA being the latest companies to depart. Because major semiconductor producers have facilities deployed globally, an exposure tool producer must have the resources to operate in all markets worldwide. The purchasing patterns and servicing requirements for each new generation of exposure tools place a premium on the credibility of the tool maker. In these circumstances, there may be room for only a few suppliers of exposure tools.

At the same time, these sweeping technological, financial and market demands greatly increase the pressure for collaboration across the board, including among exposure tool manufacturers. Similar to the electronics and semiconductor industries, equipment suppliers increasingly find that they must cooperate and compete with foreign firms. To exploit its technology fully, a firm must often be prepared to make it available to others for commensurate benefits. A successful technology policy--whether for a company, an industry or a nation--must be able to accommodate this reality.

MICRASCAN TECHNOLOGY

Micrascan technology, through SVGL and its predecessor, Perkin-Elmer, has benefitted from government R&D support. SEMATECH, a government/industry organization which funds the development of semiconductor equipment, has also worked to provide direction and improvement to the technology.

Micrascan technology has all of the features that could enable it to support the next generation in optical lithography:

- It currently operates at 0.35 microns and is readily extendable to 0.25 microns; and

- It has successfully completed rigorous, "best of breed" trials through SEMATECH and has been deemed ready for commercialization.

Four major semiconductor suppliers from the United States, Japan and Korea have placed orders with SVGL for units using the Micrascan technology, and three others are evaluating the Micrascan technology--two of which are expected to place orders in the near future.

Through ARPA's Advanced Optical Exposure Program, the Micrascan technology is extendable to 193 nanometers. This means that it should be in a position to compete for optical exposure tool sales into the next decade.

VIABILITY OF SVGL

To be in the winner's circle in 1995, SVGL will need more than pre-eminent technology. It will need the financial resources, market access and manufacturing prowess that are essential to survive in the global market. The most difficult of these hurdles is developing the ability to manufacture reliably in high volumes.

The SVGL licensing arrangement with Canon will address the concerns listed above:

- SVGL will receive royalty and licensing payments from Canon for technology sharing;
- SVGL will gain access to the Japanese market for its technology through sales by Canon;
- Canon will provide manufacturing technology to SVGL; the licensing arrangement for manufacturing seeks to ensure interchangeability of parts and processes; and
- At least one-half of the manufacturing will be done in the United States.

SEMATECH will work with SVGL to ensure transfer of manufacturing technology from Canon to SVGL's facilities in the United States. SEMATECH's Board of Directors unanimously supports the SVGL/Canon alliance and will work with SVGL to help it succeed.

All of these measures, plus the continued testing and evaluation by U.S. and foreign device firms, provide the best prospects for SVGL to commercialize the Micrascan technology. If it succeeds, the Micrascan technology will become a world standard, and SVGL will become a major force in the U.S. equipment infrastructure.

LONG-TERM CHALLENGES

In the long-term as the semiconductor industry moves from an optical exposure method to a new lithography technology, the United States will have an opportunity to take the global lead in lithography manufacturing.

- Prioritized funding should be maintained for next-generation lithography programs to permit adequate exploration and critical reviews of the competing alternatives.
- The diversity of federal funding for fiscal year 1994 reflects the multi-dimensional nature of next-generation lithography R&D. More than one-

half of all federal funds are designated for exploring long-term, next-generation alternatives to optical exposure system technologies.

- Industry and government should articulate a strategy for facilitating commercialization, with a focus on areas of common concern and shared R&D risks. This should include methods for providing effective technology transfer to users and tool manufacturers.

COMMON INTERESTS AND CHALLENGES

Government and industry have a stake in the successful development of exposure tools. In particular, they have a common interest in having lithography technology:

- Developed by U.S. companies in the United States;
- Available readily to U.S. device companies; and
- Resident in the U.S. infrastructure of equipment suppliers.

Government/industry cooperation in technology development, coupled with a strong trade policy, have been major contributors to the recapture of world market share leadership from Japan for both the semiconductor industry and the equipment industry. The industry turnaround has assured a domestic technology base and a supply of advanced semiconductors in support of both the commercial and security interests of the United States.

Despite this overall improvement, little ground has been gained with respect to exposure tools. The problem has not been technology.

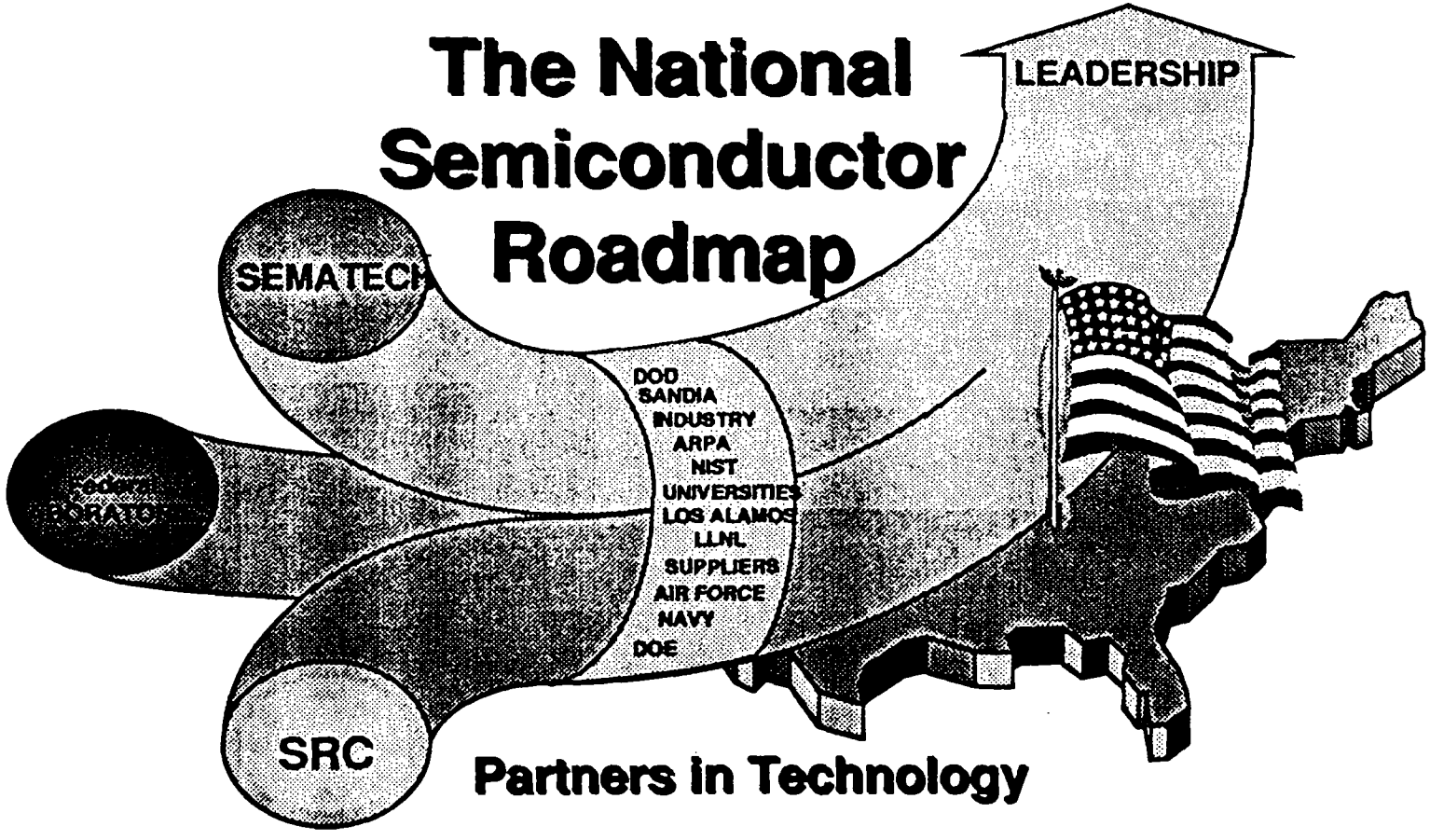
SVGL represents the principal remaining producer of leading edge optical exposure tools in the United States. There are several steps that could be taken to strengthen its prospects regarding the Micrascan technology:

- Continuing efforts by SEMATECH and the government as necessary to refine the technology;
- Careful scrutiny of the terms of the SVG/Canon arrangement to ensure that the technology is appropriately protected;
- Support from SEMATECH with respect to tool qualification and quality assurance; and
- Focusing attention on Canon's compliance with the terms of the SVG/Canon arrangement.

All producers of exposure tools face major risks, and no guarantees can or should be provided to SVGL. By focusing on Micrascan and SVGL in conjunction with an overall lithography program, government and industry can greatly facilitate SVGL's chances to succeed. In this way government and industry can also advance their common interests.

OCTOBER 1, 1993

SIA Proposal On Roadmap Needs



SEMICONDUCTOR ROADMAP NEEDS

- **Summary of Proposals:**
  - **Continue to Fund and Strengthen Current Programs**
    - **SETEC at Sandia National Laboratory**
  - **Continue to Fund and Expand Current Programs**
    - **Multi Chip Module Under ARPA**
    - **Center for Microelectronic Technology at Sandia**
    - **Lithography Program Under ARPA**
  - **Establish New Programs**
    - **Center for Semiconductor Metrology at NIST**
    - **Center for Simulation & Modeling at Los Alamos**
    - **Semiconductor Equipment Design Center at Sandia**

SEMICONDUCTOR EQUIPMENT TECHNOLOGY CENTER (SETEC)

- The SETEC Program Was Started in Mid-1989 in Support of SEMATECH to Improve the Competitive Position of the U.S. Semiconductor Equipment Industry.

- The Program Focused on Three Goals:
  - Improve Equipment Reliability;
  - Develop Diagnostic Techniques for Monitoring Processes and Adapt These Techniques to Improved Process Control; and
  - Develop Models for Describing and Optimizing Manufacturing Equipment Design and Processes.

MULTI CHIP MODULE PROGRAM

- This is a Funded Program.

- SIA Proposes to Continue and Expand This Program ($25 Million/Year)
  - To Support the Broader Packaging Areas With a Greater Emphasis on Commercial Opportunities, and
  - To Develop a Supporting Supplier Infrastructure.

CENTER FOR MICROELECTRONIC TECHNOLOGY

- **Center's Objective is to Support the SIA Technology Roadmap By Providing a Beyond State-of-the-Art Semiconductor Processing Facility For Use by Industry,Government Laboratory, and University Participants.**

- **The Facility Will Bridge the Widening Gap Between Advanced Research and Competitive Industrial Production by Supporting:**

  - **Development and Evaluation of Advanced Integrated Circuit Processing Equipment;**
  - **Benchmarking of Foreign Equipment and Establishing Competitive Evaluations;**
  - **Advanced Metrology for Qualifying Equipment and Processes;**
  - **Contamination Free Manufacturing Improvements;**
  - **Development of Advanced Sensors for Process Control and Contamination Detection;**
  - **Environmentally Conscious Manufacturing Through Effluent Monitoring and Control;**
  - **Special Testing and Evaluations of Device Structures and Circuits; and**
  - **Manufacturing Demonstration of Advanced Process or Equipment Concepts.**

CENTER FOR MICROELECTRONIC TECHNOLOGY

- **Key Project Deliverables Include:**
  - **Process Technology Modules;**
  - **New Processing Equipment;**
  - **Improved Product Manufacturing Efficiencies and Yields Resulting from Equipment Improvement;**
  - **Reduced Environmental Waste; and**
  - **Specific Solutions to Equipment, Processing, and Metrology Problems.**
- **This is a Funded Program.**
- **SIA Proposes to Continue and Expand This Program ($5 Million/Year) to Allow Additional Characterization of Research Concepts.**

ARPA's Lithography Program

- **Recommended Specific Near-Term Actions:**
  - **This is a Funded Program.**
  - **SIA Proposes to Continue and Expand Funding and Support for Optical Lithography at < 200 nm ($3 Million/Year) to Include Research and Development in the Areas of:**
    - **Resist Materials and Processing;**
    - **Optical Materials; and**
    - **Mask Processing.**

- **Future Activities:**
  - **Usefulness of Optical Lithography Continues**
  - **Optical Lithography Life is Finite**
  - **Funding of Multiple Technologies is Appropriate**

CENTER FOR SEMICONDUCTOR METROLOGY (CSM)

- The Establishment of a Government-Sponsored Center for Metrology is Proposed to Provide the Critical Metrological Technology Needs Expressed in the National Semiconductor Roadmap.

- This is Not a Funded Program.

- SIA Proposes That This CSM Program Be Funded at NIST for $25 Million in 1995 and Started in 1994 if At All Possible.

Semiconductor Modeling and Simulation

- **Needs:**
  - Characterization of Models
  - Integrated Knowledge Base to Support Models
  - Advanced Simulation Techniques

- **Purpose:**
  - There is an Important Need for a Center-Level Effort With a Focus on Modeling and Simulation and its Applications to the Full Spectrum of Semiconductor Needs.

SUMMARY OF PROPOSALS

	Suggested Annual Funding Increases
♦ **Continue to Fund and Strengthen Current Programs**	
▸ SETEC at Sandia National Laboratory	
♦ **Continue to Fund and Expand Current Programs**	
▸ Multi Chip Module Under ARPA	$25M
▸ Center for Microelectronic Technology at Sandia	$5M
▸ Lithography Program Under ARPA	$3M
♦ **Establish New Programs**	
▸ Center for Semiconductor Metrology at NIST	$25M
▸ Center for Simulation & Modeling at Los Alamos	$10M
▸ Semiconductor Equipment Design Center at Sandia	$12M
♦ **TOTAL**	$80M

SIA 10/01/93 1:13

January 13, 1993

MEMORANDUM FOR Ron Brown
Hazel O'Leary
William Perry
Neal Lane

FROM John H. Gibbons

SUBJECT Event to highlight government-industry cooperation in microelectronics

On March 2 and 3, 1994, CEOs and senior executives from U.S. semiconductor manufacturing firms such as Intel, Motorola, and Texas Instruments will be in Washington for the annual meeting of the Semiconductor Industry Association (SIA). This gives us a good opportunity to highlight the Clinton Administration's wide-ranging activities for government-industry cooperation in microelectronics. The overall magnitude of activities in this area is masked by their dispersal across various agencies and firms. We can make it much more visible by focussing on the whole activity at one time and place. Therefore, I suggest that we prepare an event to take place during the SIA annual meeting, to include industry CEOs and Cabinet and subcabinet officials from the key agencies, at which government and industry could announce:

- Formation of the Semiconductor Technology Council, as called for in the FY 1994 Defense Authorization Act;
- An intent to cooperate in at least some of the areas designated as priorities in the SIA technology road map, such as metrology, modeling and simulation, and packaging; and
- Major cooperative research and development agreements that will have been completed by March 1.

We can also take this opportunity to bring up with industry representatives issues that need discussion and debate -- for example, the desirable degree of cooperation in research priorities. The semiconductor industry has done an excellent job of describing their long-term needs, and the SIA roadmap provides a rich menu for possible areas of collaboration. However, collaboration does not require that government agencies fund a research agenda dictated by industry, since government research needs will not always coincide with those of industry. In particular, government R&D investments may need to promote paradigm shifts in microelectronics rather than focusing on evolutionary progress. Another issue is the need for two-way communication, from industry to government as well as government to industry.

Kitty Gillman of the OSTP Technology Division (tel. 202-395-6175) will be calling your office within the next few days to discuss the form the event should take and how your agency may wish to participate. I would greatly appreciate your help in assuring that important projects being planned by your agency can be ready for announcement by March 2. We can also announce at that time agreements already concluded and activities underway throughout the Clinton Administration's first year.

The principal theme of the proposed event is that government-industry cooperation can strengthen U.S. competitiveness. Although U.S. market share in semiconductors and semiconductor manufacturing equipment fell steadily throughout most of the 1980s, U.S. industry had by 1993 recaptured a position of world leadership. Part of this resurgence can be attributed to SEMATECH, and to efforts by the U.S. Government to open the Japanese market.

Presentations at the event could include such major government activities as NIST's shaping of its electronics metrology program to meet needs identified in the SIA road map and assigned top priority by the SIA; the 5-year $100 million-plus cooperative research and development agreement (CRADA) signed last year by DOE's Sandia National Laboratories and Sematech on high priority microelectronics projects, such as materials and manufacturing process modeling and contamination-free manufacturing; and ARPA's $100 million program of cooperative projects with industry to develop multi-chip modules--another top item on SIA's technology agenda.

The event would also provide the impetus and opportunity to get additional cooperative programs underway by March 1, such as conclusion of the $150 million 5-year CRADA between DOE labs and several semiconductor companies and equipment companies to develop radically new lithographic tools for semiconductor wafers.

The event should include a discussion of the benefits to the U.S. economy of continued leadership in microelectronics. By the turn of the century, the industry will be able to manufacture semiconductors containing hundreds of millions or even billions of transistors on a single chip. The impact of this increase in computing power will be enormous on U.S. economy, and is closely linked with the potential for economic growth of other Administration initiatives, such as the National Information Infrastructure.

SIA SEMICONDUCTOR INDUSTRY ASSOCIATION

March 8, 1994

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National Economic Council
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Katherine Gillman
Special Assistant for Defense Conversion
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Dear Tom and Kitty:

This is to acknowledge your skill and persistence in coordinating the White House event on March 2.

Given the early stage of implementation of the semiconductor technology roadmap program, the story line came through quite clear and resulted in some very positive press reports. We sincerely hope that the Administration achieved its objectives for the event.

Thank you.

Sincerely,

James A. Glaze, Ph.D.
VP. Technology Programs

Warren E. Davis
Vice President

cc: Kevin Brett, SIA
Bowman Cutter, NEC
John Gibbons, OSTP
Lionel Johns, OSTP
Andy Procassini, SIA

4300 Stevens Creek Boulevard, Suite 271 ■ San Jose, California 95129 ■ 408-246-2711 Fax 408-246-2830

The SIA

1995 Federal Budget White Papers

11/17/93

SRC 35MM
Sem 180
Univ 70M.

Executive Summary:

The SIA through its roadmap work has developed the following analysis of work being performed in the semiconductor R&D arena. Spending is approximately five billion dollars ($5B) for semiconductor R&D with about four billion dollars ($4B) being invested by the industry and one billion dollars ($1B) being invested by the U. S. Government. Of this investment $180M is invested through SEMATECH and $35M is invested through the SRC. The total amount of semiconductor R&D funding at universities is approximately $70M.

Investment distribution and timing is critical. Industry, due to the magnitude of its investment , focuses on the next two generations of technology while the universities focus further out on the third through fifth generations of technology. We think the ratio of 4:1 is appropriate for near term to long term. However, we have a unique asset in the U.S. University Research Community and we feel that the appropriate amount of funding given to support this asset should be around $100M, up from the current $70M.

In analyzing the distribution of this $5B investment against the needs of the semiconductor community we feel that some adjustments are needed to better meet the needs. Those adjustments are as follows:

- Increased Industry focus on the design, TCAD, packaging, and test R&D for semiconductors. SEMATECH has started to expand its focus beyond manufacturing to include these additional areas. The investment in these new areas will reach $30M by the end of 1994.

- Establish a Center for Semiconductor Metrology to provide leadership and focus on metrology. We see an activity growing from $2M to $25M per year.

- Capital productivity is becoming a major problem. SEMATECH has initiated a Future Factory Program with a goal of increasing capital productivity through improved factory designs. This Future Factory Program needs to be augmented with several National Laboratory programs to: establish a knowledge base for the design of processing equipment, develop reliability improvement techniques, develop advanced process control methodologies, and improved contamination free manufacturing techniques (SETEC); enhance modeling and simulation (CSMS); establish an equipment design support center (EDSC); and initiate a technology evaluation program to characterize the best innovations coming out of the universities (TEP). These programs will require an investment of approximately $10M in 1994 and level off at approximately $30M per year starting in 1995.

- ARPA has been a leader in the investigation of future semiconductor techniques and the industry applauds their efforts. Two specific additions would help address our ability to utilize ARPA's work.

  In addition to the recommended $60.2M ARPA funding for lithography, additional ARPA funding is needed for development of the non-exposure tool technologies necessary to augment the 193nm exposure tool work at Lincoln Labs. $3M of funding is needed.

  An expansion of the MCM packaging program for low cost and commercial applications is needed. $25M per year by 1995 is needed.

Contents:

Seven white papers follow which describe the activities needed to fill some of the gaps in the development semiconductor technology.

NIST CENTER FOR SEMICONDUCTOR METROLOGY

Recommendation

Purpose:

A government-sponsored Center for Metrology has been proposed to be established to assure that the semiconductor industry has the metrological support it needs. Metrology is one of the pervasive needs identified in the SIA Workshop Working Group Reports. Measurements needs are mentioned throughout the workshop publications, frequently as show-stoppers. Many other measurements not mentioned are serious problems, if not show-stoppers, as well. This Center would be located at the National Institute of Standards and Technology (NIST), which is the nation's lead laboratory for measurements.

This Center would conduct metrological research and development at NIST; coordinate metrological work among the cooperating Government laboratories; facilitate collaborations, CRADAs, and technology transfers; and act as the industry's focal point for metrology within the government. It would also represent NIST in roadmap management and maintenance, provide technical experts for Technical Advisory Boards, sponsor workshops to define industry needs and priorities, and work with the SEMATECH, SRC, and others to provide continuous improvement in the delivery of needed measurement tools and results.

Critical measurements and measurement techniques are needed for basic understanding, laboratory measurements, production control. A variety of measurements are needed, including but not limited to, detecting impurities, fine dimensional accuracy, and materials properties. The Center for Metrology would, as NIST now does, deliver its products to the industry through direct consultations and cooperative work, publications, talks, calibration services, special tests on customer artifacts, standard reference materials, membership on industry standards committees, and any other way that is appropriate. The following sections briefly describe potential programmatic thrusts for the Center for Metrology.

Metrology and Sensors:

This subject covers a wide range of needs identified in the National Roadmap. These measurements can provide data and new understanding for modeling and simulation (see below). Two categories of measurements are needed for process control and for evaluation of incoming materials and equipment. Robust on-line methods will give reliable measures of process performance. More basic methods are needed for gaining understanding of how processes work, for performance evaluation of incoming materials and equipment, for diagnostics, and for Standard Reference Materials.

Better process performance - Better understanding of complex processes will improve equipment design and operation and yield higher quality deposited films. Process and equipment design is now largely empirical. Because this understanding requires many good measurements, NIST is working on the physics and chemistry of plasma processes in collaboration with SRC-supported work in several universities and with SEMATECH, Sandia, IBM, and AT&T, among others. Expansion of this type of R&D will make possible the design of the new generations of equipment and processes needed for future semiconductor fabrication.

Improved basic measurements are necessary for process control. Examples of needed improvements include mass flow, temperature, and residual gas measurements. Improved mass flow controller calibrations have been established by NIST through SEMATECH temperature measurements in rapid thermal processing equipment are known to be seriously in error and critical to the success this technique. New measurement approaches are needed. More and more processes are being conducted in vacuum, but too much trust is put in the data from residual gas analyzers that can be off by orders of magnitude in vacuum systems containing plasma processes.

New in situ sensing and measuring devices are needed to give immediate feedback for process control. They may be optical, electrical, or mechanical, but they must be small and inexpensive. Some might be stripped-down or miniaturized standard instruments. Others may result from current work with micro-machined devices. New work is necessary to permit verification of whether or not innovative products from commercial instrument makers in fact do what their customers expect of them. New processes require new metrology.

Smaller structures place greater stresses on conductors and on insulators, leading to reliability problems. For example, NIST has been working for several years on electromigration, and has produced the industry standard evaluation tests now in use. Reliable data can now be obtained, but now work must be focused more on the metallization process to learn which variables must be controlled to provide metal patterns that are more resistant to electromigration. This approach has the potential of providing predictive reliability tests that will allow manufacture, by processes of demonstrated performance, of structures that have a predetermined level of reliability.

Contamination-Free Manufacturing

Reduced particle densities - Detecting particles smaller than 0.1 fm presents serious problems. Control of their presence is not possible if they cannot be found. Without better metrology, the process of equipment improvement will be even more difficult.

Clean chemicals and gases - On other contamination detection issues, similar metrology problems exist. New methods having greater sensitivity and spatial resolution are needed. In one specialized area NIST has already helped the industry. This work applies neutrons from the NIST materials-testing reactor to examine the depth distribution of certain elements, such as boron, in silicon and to measure the hydrogen content of gate oxides. Some of this work has been done in collaboration with leading semiconductor device companies.

Modeling and Simulation:

Measurements to validate models - The industry uses modeling extensively to refine device geometries and process performance. The thrust toward six sigma processes will require greater knowledge for these models. Only a few models are based on fundamental physics. Most include a great amount of empirical judgment or simplified physics that does not always scale properly when geometries shrink.

The predictions of these models must be checked to be sure that they are correct. As one example of the experimental data that is needed for this purpose, NIST accepted responsibility at the Roadmap Workshop for improved 2D and 3D measurements of dopant distributions in very small structures to show whether or not the predictions of existing computer-aided design models are correct. Measurements described under Metrology and Sensors above will provide most of the information needed for model validation.

Pattern Placement:

Smaller and smaller feature sizes - The National Roadmap calls for feature sizes that are smaller than can be supported by today's standards. Present optical methods cannot provide a new metrology base below about 0.2 fm. New approaches are needed because calibrated SEM methods may not be ready to meet the industry's needs in time. Measurement of small geometries on wafers cannot now be calibrated at all because they have thicknesses large compared with the wavelength of the illuminating light, because the edge shape is not well controlled, because the edges are not straight, or because the optical properties of the materials are not under good control. Some or all of these problems apply to almost every critical dimension measurement on a wafer. Scanning electron microscopes give clear images but without an accurate size calibration. NIST reference materials are universally used to calibrate measurements on masks and reticles. NIST is working on improvements in SEM magnification calibration. Solutions to the other problems mentioned must be sought.

In addition, two-dimensional measurements needed to verify the placement of images on reticles are not now accurate enough. A major improvement in

capability is needed. The industry needs significant improvement in pattern overlay and registration measurement and control as well.

X-ray lithography adds measurement challenges in source characteristics, optical components, and the wafer handling system. Although progress is being made, significant effort is needed to produce low-cost, reliable systems.

Packaging:

Packaging is a major cost contributor now. Technical drivers are the need to handle high frequencies and high power levels, and the need to integrate several chips into the same assembly. These needs require thermal, electrical, and mechanical measurement accuracy and techniques beyond today's capability. For example, designing for high power requires data on materials properties that now are seriously in error or entirely lacking.

These same data are also needed for design of conductor paths to carry very high frequency pulses without distortion. Most existing designs for multi-chip packages were made for applications in which cost was secondary to performance. Cost-effective designs rely at least as much as do high-performance designs on reliable materials data and on appropriate models for high-frequency design.

Metrology to solve these problems includes accurate measurement of thermal, stress, and high-frequency electrical properties of materials and of the ability of electrical connections, such as strip lines, to handle fast pulses, etc. Computer models to analyze electrical and thermal performance are also needed.

THE SIA 1995 FEDERAL BUDGET PROPOSAL:

Funding for this program is not in place. The SIA is proposing that this Center for Semiconductor Metrology be funded, if at all possible, starting in 1994, at a $10M level in 1995, and reaching a $25M/year beginning in 1996. We strongly suggest that 1994 budget be reviewed to find funds to start this center in 1994.

CONTACTS:

The SIA person most knowledgeable of this proposal is Owen Williams and the NIST person most knowledgeable of this proposal is Bob Scace.

TECHNOLOGY EVALUATION PROGRAM (TEP)

Program Recommendation

BACKGROUND:

The U.S. has a strong publicly funded research infrastructure within the national laboratory and university systems and is a world leader in the innovation of technology. However, recognized weaknesses are the effective transfer of this Research and Development to the commercial sector and the timely application of new technologies to defense needs. For example, university researchers develop new concepts and publish their results. However, due to the nature of the University Graduate Program, the evaluation of these concepts is frequently left incomplete. Potential industrial recipients of the research seldom can determine if practical application has been adequately demonstrated. Therefore, the risk associated with commercialization is too high for small to medium size commercial companies. In general, industry resources are widely dispersed and uncoordinated, preventing the detailed assessment necessary to prove practical value. The slow transfer of technology from universities to industry often allows other countries (such as Japan) to be the first to develop commercialized applications of U.S. research.

CURRENT ACTIVITIES:

Shrink technology (lithography) and manufacturing improvements (increase in chip size) have been the main contributors to increased levels of integration at the chip level; nevertheless, the technology would not be where it is today without corresponding innovations that have taken place in material, tools, processes, devices, circuits and design. Industry is emphasizing continued improvement along these lines, moving manufacturing into the nanofabrication region. Complexity is increasing while the development cycle continues to shrink. Industry continues to fund university research, through the SRC, SEMATECH, and direct investment. Escalating costs of development and manufacturing are increasing Industry's dependence on universities to provide the pre competitive research innovations. It is therefore becoming increasingly important that the U.S. address and minimize the barriers to rapid commercialization of its research results.

INITIATIVE:

Sandia National Laboratories has proposed utilizing its semiconductor fabrication facility to provide unique engineering and development support to bridge the gap between research ideas and engineering prototypes or process demonstrations for industrial and government application. The objective of the program is to select a few of the most promising, but un-proven, concepts coming out of the university research program each year and characterize that concept to demonstrate the potential for commercialization. Depending on the concepts chosen the characterization activities might relate to: (1) novel semiconductor device structures and circuits in a fully integrated implementation; (2) novel research ideas in design, development, or manufacturing and their usefulness in a fully integrated product or process; (3) novel processing concepts in a manufacturing environment; and (4) novel ESH concepts which require proof of concept to reduce risk. These activities would be organized for efficient transfer of technology by setting up joint projects between visiting university and industrial personnel. Appropriate funding to support this cooperative incubation activity is endorsed.

IMPLEMENTATION

Sandia has a finite process capacity. Management of projects is essential to optimize results. It is proposed that project selection from the SRC research program be based on committee reviews (1) to assure the project addresses a critical need in the national Semiconductor Industry Association (SIA) Roadmap, (2) has measurable and well defined goals and milestones, and (3) has an industrial advocate identified and committed to the program. The committee will consist of appropriate representatives from SRC, Sandia and industry.

Example projects that might be executed under this activity are:

1. Silicon Semiconductor Process Development: This type of project will support the characterization of novel semiconductor processing modules for improving device performance and reliability, increasing device and circuit yield, and reducing manufacturing cost. Special test devices and circuits may need to be fabricated to demonstrate reliability, to integrate process

modules into a full flow process, and to statistically characterize the acceptable processing parameter range.

Typical projects might include demonstrations of: new metal deposition and patterning processes, new high and low dielectric constant insulator deposition and patterning processes, methods for removing organic and metallic contamination from wafers during or after specific processing steps, selective deposition of insulators and metals, and methods for reducing process complexity.

2. Silicon Device Structure and Circuit Fabrication: This type of project would support the characterization of novel silicon semiconductor devices and circuits required to demonstrate new ideas in the areas of device structures and circuit architectures, smart solid state sensors, and test devices.

   Typical devices concepts might include: novel test devices for measuring model parameters, or determining contamination effects, or determining process variations effects on yield and performance; and might also include new neural network cells and circuits; fuzzy logic circuits; non-volatile memories using novel dielectrics; smart sensors; novel signal processor circuits; and innovative optical communications interface circuits.

3. Apparatus Development: This type of project would support characterization of novel manufacturing processes by constructing demonstration apparatus and applying detailed analytical and experimental resources to develop demonstration modules or chambers for characterizing such novel manufacturing processes.

   Typical activities might include: demonstration of novel energy sources, verification of models for equipment operation; demonstration of improved equipment and component reliability; and demonstration of new materials and methods to increase component life, reduce contamination, and decrease environmental impact. Specific problems may involve altering surface coating and base construction materials, measuring tribology characteristics of material combinations, developing in-situ sensors for process control, altering the use of environmentally hazardous chemicals and gases in particular

processes, and demonstrating methods for reducing effluent and waste products from manufacturing operations.

THE SIA 1995 FEDERAL BUDGET PROPOSAL:

The SIA proposes the above TECHNOLOGY EVALUATION PROGRAM be funded at a level of $5M/Y.

CONTACTS:

The SIA person most knowledgeable of this proposal is Jim Freedman and the Sandia person most knowledgeable of this proposal is Paul Peercy.

LITHOGRAPHY EXPANSION FOR 193nm

Program Recommendations

BACKGROUND:

Lithography is the key technology that has enabled the dynamic growth of the integrated circuit industry over the past two decades. This dramatic growth has been the result of improved resolution and overlay across increasingly larger chip areas. The key components of the lithography set are the exposure system; resist materials and processing; tracks for resist coat and develop; masks, including mask writer and associated processing; and metrology. All of these elements must be developed to produce a complete lithography solution. Lithography is a significant economic factor in integrated circuit manufacture; currently, it represents about 35% of the processed wafer cost.

INDUSTRY'S CURRENT ACTIVITIES

The industry has been and is focused on the use of optical lithography and expects it to continue as the technology of choice for the 0.35μ and 0.25μ feature size applications. Optics will be extensively used through at least the 0.25μm resolution generation. Progress in optical lithography has come about through many factors but wavelength reduction will be particularly important in the future: from 436nm (G-line) and 365nm (I-line) today, to 248nm (DUV) and to 193nm. Additional means of extending optics, including phase shift mask technology and off-axis illumination, are also being pursued. The industry's aspirations are behind optical extensions and this may well lead to optics being the technology of choice at 0.18μm resolution near the end of the decade. However, the difficulties of extending optical requires a parallel pursuit of non-optical approaches and several techniques are being investigated.

RECOMMENDED SPECIFIC NEAR-TERM ACTIONS (FOR THE GOVERNMENT):

The SIA recommends the continuation of the ARPA funding for Lithography (optical and non-optical) at the 1994 level of $60.2M. In addition to the $60.2M we propose increased funding specifically to support optical lithography at <200nm:

ARPA has been funding MIT Lincoln Laboratories pioneering work at 193nm. Funding of 193nm work on exposure systems should be continued and be expanded to include research and development in the areas of resist materials and processing, optical materials, and mask processing. This expanded work should be initiated at the appropriate site where the expertise resides.

The expanded 193nm activities will establish and initiate work on the critical techniques, methods, processes, etc. which must be proven before this lithography system can be considered a viable candidate for commercialization.

THE SIA 1995 FEDERAL BUDGET PROPOSAL:

The SIA proposes the continuation of ARPA lithography program at the $60.2M and a incremental increase of $3M/Yr to the 193nm program to allow for the above activities.

CONTACTS:

The SIA persons most knowledgeable of this proposal are Gordon McMillan and Dan Fleming, the ARPA person most knowledgeable of this proposal is Dave Patterson, and the Lincoln Labs person most knowledgeable of this proposal is Dave Shaver.

CENTER FOR SEMICONDUCTOR MODELING AND SIMULATION (CSMS)

Program Recommendation

NEED:

The National Semiconductor Technology Roadmap identifies modeling and simulation as an increasingly important tool in every R&D area. To meet these needs, augmentation of existing industry and university efforts is required to meet the complexity and computation challenges associated with future microelectronics products. In addition, the extension of modeling and simulation capabilities is required to address the vastly more complex circuits, the deep submicron structures and devices, the development and integration of manufacturing processes, and the design challenges associated with systems using integrated circuits. Therefore, a leading edge modeling and simulation capability is a prerequisite to a winning strategy for the U.S. semiconductor technology base.

Existing R&D in semiconductor modeling and simulation are fragmented among the various technology areas identified in the Roadmap. To meet the needs, an additional effort is required to provide:

- access to broader modeling and simulation experience,
- higher quality software research products for users,
- access to advanced computation facilities,
- common frameworks that link different application areas, and
- integrated models for broader, more complex applications.

RELATED PROGRAMS:

Semiconductor modeling and simulation is a result of several decades of high quality university research efforts. These efforts have resulted in a recognition that an expanded effort is required. In the expanded effort, it is extremely important to maintain and build upon the productivity and creativity of the university research base and to make available to them with the required computing power and programming capability.

To this end, it is strongly recommended that the government continue to fund the very important programs at ARPA and NSF in applied computation that have supported many of these university activities. This funding base has been threatened by shifting emphasis toward high performance computer development and the information highway. In particular, support should be maintained for 1) the ARPA programs in semiconductor modeling and simulation, in general, and TCAD, in particular, and 2) the highly seminal NSF support for computational electronics. Without continued support for these research programs, advances in semiconductor modeling and simulation efforts will be slowed.

INITIATIVE:

A new initiative is proposed for enhancing these university efforts and providing for the needs of the technology base. This is the DoE Center for Semiconductor Modeling and Simulation which will be based at the Los Alamos National Laboratory, but will include collaborative activities with Sandia National Laboratory and Lawrence Livermore Laboratory. It is proposed that this Center be created by means of a CRADA between Los Alamos and the Semiconductor Research Corporation (SRC). It will merge the advanced modeling and simulation experience and computation facilities of the National Laboratories with the demonstrated semiconductor technology expertise of universities.

The Center will be an industry monitored effort that takes advantage of the industry research advisory structure, demonstrated technology dissemination and transfer knowhow, and university interface that are available in the SRC. This will assure continuous application of the results as they become available and a firm focus on industry status and needs. In addition, Los Alamos would participate in the advisory structure for the National

Semiconductor Technology Roadmap so as to be continually aware of the status of R&D with which the Center would interface. In addition, the Center is integrated with and depends on the ARPA Process Synthesis Program.

The short-range goals of the Center are to cooperate with present university semiconductor modeling and simulation efforts as well as those in SEMATECH and other research organizations to provide enhanced modeling and simulation capabilities; and to upgrade university research products, when necessary, to be usable by the industry.

The long-range goals of the Center are to address complexity issues beyond the scope of university research and to integrate the university research products into coherent modeling and simulation packages. These long-range goals are among the most important success factors identified in the Roadmap for assuring the future success of the key U.S. microelectronics industry.

THE SIA 1995 FEDERAL BUDGET PROPOSAL:

The SIA proposes the funding of the above Center for Semiconductor Modeling and Simulation at a level starting at $2M in 1994 and increasing to 10M/Yr. in 1995

CONTACTS:

The SIA person most knowledgeable of this proposal is Bill Holton at the SRC and the LANL person most knowledgeable of this proposal is David Cartwright.

MULTI CHIP MODULE (MCM) TECHNOLOGY AND OTHER PACKAGING OPPORTUNITIES

Program Recommendations

BACKGROUND:

The U.S. packaging technology is fragile, as sources of component materials suppliers are virtually forfeited to foreign entities. However, opportunities exist especially in the integrated areas, in particular with Multi Chip Module Technology. MCM is an advanced compact substitute for Package-to-Board technology, and provides enormous systems advantages for the user. For example, higher levels of integrated functionality can be obtained by combining existing large scale (yield-limited) integrated chips, and equivalent performance can be achieved with reduced interconnect levels on chip.

The first national electronics infrastructure that successfully exploits the performance and packaging advantages of MCM's will gain enormous market penetration and advantage. It can be used as a stand alone strategy or as a complementary strategy with chip integration by time phasing the products with MCM technology - first with smaller chips to capture market position followed by silicon chip integration to drive cost down. In addition, the proliferation of portable commercial electronics makes it imperative that the MCM capability be coupled with low voltage operating capabilities. The nation that brings complex applications with low voltage technology to market first will achieve an advantageous position of wealth.

CURRENT ACTIVITIES:

ARPA has supported the development of these technologies, and provided a basis for a commercial capability in the industry, and this is laudable. However, there are additional areas that will need to be addressed beyond those covered by the current funding, set at $75M/yr.

INITIATIVE:

An emphasis and focus on the development of low cost packaging technologies is absolutely essential for widespread commercial use. A factor of about 5x reduction in cost of MCMs is needed. As the cost or MCM is driven down it will continue to compete with higher performance Printed Circuit Boards as interconnect density is increased. Other areas that need additional funding in the general and related packaging areas are: Wafer Level Burn In, Low Cost Flip Chip Assembly, Equipment and Processes for Wafer Bumping, Low Stress Molding Compounds and integration with Low Power Technologies.

THE SIA 1995 FEDERAL BUDGET PROPOSAL:

This is a funded program. The SIA proposes the continuation and expansion of this program by $25M/Yr to support these broader packaging areas with a greater emphasis on low cost, commercial opportunities.

CONTACTS:

The SIA persons most knowledgeable of this proposal are Tom Seidel, Alex Oscilowski, and John Kelly, and the ARPA person most knowledgeable of this proposal is Nick Naclerio.

Equipment Design Support Center (EDSC)

Program Recommendations

Because of the escalating development time and costs for precision equipment to support advanced semiconductor processes, a new design approach is needed for equipment development. The Equipment Design Support Center (EDSC) is planned to support the entire process of developing improved IC manufacturing equipment from basic research to machine prototype; followed by characterization in a semiconductor processing line. The development process relies on the use of accurate computer models to simulate the process and equipment operation, support from a variety of materials, physics, chemistry, process and mechanical experts, access to state of the art computing resources for design, manufacturing facilities for fabricating the prototype machines, and a wafer fabrication line for detailed equipment characterization and benchmarking. Although the focus of the center will be to support the semiconductor equipment industry in developing new six sigma process chambers for future semiconductor factory applications, the center will also provide consulting support for solving problems with present equipment designs and upgrade improvements.

In addition to providing personnel for assisting in detailed equipment designs, the center will provide computer facilities with on site workstations for use by visiting equipment design personnel, and remote computing access for equipment designers at company sites. The design computing center will contain a variety of codes for modeling plasma, CVD, and RTP processes, equipment reliability, and mechanical designs along with support utilities for meshing multi dimensional structures. The capabilities will support the complete design and analysis of, basic physics, chemistry, thermal, and fluid flow properties for proposed equipment designs. Process and chamber models developed during the equipment design phase can be used for equipment process control and flexible processing.

To support advanced equipment design and development, the center will:

Provide core support personnel & access to computing resources
Collect/Develop/Integrate/Maintain Process and Equipment modeling codes
Provide Expert Assistance/Consulting for equipment design
Provide computer resources for modeling and design evaluation
Develop model based and sensor based control strategies
Conduct workshops on design capabilities and processes
Maintain the knowledge base and database of contacts for specialty subjects

Track world wide progress via papers, presentations and visits
Acquire model verification data (existing and new designs)
Optimize university interfaces via direct support through the Center for Microelectronics Technology Interface control and diagnostic methods, in situ/in line sensors, materials, CFM, equipment characterization / instrumentation, environmental issues into equipment development process

The Center will also be responsible for developing and maintaining a business plan and a roadmap aligned with the national roadmap for semiconductor technology, as well as integrating and coordinating synergistic ARPA, DOE, DOD projects. The strategic approach utilizes the broad multidisciplinary engineering capabilities and the microelectronics fabrication laboratory (MDL) at Sandia National Laboratories, in a partnership with industry to provide a resource center of advanced equipment design expertise. Projects for the partnership will be selected on the basis of alignment with the SIA roadmap and potential for implementing new revolutionary designs, which can impact factory cost and provide significant advances in implementing the next generation technology.

Description of Work:

Specific tasks include assembling design teams and developing / collecting / integrating / maintaining basic processing and equipment modeling codes; providing computer resources and expert assistance for equipment design; developing model-based control systems; developing in situ sensors for on-line monitors and process control; reduction of contamination in equipment and processes; robotics for transfer of wafers between and within chambers; and fabrication and extensive benchmarking and characterization of prototype equipment.

In addition to formally establishing the center and providing basic modeling and simulation capabilities, consulting and training will be provided to assist equipment companies in utilizing the center's resources, both on site and in remote locations or at regional design access centers. The center is also expected to provide the nucleus for special design support teams in designing six sigma chamber prototypes for future factory applications. To begin the project, it is proposed that two teams be established to develop models and the knowledge base to support the design of new LPCVD and Plasma Polysilicon Etch Chambers.

The goal for LPCVD will be to establish the knowledge base to support the design, fabricate and characterize an ultra reliable mini batch chamber with optimized temperature control and gas injection, minimum furnace effluents, interface to a standard wafer handler, and efficient model based control.

The goal for polysilicon plasma etch will be to establish the knowledge base to support the complete system design for a polysilicon etch chamber with optimized chamber geometry, materials, plasmas source, power supply, matching networks, electrostatic chuck, wafer loading/unloading, gas distribution, waste handling, chamber and wafer cooling, chamber cleaning, sensors for monitoring and control, and integrated control system. The knowledge base must include techniques for acheiving low contamination levels, six sigma performance goals, optimized geometry is for flow, no (few) internal perturbations and/or instrumentation ports, and ideal wafer transfer and positioning.

Although the initial focus will be on LPCVD and Polysilicon Plasma Etch chambers, other common chamber may include: (1) Plasma etch (Oxide, silicon nitride), (2) Metal deposition (Aluminum, Copper, Tungsten), (3) Metal etch, (4) Plasma enhanced deposition (Immersion Implantation, nitride), (5) Photoresist ashing, (6) RTP (CVD, anneal, oxide growth), (7) Chemical Mechanical Polishing, (8) Lithography (x ray, e beam), (9) Photoresist deposition, and (10) Advanced cleaning.

THE SIA 1995 FEDERAL BUDGET PROPOSAL:

The SIA proposes the funding of the above ECSC program at a level starting at $3M in 1994 and increasing to 12M/Yr. in 1995

CONTACTS:

The SIA person most knowledgeable of this proposal is Richard Deininger at SEMATECH and the Sandia person most knowledgeable of this proposal is Paul Peercy.

SEMICONDUCTOR EQUIPMENT TECHNOLOGY CENTER (SETEC)
Program Recommendation

The SETEC program was started in mid 1989, in support of SEMATECH, to improve the competitive position of the U.S. semiconductor equipment industry. The program focused on three goals: (1) improve equipment reliability, (2) develop diagnostic techniques for monitoring processes and adapt these techniques to improved process control, (3) develop models for describing and optimizing manufacturing equipment design and processes, and (4) the research and development in the area of Contamination Free Manufacturing (CFM). Over 35 projects have been supported including: extensive benchmarking and characterization of foreign and domestic processing equipment; modeling of the physics, chemistry and operation for plasma, RTP and LPCVD equipment; development of reliability guidelines and software quality improvement methods; development of diagnostics for plasma processing equipment; development of control systems for magnetically levitated fine stages for lithography equipment; modal and vibrational analysis of lithography equipment; development of selective tungsten deposition processes; tribology analysis for critical component interfaces in processing equipment; ergonomics analysis of equipment and optimization of the human interface; development of improved materials and coatings for critical plasma chamber and lithography tool components and electrostatic chucks; design of improved control systems for CVD furnaces and plasma chambers; and reliability modeling of manufacturing equipment.

THE SIA 1995 FEDERAL BUDGET PROPOSAL:

This is a funded program under a five year CRADA between SEMATECH and Sandia. The SIA proposes the 1995 Federal Budget reflect the CRADA commitment and include the budget it requires.

CONTACTS:

The SIA person most knowledgeable of this proposal is Richard Deininger and the Sandia person most knowledgeable of this proposal is Paul Peercy.

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INTRODUCTION AND SUMMARY

The Semiconductor Industry Association (SIA) has established a national technology strategy in partnership with SRC and SEMATECH, the Federal government, industry and academia. The focus of this initiative is the identification of technologies critical to the future success of the U.S. semiconductor industry and utilization of this Nation's intellectual and financial resources to meet the daunting technological challenges that face this industry.

As a first step in implementing its strategy, SIA has developed a 15 year National Semiconductor Technology Roadmap developed by almost 200 experts from industry, government and academia. From this Roadmap, SIA will identify high risk pre-competitive initiatives that fit the dual use private-public partnership model.

Enclosed herein are seven initiatives that SIA believes should be supported by the government beginning in FY 1995. These initiatives focus on critical needs in metrology, modeling and simulation, packaging, lithography, equipment, technology evaluation and processing. In total these programs represent expenditures of approximately $60M in FY 1995 increasing to approximately $80M in FY 1997.

Today, industry alone is spending almost four billion dollars for semiconductor research and development. The programs proposed in this memorandum provide substantial leverage for pre-competitive initiatives of critical importance for both industry and government.

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DEPARTMENT OF DEFENSE
(SIA RECOMMENDATIONS FOR FY 1995)

193 nm Lithography

The Semiconductor Industry Association (SIA) strongly supports ARPA's current program in lithography including the 193 nm work at MIT's Lincoln Laboratories. In addition, SIA recommends that ARPA augment the 193 nm Lithography research at Lincoln Laboratories. More specifically, SIA would like to see ARPA's 193 nm program expanded to include additional R&D in critical areas of resist materials and processing, optical materials, mask processing and exposure systems in support of optical extension to 193 nanometers.

Optical lithography is a critical technology which, perhaps more than any other, has enabled the integrated circuit industry to enjoy over two decades of dynamic growth. Lithography at 193 nm is an extension to shorter optical wavelengths for the purpose of increasing resolution in order to reduce IC device feature size. SIA estimates that the extension to 193 nm may play a significant role in achieving its National Technology Roadmap goals throughout this decade.

Today optical lithography accounts for over 35% of the cost of a processed wafer. As this technology is extended to 193 nm, costs will escalate rapidly unless critical issues are resolved. This can only be accomplished if industry is supported by a strong national R&D program which addresses the high risk precompetitive aspects of this technology. Extension of the program to address 193 nm lithography at Lincoln Labs is a small but important step toward this goal.

SIA proposes the continuation of ARPA's lithography program presently funded at $60.2 M and an incremental increase in FY 1995 of $3M per year for the 193 nm program presented above.

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DEPARTMENT OF DEFENSE
(SIA RECOMMENDATIONS FOR FY 1995)

Multi Chip Modules

The Semiconductor Industry Association (SIA) recommends that ARPA, through its Electronic Systems Technology Office (ESTO), re-structure a portion of its 1995 **Multi Chip Module** technology initiative to include an expanded effort in support of SIA's National Technology Roadmap on Advanced Packaging.

Advanced Packaging is a critical element of SIA's Roadmap strategy to address the IC needs of future generations of electronics products. Packaging is the interface between the chip and the system. As both function and complexity at the chip level increase, complementary advances in package design must follow. Presently, the broad commercial market for semiconductor devices is driven by single chips wire bonded to plastic packages. However, the industry must now actively pursue advanced packaging architectures which satisfy both the demanding technical requirements of future generation IC devices and, at the same time, be low enough in cost to be competitive in mainstream commercial markets.

ARPA has been a leader in the sponsorship of Multi Chip Module packaging technology. Much of ARPA's efforts have been directed at architectures that serve highly integrated applications such as mainframe computers and military systems. The cost structure of this technology will not support widespread use in commercial products or meet many of the cost objectives of future military components. Therefore ARPA sponsorship of low cost MCM design and manufacturing technologies can serve both its military development objectives and aid U.S. industry in its drive to achieve a competitive posture for future generations of commercial products.

SIA supports ARPA's ongoing programs in MCM research and development. Further, SIA recommends that a portion of ARPA's efforts be expanded and/or re-aligned to place greater emphasis on the development of low cost packaging initiatives that are essential for future commercial and military applications. Proposed funding of this initiative is $25M per year beginning in FY 1995.

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DEPARTMENT OF COMMERCE
(SIA RECOMMENDATIONS FOR FY 1995)

Metrology

The Semiconductor Industry Association (SIA) recommends that a new **Center for Metrology** be established at the National Institute of Standards and Technology (NIST). As this Nation's lead laboratory for measurements, NIST is preeminently positioned to provide the leadership in metrology science that is required if the U.S. semiconductor industry is to meet its manufacturing goals through the end of this century and beyond.

Metrology cuts across all aspects of advanced microelectronic manufacturing. As device features continue to shrink, demand for improved manufacturing equipment, process control and inspection escalates dramatically. Perhaps more than any other discipline, metrology is the key enabler for achieving many of the critical technology milestones identified in SIA's National Roadmap. Its dependency is pervasive throughout the entire semiconductor manufacturing process.

With the creation of the new **Center for Metrology**, the semiconductor industry will be provided with a critical focal point from which it can coordinate the implementation of its metrology needs as detailed in the National Roadmap. This coordination can be accomplished in cooperation with government, industry, academia and the SIA affiliate organizations SRC and SEMATECH. In addition to conducting metrology research and development, the Center will also coordinate metrology work among cooperating Government laboratories and provide a critical path to future commercialization through the technology transfer process.

SIA recommends that seed funding of $10M be added to NIST's FY 1995 budget. This funding should be increased to $25M per year in 1996.

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DEPARTMENT OF ENERGY
(SIA RECOMMENDATIONS FOR FY 1995)

Modeling and Simulation

The Semiconductor Industry Association (SIA) proposes to create a new **DoE Center for Semiconductor Modeling and Simulation.** This center will be based at Los Alamos National Laboratory and will be funded by a CRADA between Los Alamos National Laboratory and the Semiconductor Research Corporation (SRC), an SIA affiliate. This Center will merge the capabilities of the national laboratories, including advanced modeling and simulation experience, with the demonstrated semiconductor technology expertise of the universities.

Integrated circuit manufacturing complexity is progressing at a rate which exceeds the industry's ability to model and simulate its critical elements. With the escalating costs of factories and equipment, the U.S. semiconductor industry, if it is to remain competitive, must ameliorate the risks inherent in its multi-billion dollar commitments to advanced generations of microcircuit design and fabrication. Modeling and simulation will provide essential predictive capabilities for many of the critical technologies identified in the SIA National Roadmap as well as provide an in-depth knowledge base of the technologies being simulated. This knowledge base will ultimately lead to superior applications of the technology.

The semiconductor industry needs a well coordinated and focused initiative in modeling and simulation if it is to meet the objectives of SIA's National Roadmap. Presently, efforts in this area are fragmented. With its extensive computational capability and past experience in modeling and simulation, the Los Alamos National Laboratory can play a vital leadership role. Moreover, it can serve to support the innovative research efforts of the universities by providing the long-term continuity required to transition the results of their research to hardened systems for use by industry.

SIA recommends that funding for this program should be $10M per year starting in 1995.

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DEPARTMENT OF ENERGY
(SIA RECOMMENDATIONS FOR FY 1995)

Sandia National Laboratory

Sandia National Laboratory is a leader in its support of SEMATECH and SIA sponsored technology programs. SIA supports the continuation and strengthening of Sandia's Semiconductor Equipment Technology Center (SETEC). In addition, SIA supports Sandia's programs to develop and improve IC manufacturing equipment through its proposed Equipment Design Support Center (EDSC) and to facilitate the transfer of results of university research and development programs to the commercial sector through its proposed Technology Evaluation Program (TEP).

The **Technology Evaluation Program** will provide a vital link between innovative research performed by universities and research institutions and the very specific practical needs of industry and defense. This evaluation of innovative concepts will help ameliorate risks that many small to medium size firms are ill prepared to shoulder. Further, it will aid in speeding promising technologies into the marketplace, while screening those initiatives that are premature and/or require further development.

The **Equipment Design Support Center** will address the critical issues of escalating equipment costs and ever increasing time-to-market for advanced production equipment. EDSC will address issues ranging from basic research to the use of equipment in manufacturing. EDSC will coordinate its activities with the semiconductor equipment industry and will provide access to sophisticated computational resources including software for use in process modeling.

SIA recommends that the **Technology Evaluation Program** be funded at a level of $5M per year starting in FY 1995. SIA further recommends that the **Equipment Design Support Center** receive funding of $3M in FY 1994, increasing to $12M per year in FY 1995.