DM3730/AM3703 Torpedo™ SOM Design Checklist

Application Note 493

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Abstract

This application note provides a list of items to verify when designing the DM3730/AM3703 Torpedo SOM into an embedded system. Reviewing this checklist prior to releasing design files and software for production can help reduce the probability of future board spins.

Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	RAH	-Initial Release	RAH, NJK	08/17/11
B	RAH, SO	-Throughout: Updated baseboard references to Torpedo Launcher 3; -Added Table 2.3; - Table 2.4: Corrected SOM pin number for GPIO_5 to J2.20; -Section 2.4: Added 80uF to Main_Battery requirement to list number 1; -Section 9: Added list number 2 regarding TRS3386 RS-232 transceiver; -Section 11: Added language regarding support for 24-bit (8:8:8) color; -Section 2.17: Added note about putting down a serial EEPROM	RAH	07/24/12
C	BSB, NJK	-Section 2.4: Added list number 2 and 3 regarding minimum battery threshold for device to power OFF and ON; added list number 9 regarding the BQ27000 fuel gauge; -Section 2.12: Added information on voltage translator for MMC2 and MMC3; -Section 0: Added note to ensure the SOM PMIC can adequately recharge backup battery; added currently recorded consumption of BACKUP_BATT; added note that battery must provide sufficient power for entire length of time required by usage model; -Added Section 2.19;	RAH, SO	01/25/13
D	SO	-Section 2.4: Added list number 9.a, 9.b, and 9.c regarding the BQ27000 gas gauge; -Section2.7: Added list number 11 regarding the CONFIG3/MCSPI3_CLK signal; -Section 2.12: Recommended TXB0108 as voltage-level translator rather than TXS0108	RAH, NJK	07/03/13
E	SO	-Throughout: Updated template; updated links for new support site; -Section 2.8: Added list number 4 and 5; -Section 3.4: Updated list number 5 with additional recommendation to add outline of CPU and debug connectors	RAH, BSB	11/26/13
F	BSB	-Throughout: Removed most "Contact Logic PD" links and pointed users to TDG forum instead; -Section 2.12: Added reference to example source code in Appendix A; -Added Section 2.18 regarding the GPMC bus; -Table 5.2: Corrected information for LOCK NAND signal; -Added Appendix A	SO	05/15/14
G	ABF	-Added note on BACKUP_BATT -Additional Wake-up from pins -Update to note is section 2.3 clarifying MSTR_nRST -Fix comment about terminating the LCD signals	AM	07/16/14
H	BSB	-Section 2.11: Updated USB OTG VBus for external VBUS supply -Section 2.17: Added the recommendation to use the Microchip 93AA46AT-I for the Ethernet EEPROM. -Section 3.5: Added information to reference the Thermal Management WP -Section 4: Added information concerning the usage of audio mute -Appendix A: Updated patch to included Torpedo and Torpedo + Wireless SOMs	ABF	11/14/14
I	BSB	-Section 2.7: Remove #12 showing some GPIO signals are not available.	BSB, AF	03/09/16
J	BSB	-Section 2.19: Updated the hyperlink for the Logic PD ZIP product.	AF	12/09/16

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1 Introduction

When using the DM3730/AM3703 Torpedo SOM in an embedded system, reviewing some specifics during the design phases can minimize or even eliminate future board spins. Information provided in this application note should be reviewed prior to releasing a design for fabrication and assembly. It is also critical that software teams review Sections 4 and 5 to ensure a trouble-free first board boot.

2 Schematic Checklist

Items in this section should be reviewed by the system designer prior to releasing the design for layout.

2.1 Analog-to-digital Converter Signals

Analog-to-digital converter (ADC) signals that are not used must have the connections outlined in Table 2.1 per the TPS65950 specification.

Table 2.1: Connections for Unused ADC Signals

ADC Signal	SOM Signal Name	SOM Pin	Connection	Maximum Voltage Input
PMIC.ADCIN0	CONFIG11	J1.76	GND	1.5V
PMIC.ADCIN1	CONFIG10	J1.78	GND	1.5V
PMIC.ADCIN2	CONFIG9	J1.80	GND	2.5V
PMIC.ADCIN3	CONFIG8	J1.82	GND	2.5V

It is recommended that these signals are connected to GND when not used on the baseboard; however, there are also no-pop resistor options available on the DM3730/AM3703 Torpedo SOM to connect these signals to ground. Contact Logic PD[1] for information on generating a new product introduction (NPI) to populate these resistors according to your usage model.

2.2 Clocks

Verify that series termination is available for all clock signals that do not have internal drive strength control.

2.3 Reset

The MSTR_nRST signal is driven by the on-board power management IC (PMIC), and it can only be driven low by external devices.Logic PD recommends avoiding an external power-on reset sequence.

2.4 Power

1. Verify all power and ground signals are connected correctly and are at the correct voltage level. Most importantly, Main_Battery should be driven directly by a single-cell lithium-ion battery or a fixed, regulated power source. Connecting a minimum 80uF capacitor to this rail on the baseboard is recommended.
2. For battery-powered designs, the minimum voltage supplied to MAIN_BATTERY at which the device will power ON is 3.2V +/- 100 mV. Note that 2.7V is the minimum

[1] http://www.logicpd.com/contact/inquiry/

threshold for the battery at which the device will power OFF once the system is running.

3. For non-battery-powered designs (i.e., MAIN_BATTERY is supplied by a fixed-voltage supply), the minimum voltage supplied to MAIN_BATTERY at which the device will power ON may be as high as 3.3V, depending on silicon variances. The fixed-voltage supply to MAIN_BATTERY must guarantee a minimum voltage of 3.3V, including any tolerance in the fixed-voltage supply or IR drop from the supply to the SOM. Note that once the system is running, the SOM will power off if MAIN_BATTERY falls below 2.7V.
4. Review Logic PD's *AN 489 DM3730/AM3703 Torpedo SOM Power Management*[2] for specific power interface connections.
5. Verify the recommended bulk capacitance is used. Refer to *AN 489 DM3730/AM3703 Torpedo SOM Power Management* for requirements.
6. Verify the regulator provides sufficient current to meet demands, including any peripherals powered by the DM3730/AM3703 Torpedo SOM.
7. VAUX4 is not enabled by default in Logic PD software. This power supply must be enabled before using the signals in Table 2.2. Refer to *AN 489 DM3730/AM3703 Torpedo SOM Power Management* for details.
8. VPLL2 must be enabled to power VDDS_DSI of the processor during normal operation.
9. The battery fuel gauge shown in the reference design, a Texas Instruments (TI) BQ27000, requires 21V to program some of the registers for the best performance. If the gas gauge will not be pre-programmed during manufacturing:
    a. Ensure that the charger circuit will allow the BQ27000 to detect battery full. The default taper current for battery full is ~100 mA. The charger circuit must allow the charging current to drop below this threshold for at least thirty seconds before shutting off.
    b. For proper capacity measurements, ensure any battery starts fully discharged before attaching to the BQ27000. The default battery capacity for the BQ27000 is 2000 mAh. Values above 2000 mAh will be learned on the first charge cycle. Values below 2000 mAh will be approached over full charge/full discharge cycles, with a maximum decrease of 12.5% per cycle. The default battery discharge learning cutoff is 3.25V, where the BQ27000 assumes 6.25% of capacity remains.
    c. Refer to TI's BQ27000 product page[3] for more information on this fuel gauge.

2.5 Level Shifters

1. Verify if any of the signals or busses used from the DM3730/AM3703 Torpedo SOM need level shifting for your specific design. In general, the SOM is a 1.8V I/O module.
2. The TRS3386 RS-232 transceiver is no longer qualified to work at 1.8V. The TRS3253 is an alternative device that does support 1.8V operation.
3. Verify the correct reference voltage from the DM3730/AM3703 Torpedo SOM is used for signal level shifting or pull-ups.
4. Verify that the reference voltage is not used as a power source, except within the limits allowed.
5. Verify that the direction signal has the proper direction control.
6. Verify that unused level-shifter input signals are tied per the level-shifter specification and are not left floating (unless required by the specification).

[2] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=585
[3] http://www.ti.com/product/bq27000

7. For interface signals that have different directions (e.g., RX and TX), verify that the level shifters also have different direction signals.
8. Verify that the level-shifter voltage requirements for VCCA and VCCB are being met. Most level shifters require VCCB to be higher, but this is not a guarantee.

2.6 Peripheral Interfaces

1. Verify peripheral interface connections, such as USB, serial, and MMC/SD card, are equivalent to those on the Torpedo Launcher 3 Baseboard.
2. If you plan to use a custom population option of the CONFIG resistors, note that on the schematics and contact Logic PD to begin the NPI process. Be sure to include the NPI turnaround time in your schedule.

2.7 GPIO

1. Verify the signal selected to be a GPIO is actually available as an alternative function or has a dedicated GPIO, GPI, or GPO function needed for the design.
2. Avoid using MCSPI2_SOMI and MCSPI2_SIMO as input or output signals in your design, as they are used to drive status LEDs from LogicLoader. Even if your system design will not use LogicLoader, it is recommended to use other available GPIO signals and avoid MCSPI2_SOMI and MCSPI2_SIMO. If you do not plan to use these GPIOs, place easy-to-access test points so that they can be used for debugging.
3. Verify that no contention occurs on GPIO signals during reset and low-power mode states.
4. Verify that signals designated as GPIO have reset states with the desired direction and level.
5. BT_PCM_DR and BT_PCM_DX from the DM3730/AM3703 Torpedo SOM are actually connected to the PMIC. Use all of the processor GPIO pins before using GPIO pins connected to the PMIC. If your design absolutely requires the use of PMIC GPIO pins, please post a question to the Logic PD Technical Discussion Group (TDG) forum[4] for programming suggestions.
6. uP_DREQ0 should be left floating at power on; it is tied to the NAND flash LOCK pin and is read at power on.
7. Verify the GPIO signals in Table 2.2 are used as input-only (GPI) signals. **NOTE:** The VAUX4 supply powering these signals is not enabled by default in Logic PD software. This power supply must be enabled before these signals can be used.

Table 2.2: GPI Signals

uP GPIO Signal	SOM Signal	SOM Pin
GPIO_99	CSI_D0	J2.85
GPIO_100	CSI_D1	J2.87
GPIO_105	CSI_D6	J2.57
GPIO_106	CSI_D7	J2.55
GPIO_107	CSI_D8	J1.76 (optional)
GPIO_108	CSI_D9	J1.78 (optional)

8. Verify the GPIO signals in Table 2.3 below have series termination due to buffer strength on these pads. TI recommends starting with a 30 ohm dampening resistor. Depending on the specific design requirements, change to the resistor value may be

[4] http://support.logicpd.com/TDGForum.aspx

necessary to reduce overshoot and undershoot signals. TI recommends these signals be used as GPIOs only if no other solutions are possible. See "Section 25.2" of TI's *AM/DM37x Multimedia Device Technical Reference Manual (TRM)*[5] and TI's *SD-MMC Usage Notes on OMAP35 and AM37x* wiki page.[6]

Table 2.3: GPIO Signals with Series Termination

uP GPIO Signal	SOM Signal	SOM Pin
GPIO_120	SD1_CLK	J2.32
GPIO_121	SD1_CMD	J2.42
GPIO_122	SD1_DATA0	J2.48
GPIO_123	SD1_DATA1	J2.46
GPIO_124	SD1_DATA2	J2.44
GPIO_125	SD1_DATA3	J2.50
GPIO_126	SD1_DATA4	J2.52
GPIO_127	SD1_DATA5	J2.54
GPIO_129	SD1_DATA7	J2.60

9. Verify that GPIO signals used to wake up the processor have power to the I/O pads within the processor at the time the processor is in low-power mode. When only the WAKEUP power domain is active (ie, OFF mode), the following signals can be used to generate a direct wake-up event:

   - GPIO_1 (T2_CLKREQ) – Not routed externally
   - GPIO_9 (uP_SYS_OFF_MODE) – Not routed externally
   - GPIO_10 (uP_CLKOUT1_26MHz) – Available on J2.88
   - GPIO_11 (uP_EMU0) – Not routed externally
   - GPIO_30 (SYS_nRESWARM) – Available on J2.6
   - GPIO_31 (uP_EMU1) – Not routed externally

   For the rest of the GPIOs in the GPIO1 module (GPIO_0-31, not include the ones above), they can only generate wakeup events if the CORE power domain is active.

   For the GPIOs in module GPIO2-6 (ie, GPIO_32-191), they can only generate wakeup events if the PER power domain is active.

   Ensure that if you intend to use a GPIO as a wakeup event, you connect it to the appropriate GPIO signal.

   For GPIOs not listed above as wake-up sources, the processor provides a wake-up scheme controlled by the I/O daisy chain. This scheme allows GPIOs to be monitored while the PER power domain is off. In order to function correctly as wake-up sources, GPIOs must be properly enabled before the PER power domain is disabled. Please refer to "Section 3.5.7.2.2" of TI's *AM/DM37x Multimedia Device TRM* for more information on how to enable this feature.

Verify the GPIO signals listed in

10. Table 2.4 are not pulled high or low during reset.

[5] http://focus.ti.com/docs/prod/folders/print/dm3730.html#technicaldocuments
[6] http://processors.wiki.ti.com/index.php/SD-MMC_Usage_Notes_on_OMAP35x_and_AM37x

Table 2.4: GPIO Signals Not Pulled High or Low during Reset

uP GPIO Signal	SOM Signal	SOM Pin
GPIO_2	LCD_D18	J2.36/J2.100
GPIO_3	LCD_D19	J2.34
GPIO_5	LCD_D20	J2.20
GPIO_6	LCD_D21	J2.40
GPIO_7	LCD_D22	J2.80/J2.89
GPIO_8	LCD_D23	J1.87 (CONFIG2)

11. CONFIG3 (default MCSPI3_CLK) is used by software to control the audio mute circuit on the Torpedo Launcher 3 Baseboard. If you wish to use this signal as a GPIO or SPI CLK, please post a question to the Logic PD TDG forum for information about how to modify the source code.

2.8 LCD

1. The recommended LCD interface is to support 16-bit (5:6:5) or 24-bit (8:8:8) color. Please post a question to the Logic PD TDG forum for additional information about supporting other color depths.
2. Verify that the targeted LCD works by using LogicLoader scripts to interface with the Torpedo Launcher 3 Baseboard. Please post a question to the Logic PD TDG forum for assistance if needed.
3. If your LCD requires a specific power supply startup sequence, use LCD_PANEL_PWR to initiate the sequence and use LCD_BACKLIGHT_PWR to control the backlight. This will align with the OS software provided by Logic PD.
4. Add 10 ohm series termination resistors to all data lines, HSYNC, VSYNC, ACBIAS, and PCLK.
5. See TI's *AM37x/DM37x Schematic Checklist* wiki page[7] for additional information about the Display Sub-System.

2.9 Debug

1. Serial: Logic PD recommends all designs have a debug serial port. This port is used for terminal access to LogicLoader and Linux. Also, Windows CE debug messages can be enabled to output to the debug serial port. uP_UARTA_TX and uP_UARTA_RX are the dedicated debug port signals used on the DM3730/AM3703 Torpedo SOM.
2. JTAG: The JTAG interface and voltage required for your tools may be different than those used on the DM3730/AM3703 Torpedo SOM. Verify that the JTAG connector interface on the DM3730/AM3703 Torpedo SOM will interface to the emulator that is planned for software development.
3. Ethernet: Logic PD recommends putting down a WLAN Ethernet port on the first pass of baseboards. This port can be used for development and download purposes and can be copied from the Torpedo Launcher 3 Baseboard.
4. Reset: Logic PD recommends designing in a debounced MSTR_RST button to the DM3730/AM3703 Torpedo SOM to aid in debug.

[7] http://processors.wiki.ti.com/index.php/AM37x/DM37x_Schematic_Checklist#DSS

5. GPIO: Connect LEDs to MCSPI2_SOMI and MCSPI2_SIMO to act as status indicators during board bring-up. At a minimum, provide test point access to these signals.
6. Test Points: Place test points for all power supplies and reset signals going into the DM3730/AM3703 Torpedo SOM. Label with descriptive names on the silkscreen.
7. R-packs: Avoid use of R-packs on the first pass of a custom baseboard. Using discrete resistors will allow for easier rework.

2.10 I/O Interface

Verify that any signal driven from the DM3730/AM3703 Torpedo SOM has no more than one load. A buffer must be used if driving more than one load from the SOM in your design.

2.11 USB OTG VBUS

A 4.7 uF capacitor must connect J2.11 and J2.13 (USB1_VBUS) to ground.

USB1_VBUS is driven by the TPS65950 and can only supply 100 mA of current on VBUS. If more than 100 mA is required, it is possible to design an external VBUS supply to coexist with the USB1_VBUS signal.

When using an external VBUS supply similar to the NCP380 it is recommended VBUS from the SOM be connected to an external a 10uF capacitor.

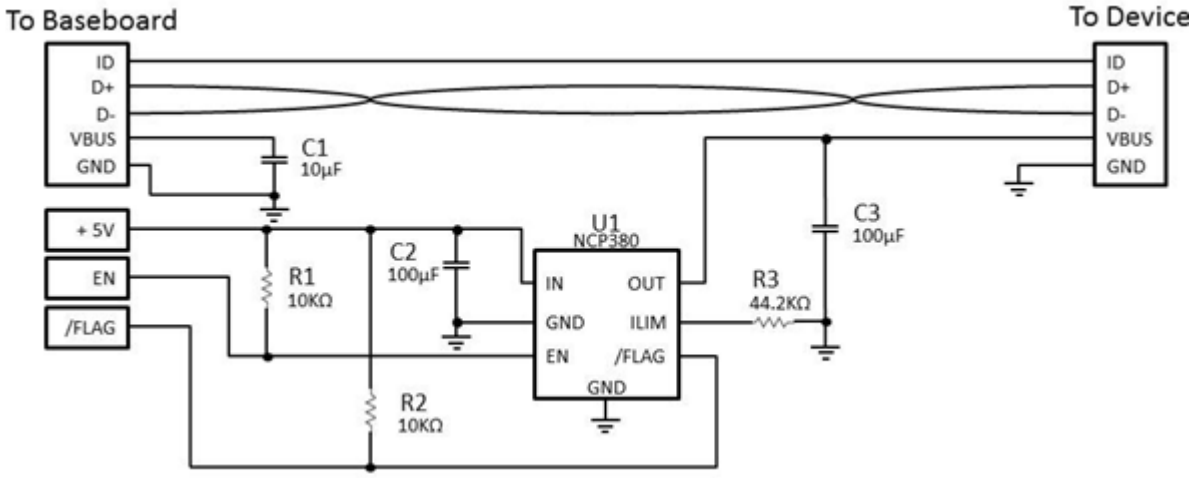

Figure 1 Example Using NCP380

2.12 Secure Digital / MicroSD Card Detect

When Secure Digital (SD) or MicroSD cards are used in a system design, signal J2.54 (uP_GPIO_127) is configured by LogicLoader as a card detect signal. For card sockets that do not have a card detect pin, connect J2.54 (uP_GPIO_127) to ground. Example source code changes when using a MicroSD card with Linux are provided in Appendix A.

Voltage-level translation is required to support 3.0V cards on the MMC2 interface. An 8-bit, bidirectional voltage-level translator for open-drain and push-pull applications allows for voltage translation without the need of direction control signals. Logic PD has used the TXB0108[8] from TI in several designs.

2.13 Real-Time Clock Battery Backup

If your design uses a rechargeable battery to back up the real-time clock (RTC) on the TPS65950, do not place any capacitors on the BACKUP_BATT rail. Doing so will prevent the TPS65950 from charging the backup battery.

Verify the rechargeable backup battery targeted for your design can be adequately charged by the DM3730/AM3703 Torpedo SOM PMIC. The PMIC provides a constant current that can be set at 25 uA, 150 uA, 500 uA, or 1 mA. The available cutoff voltages for the backup battery are 2.5V, 3.0V, 3.1V or 3.2V. Inadequate charging could prevent the backup battery from being fully charged.

[8] http://www.ti.com/product/txb0108

If your design uses a non-rechargeable battery, place a diode on BACKUP_BATT to prevent accidental charging of the battery.

Current consumption on BACKUP_BATT has been measured as high as 50 uA but is typically 10 uA. Choose a battery, rechargeable or not, that can supply sufficient power for the entire length of time required by your usage model. For example, if your usage model leaves MAIN_BATT disconnected for a total of six months over a product life cycle, a backup battery of at least 216 mAh is required, such as a CR2032.

Please refer to *AN 489 DM3730/AM3703 Torpedo SOM Power Management* for details on connections.

If your design is not powering the BACKUP_BATT signal it must be connected to ground.

2.14 McBSP

The DM3730/AM3703 Torpedo SOM can support up to four McBSP ports (McBSP2 – McBSP5). Of the four McBSP ports, McBSP2 and McBSP3 are connected to the TPS65950.

- McBSP2 is connected to the TPS65950 audio interface. To use McBSP2 externally, the AUDIO_IF[AIF_TRI_EN] bit must be set to program the audio interface on the TPS65950 for high impedance.
- McBSP3 is connected to the TPS65950 PCM interface. To use McBSP3 externally, the VOICE_IF[VIF_TRI_EN] bit must be set to program the PCM interface on the TPS65950 for high impedance.

2.15 UARTs

When using high-speed or continuous data transmission, the use of hardware flow control should be considered to guarantee correct delivery of data. Transitioning in and out of low-power modes or high processor utilization could cause receive first in, first out (FIFO) overruns.

2.16 Audio

The DM3730/AM3703 Torpedo SOM does not have on-board muting capability. External FETs must be added to CODEC_OUTL and CODEC_OUTR to provide muting capability. Use N-channel FETs and follow the design on the Torpedo Launcher 3 Baseboard, using J1.88/CONFIG3 (default MCSPI3_CLK) to turn on the FETs.

2.17 Ethernet

If you plan to use the SMSC Ethernet chip on the Torpedo Launcher 3 Baseboard, SMSC recommends adding 15 pF, 50V capacitors to ground on all four TPx signals to minimize EMI. Place these caps as close as possible to the magnetics.

When directly connecting the Ethernet port to another Ethernet device like a hub, magnetics are not required. Proper differential signaling layout rules must still be followed. Contact SMSC for the proper passives configuration.

The Atmel AT93C46D EEPROM seen on the Torpedo Launcher 3 Baseboard is no longer recommended for future designs. Recent review of the Atmel AT93C46D data sheet revealed that the maximum clock frequency is specified as 250 KHz, however the Microchip LAN9221 Ethernet Controller chip has a nominal clock frequency of 893 KHz for this EEPROM interface. The replacement Microchip 93AA46AT-I device has a maximum clock frequency specification of 1 MHz which better meets the specification of the LAN9221 Ethernet Controller chip.

NOTE: Always put down a serial EEPROM to hold the MAC address. Contact IEEE to obtain MAC addresses.

2.18 GPMC Bus

Customers looking to use the GPMC bus or alternate functions of the GPMC bus must consider the current reserved usage of the GPMC signals. Customers must consider signals dedicated for NAND access for modules populated with NAND memory. See Table 5.2 for information describing signals used for NAND access.

2.19 Reduce Boot Time

Customers looking to boot from NAND can reduce boot time by over one second simply by changing the boot order. The current boot order positions NAND as the last boot device. To change NAND to the first boot device, pull down SYS_BOOT5 during power up. This may be done through Logic PD's New Product Introduction (NPI) process or on the customer baseboard. This boot-time savings is in addition to what is offered by Logic PD's ZIP™[9] technology. Contact Logic PD for assistance in further reducing boot time.

3 Layout Checklist

Items listed in this section must be reviewed by the layout designers prior to releasing the Gerber design files for board production.

3.1 USB

Verify that the USB differential pairs listed below have an impedance match of 90 ohms:

- USB1_D+/USB1_D-

3.2 Decoupling Caps

Decoupling caps must be placed as close as possible to the targeted component.

3.3 Probe points

1. Provide probe points for critical signals that do not have resistors or capacitors.
2. Provide access to ground near high-speed signals and at points across the board.

3.4 Silkscreen

1. Logic PD recommends that the silkscreen display dots for every ten J1/J2 connector edge pins (e.g., 10, 20, 30, … 100).
2. Review all silkscreen markings to make sure nothing is covered due to vias or part placement.
3. Place tables of all possible jumper configurations on the silkscreen.
4. Label probe points for power supplies with the voltage.
5. Mark the baseboard silkscreen to show proper positioning of the DM3730/AM3703 Torpedo SOM. This can be done by providing an outline of the SOM and showing the two notched corners. Additionally, include an outline of the CPU and debug connectors to assist with proper insertion.

[9] http://www.logicpd.com/news/in-the-news/how-to-boot-linux-in-under-one-second/

3.5 DM3730/AM3703 Torpedo SOM Placement

1. Verify sufficient baseboard space exists in terms of height, width, and length for the DM3730/AM3703 Torpedo SOM per the recommended baseboard footprint in the *DM3730/AM3703 Torpedo SOM Hardware Specification*[10].
2. Keep bare vias, silkscreen, and any stickers out of the keep-out region on the baseboard SOM footprint. These can cause problems with the Z-height clearance for the module components. If changes to futures SOMs is required, maintaining the Z-height clearance is not guaranteed.
3. If planning to use a hold-down, verify that holes on the baseboard are present per the recommended baseboard footprint in *WP 419 Torpedo SOM Mechanical Hold-Down Scenarios*.[11]
4. Engineers should consider adding a copper pour with the use of a thermal pad to increase thermal dissipation. Refer to the *WP 491 DM3730 - AM3703 Torpedo SOM Thermal Management*[12] for additional information concerning thermal management.

4 Software Checklist

Items listed in this section must be reviewed by the software engineer prior to releasing software for testing.

1. Pull-ups/downs: Verify that software configures all signals that are not pull-ups, pull-downs, or present in hardware. A common oversight is to not use software to configure the pull-ups for nIRQx signals since they are not controlled by hardware.
2. Power Management: Verify the targeted BSP has the required power-management support to meet your system requirements.
3. If your LCD has power-sequencing requirements, ensure these are completed correctly.
4. If using a non-rechargeable RTC backup battery or an always-on power source, disable charging the backup battery in the BSP.
5. If using a rechargeable RTC backup battery, make sure charging is enabled in the BSP and that the voltage is set appropriately using TI's *TPS65950 OMAP Power Management and System Companion Device ES 1.2 TRM*.[13] See *AN 489 DM3730/AM3703 Torpedo SOM Power Management* for details.
6. If using a GPIO powered by VAUX4 or VPLL2, make sure the supply is enabled.
7. J1.88 (CONFIG3/MCSPI3_CLK/GPIO_17) is used by default as audio mute in a few Logic PD BSPs. Customers looking to use this signal for another function may need to update their BSP to disable the audio mute function.

5 Board Bring-Up Checklist

Items listed in this section can aid in system bring-up. Check the items in the order provided below.

1. Boot Sequence: Default for the DM3730/AM3703 Torpedo SOM is USB, UART3, MMC1, NAND.
2. Verify that LogicLoader boots to the `losh>` prompt. If it does not, continue checking the steps below.

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[10] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=52
[11] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=984
[12] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=605
[13] http://focus.ti.com/docs/prod/folders/print/tps65950.html#technicaldocuments

a. Power: Verify adequate power is applied to MAIN_BATTERY.

b. Reset In: Verify the MST_nRST signal goes high.

c. Reset Out: Verify the SYS_nRESWARM signal goes high.

d. Verify uP_UARTB_TX (J1.134) toggles since the internal boot ROM will attempt to boot from UART3 before SD or NAND.

e. GPIO: Verify that MCSPI2_SOMI and MCSPI2_SIMO toggle opposite of each other, as this indicates that the LogicLoader idle thread is running.

f. UARTA: Verify that serial output from the debug serial port shows the LogicLoader `losh>` prompt (the serial port must be set at baud rate: **115200**; data: **8-bit**; parity: **none**; stop: **1-bit**; flow control: **none**).

5.1 Bootloader Does Not Boot Successfully

If the bootloader does not boot successfully and everything through Step 2d above is working correctly, the boot ROM internal to the DM3730/AM3703 processor is failing to access your bootloader due to other problems.

By default, the DM3730/AM3703 Torpedo SOM signals the internal boot ROM to boot USB, UART, MMC1, and then NAND using the SYS_BOOT signals. This default configuration can be changed by pull resistors on the baseboard attached to LCD_D18 through LCD_D23 (SYS_BOOT0 – SYS_BOOT6).

If all SYS_BOOT signals are connected as expected and the bootloader still does not boot, check for possible problems with the signals listed in the sections below.

5.1.1 SOM Does Not Boot from SD Card

1. Verify that SD1_CLK is toggling. This is an indication that the internal boot ROM is trying to access the SD card.
2. Verify that your SD card is configured correctly and check to see that it boots in your DM3730 Torpedo Development Kit. If not, see information provided in the Logic PD FAQ: Why doesn't my OMAP3-based Development Kit boot from the SD Card?[14]

   The default boot order positions SD before NAND. In order for the processor to boot successfully, no shorts can exist for the connections associated with the signals listed in Table 5.1.

Table 5.1: MMC/SD Signals

SOM SD Signal	uP Signal	SOM Pin
VREF_SD1/MMC	VMMC1	J1.3
SD1_CLK	MMC1_CLK	J2.32
SD1_CMD	MMC1_CMD	J2.42
SD1_DATA0	MMC1_DAT0	J2.48
SD1_DATA1	MMC1_DAT1	J2.46
SD1_DATA2	MMC1_DAT2	J2.44
SD1_DATA3	MMC1_DAT3	J2.50
uP_GPIO_127	GPIO_127	J2.54

[14] http://www.logicpd.com/faqs/answer/why-doesnt-my-omap3-based-development-kit-boot-from-the-sd-card/

5.1.2 SOM Boots from SD Card but Not NAND Flash

Table 5.2 is a complete list of signals used to access the NAND flash on the DM3730/AM3703 Torpedo SOM; some signals are not accessible through the Torpedo connectors. If any of the signals in this table below have a short, the bootloader will not boot. Verify all signals are clear of shorts to successfully boot your system.

Table 5.2: NAND Signals

NAND Signal	uP Top Ball	uP Bottom Ball	uP Signal	SOM Signal	SOM Pin
I/O0	M2	K1	gpmc_d0	uP_D0	J1.35
I/O1	M1	L1	gpmc_d1	uP_D1	J1.37
I/O2	N2	L2	gpmc_d2	uP_D2	J1.33
I/O3	N1	P2	gpmc_d3	uP_D3	J1.39
I/O4	R2	T1	gpmc_d4	uP_D4	J1.49
I/O5	R1	V1	gpmc_d5	uP_D5	J1.57
I/O6	T2	V2	gpmc_d6	uP_D6	J1.53
I/O7	T1	W2	gpmc_d7	uP_D7	J1.55
I/O8	AB3	H2	gpmc_d8	uP_D8	J1.29
I/O9	AC3	K2	gpmc_d9	uP_D9	J1.31
I/O10	AB4	P1	gpmc_d10	uP_D10	J1.43
I/O11	AC4	R1	gpmc_d11	uP_D11	J1.45
I/O12	AB6	R2	gpmc_d12	uP_D12	J1.41
I/O13	AC6	T2	gpmc_d13	uP_D13	J1.47
I/O14	AB7	W1	gpmc_d14	uP_D14	J1.59
I/O15	AC7	Y1	gpmc_d15	uP_D15	J1.63
WE#	V1	F4	gpmc_nwe	uP_nWE	J1.1
RE#	V2	G2	gpmc_noe	uP_nOE	J1.15
ALE	W1	F3	gpmc_nadv_ale	uP_nADV_ALE	J1.23
CE0#	Y2	G4	gpmc_ncs0	uP_nCS0	J1.9
LOCK	AB9	AG11	POP_INT0_FT	uP_DREQ0	J1.30
WP#	AB10	H1	gpmc_nwp	uP_nWP	No connection
R/B#	AB12	M8	gpmc_wait0	Pulled up 1.8V	J1.26
CLE	AC12	G3	gpmc_nbe0_cle	uP_nBE0	J1.25
VCC	U1	A15	Feed through pins	VIO_1V8	VIO_1V8

6 TI DM3730/AM3703 Processor Schematic Checklist

Additional DM3730/AM3703 processor schematic checklist information can be found on the TI's *AM37x/DM37x Schematic Checklist* wiki page.[15] Though information provided in the TI checklist may not apply specifically to Logic PD hardware, it can be used as a reference. If there are any conflicts between the TI checklist and this Logic PD design checklist, please post a question to the Logic PD TDG forum.

[15] http://processors.wiki.ti.com/index.php/AM37x/DM37x_Schematic_Checklist

7 Summary

This application note is provided as a guide to use during development and bring-up of your platform. The ideas provided within this document may help reduce debug time and limit or eliminate future re-spins of your embedded system. Information provided in the *DM3730/AM3703 Torpedo SOM Hardware Specification* or any other specification document for onboard components takes precedence over the information within this application note.

Appendix A

The information below provides recommended source code changes in Linux for customers looking to use a MicroSD card instead of an SD card.

```
--- arch/arm/mach-omap2/board-omap3logic.c.orig    2014-01-22
14:56:32.616383999 -0600
+++ arch/arm/mach-omap2/board-omap3logic.c    2014-01-23
13:45:26.614619292 -0600
@@ -1116,20 +1116,21 @@
 };
 #endif

 static struct omap2_hsmmc_info __initdata board_mmc_info[] = {
     {
         .name        = "external",
         .mmc        = 1,
         .caps        = MMC_CAP_4_BIT_DATA,
         .gpio_cd    = -EINVAL,
         .gpio_wp    = -EINVAL,
+        .cover_only    = 1,
     },
     {
         .name        = "wl1271",
         .mmc        = 3,
         .caps        = MMC_CAP_4_BIT_DATA | MMC_CAP_POWER_OFF_CARD,
         .gpio_cd    = -EINVAL,
         .gpio_wp    = -EINVAL,
         .nonremovable    = true,
     },
     {}      /* Terminator */
@@ -1328,25 +1329,25 @@
 }

 static void __init board_mmc_init(void)
 {
     int ret;

     omap3torpedo_fix_pbias_voltage();

     if (machine_is_omap3530_lv_som() || machine_is_dm3730_som_lv()) {
         /* OMAP35x/DM37x LV SOM board */
-        board_mmc_info[0].gpio_cd = OMAP3530_LV_SOM_MMC_GPIO_CD;
-        board_mmc_info[0].gpio_wp = OMAP3530_LV_SOM_MMC_GPIO_WP;
+        //board_mmc_info[0].gpio_cd = OMAP3530_LV_SOM_MMC_GPIO_CD;
+        //board_mmc_info[0].gpio_wp = OMAP3530_LV_SOM_MMC_GPIO_WP;
         /* gpio_cd for MMC wired to CAM_STROBE; cam_strobe and
          * another pin share GPIO_126. Mux CAM_STROBE as GPIO. */
-        omap_mux_init_signal("cam_strobe.gpio_126", OMAP_MUX_MODE4 |
OMAP_PIN_INPUT_PULLUP);
+        //omap_mux_init_signal("cam_strobe.gpio_126", OMAP_MUX_MODE4 |
OMAP_PIN_INPUT_PULLUP);
     } else if (machine_is_omap3_torpedo() ||
machine_is_dm3730_torpedo()) {
         /* OMAP35x/DM37x Torpedo board */
-        board_mmc_info[0].gpio_cd = OMAP3_TORPEDO_MMC_GPIO_CD;
```



```
+         //board_mmc_info[0].gpio_cd = OMAP3_TORPEDO_MMC_GPIO_CD;
      } else {
          /* unsupported board */
          printk(KERN_ERR "%s(): unknown machine type\n", __func__);
          return;
      }

      /* Check the SRAM for valid product_id data(put there by u-boot).
*/
```

After making this change, you will need to edit the */etc/fstab* file for your SD card and mount and umount from the command line.

