DM3730/AM3703 SOM-LV Design Checklist

Application Note 490

Logic PD // Products
Published: July 2011
Last revised: March 2016

Abstract

This application note provides a list of items to verify when designing the DM3730/AM3703 SOM-LV into an embedded system. Reviewing this checklist prior to releasing design files and software for production can help reduce the probability of future board spins.

Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	RAH	-Initial release	NJK	07/20/11
B	RAH, SO	-Added Table 2.3; -Section 2.4: Added 80uF to Main_Battery requirement to list number 1; -Section 2.5: Added list number 2 regarding TRS3386 RS-232 transceiver	RAH	07/24/12
C	BSB, NJK	-Section 2.4: Added list number 2 and 3 regarding minimum battery threshold for device to power OFF and ON; -Section 2.12: Added information on voltage translator for MMC2; -Section 2.14: Added note to ensure the SOM PMIC can adequately recharge backup battery; added currently recorded consumption of BACKUP_BATT; added note that battery must provide sufficient power for entire length of time required by usage model; -Added Section 2.17; -Added Section 2.19	RAH, SO	01/25/13
D	SO	-Throughout: Updated template; updated links for new support site; -Table 2.3: Corrected SOM-LV pin numbers for signals SD1_CLK, SD1_CMD, SD1_DATA0, SD1_DATA1, SD1_DATA2, and SD1_DATA3;corrected SOM-LV signal names for pins J2.132, J2.128, and J2.136; -Section 0: Added list number 3 and 4 regarding additional LCD recommendations	RAH, NJK	12/05/13
E	BSB	-Throughout: Removed most "Contact Logic PD" links and pointed users to TDG forum instead; -Section 2.12: Added reference to example source code in Appendix A; -Added Section 2.18 regarding the GPMC bus; -Table 5.2: Corrected information for LOCK NAND signal; -Added Appendix A	SO	05/15/14
F	ABF	-Section 2.3: Explain power-on reset circuit -Section 2.7: Expand description of wake up. -Section 2.8: Fix typo when listing which pins get 10-ohm resistors -Section : Add note on what to do when there is no BACKUP_BATT	AM	07/16/14
G	BSB	-Section 2.7: Added information concerning using GPIO_128 and GPIO_156	BSB, AF	3/08/216

Table of Contents

1 Introduction

When using the DM3730/AM3703 SOM-LV in an embedded system, reviewing some specifics during the design phases can minimize or even eliminate future board spins. Information provided in this application note should be reviewed prior to releasing a design for fabrication and assembly. It is also critical that software teams review Sections 4 and 5 to ensure a trouble-free first board boot.

2 Schematic Checklist

Items in this section should be reviewed by the system designer prior to releasing the design for layout.

2.1 Analog-to-digital Converter Signals

Analog-to-digital converter (ADC) signals that are not used must have the connections outlined in Table 2.1 per the TPS65950 specification.

Table 2.1: Connections for Unused ADC Signals

ADC Signal	SOM-LV Signal Name	SOM-LV Pin	Connection	Resolution	Maximum Voltage Input
PMIC.START.ADC	START.ADC	J2.79	GND	—	1.8V
PMIC.ADCIN0	ADCIN0	J2.200	GND	10 bit	1.5V
PMIC.ADCIN1	ADCIN1	J2.198	GND	10 bit	1.5V
PMIC.ADCIN2	ADCIN2	J2.196	GND	10 bit	2.5V
PMIC.ADCIN3	A/D2	J1.200	GND	10 bit	2.5V
PMIC.ADCIN4	A/D3	J1.198	100nF CAP to GND	10 bit	2.5V
PMIC.ADCIN5	A/D4	J1.196	Floating	10 bit	2.5V
PMIC.ADCIN6	ADCIN6	J2.195	Floating	10 bit	2.5V
TSC2004	A/D1	J1.202	100nF CAP to GND	12 bit	3.0V

2.2 Clocks

Verify that series termination is available for all clock signals that do not have internal drive strength control.

2.3 Reset

The MSTR_nRST (J1.227) signal is driven by the on-board power management IC (PMIC), and it can only be driven low by external devices. Logic PD recommends avoiding an external power-on reset sequence.

MSTR_nRST can only be driven low; therefore, no pull-ups or active drivers must be used to drive MSTR_nRST.

2.4 Power

1. Verify all power and ground signals are connected correctly and are at the correct voltage level. Most importantly, MAIN_BATTERY should be driven directly by a

single-cell lithium-ion battery or a fixed, regulated power source. Connecting a minimum 80 uF capacitor to this rail on the baseboard is recommended.

2. For battery-powered designs, the minimum voltage supplied to MAIN_BATTERY at which the device will power ON is 3.2V +/- 100 mV. Note that 2.7V is the minimum threshold for the battery at which the device will power OFF once the system is running.
3. For non-battery-powered designs (i.e., MAIN_BATTERY is supplied by a fixed-voltage supply), the minimum voltage supplied to MAIN_BATTERY at which the device will power ON may be as high as 3.3V, depending on silicon variances. The fixed-voltage supply to MAIN_BATTERY must guarantee a minimum voltage of 3.3V, including any tolerance in the fixed-voltage supply or IR drop from the supply to the SOM. Note that once the system is running, the SOM will power off if MAIN_BATTERY falls below 2.7V.
4. Review Logic PD's *AN 488 DM3730/AM3703 SOM-LV Power Management*[1] for specific power interface connections.
5. Verify the recommended bulk capacitance is used; refer to *AN 488 DM3730/AM3703 SOM-LV Power Management* for requirements.
6. Verify the regulators provide sufficient current demands.
7. VAUX4 is not enabled by default in Logic PD software. This supply must be enabled before the signals listed below in Table 2.2 can be used. More details can be found in Logic PD's *AN 488 DM3730/AM3703 SOM-LV Power Management*.

2.5 Level Shifters

1. Verify whether or not any of the signals or buses used from the DM3730/AM3703 SOM-LV require level shifting for your specific design. In general, the SOM-LV is a 1.8V I/O module.
2. The TRS3386 RS-232 transceiver is no longer qualified to work at 1.8V. The TRS3253 is an alternative device that does support 1.8V operation.
3. Verify the correct reference voltage from the DM3730/AM3703 SOM-LV is used for signal level shifting or pull-ups.
4. Verify that the reference voltage is not used as a power source.
5. Verify that the direction signal has the proper direction control.
6. Verify that unused input signals to the level shifter are tied per the level-shifter specification and are not left floating.
7. For interface signals that have different directions (e.g., RX and TX), verify that the level shifters also have different direction signals.
8. Verify that the level shifter voltage requirements for VCCA and VCCB are being met. Most level shifters require VCCB to be higher, but this is not a guarantee.

2.6 Peripheral Interfaces

1. Verify peripheral interface connections, such as USB, serial, and MMC/SD card, are equivalent to those on the SDK2 Baseboard.
2. The Ethernet configuration on the SDK2 Baseboard supports several different PHY interfaces. Therefore, the recommended Ethernet configuration is to follow the SMSC *LAN9221 Reference Design*[2] schematic. See Section 2.13 for additional details about Ethernet magnetics.

[1] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=695
[2] www.smsc.com/media/Downloads_Public/lan9000/9221sch.pdf

2.7 GPIO

1. Verify the signal selected to be a GPIO is actually available as an alternative function or has a dedicated GPIO, GPI, or GPO function needed for the design.
2. Avoid using uP_GPIO_1 and uP_GPIO_0 as input or output signals in your design, as they are used to drive status LEDs from LogicLoader. Even if your system design will not use LogicLoader, it is recommended to avoid uP_GPIO_1 and uP_GPIO_0, and to use other available GPIO signals. If you do not plan to use these GPIOs, place easy-to-access test points so that they can be used for debugging.
3. Verify that no contention occurs on GPIO signals during reset and low-power mode states.
4. Verify that signals designated as GPIO have reset states with the desired direction and level.
5. Many of the GPIO pins for the DM3730/AM3703 SOM-LV are actually connected to the PMIC. Use all of the processor GPIO pins before using any GPIO pins connected to the PMIC. If your design absolutely requires the use of PMIC GPIO pins, please post a question to the Logic PD Technical Discussion Group (TDG) forum[3] for programming suggestions.
6. Do not connect to the SPI1 interface if your DM3730/AM3703 SOM-LV has Bluetooth; the SPI1 interface is dedicated for the Bluetooth chipset. Use the SPI3 interface instead.
7. uP_DREQ0 should be left floating at power-on; it is tied to the NAND flash LOCK pin and is read at power-on.
8. Verify the GPIO signals in Table 2.2 are used as input only (GPI) signals. **NOTE:** The VAUX4 supply powering these signals is not enabled by default in Logic PD software. This power supply must be enabled before these signals can be used.

Table 2.2: GPI Signals

uP GPIO Signal	SOM-LV Signal	SOM-LV Pin
GPIO_99	CSI_D0	J2.133
GPIO_100	CSI_D1	J2.135
GPIO_105	CSI_D6	J2.145
GPIO_106	CSI_D7	J2.147
GPIO_107	CSI_D8	J2.151
GPIO_108	CSI_D9	J2.153
GPIO_112	CSI1_DX0	J2.187
GPIO_113	CSI1_DY0	J2.185
GPIO_114	CSI_DX1	J2.183
GPIO_115	CSI_DY1	J2.181

[3] http://support.logicpd.com/TDGForum.aspx

9. Verify balls corresponding to the GPIO signals in Table 2.3 below have series termination due to buffer strength on these pads when muxed with MMC signals. Texas Instruments (TI) recommends starting with a 30 ohm dampening resistor. Changes to the resistor value may be necessary to reduce overshoot and undershoot signals, depending on the specific design requirements. TI recommends these signals be used as GPIOs only if no other solutions are possible. See "Section 25.2" in TI's *AM/DM37x Multimedia Device Technical Reference Manual (TRM)*[4] and TI's *SD-MMC Usage Notes on OMAP35x and AM37x* wiki page[5] for additional information.

Table 2.3: GPIO Signals with Series Termination

uP GPIO Signal	SOM-LV Signal	SOM-LV Pin
GPIO_120	SD1_CLK	J2.94
GPIO_121	SD1_CMD	J2.90
GPIO_122	SD1_DATA0	J2.88
GPIO_123	SD1_DATA1	J2.86
GPIO_124	SD1_DATA2	J2.84
GPIO_125	SD1_DATA3	J2.82
GPIO_126	SIM0_IO/TX	J2.132
GPIO_127	SIM0_CLK	J2.128
GPIO_129	SIM0_nRESET	J2.136

10. Verify that the GPIO signals used to wake up the processor have power to the I/O pads within the processor at the time the processor is in low-power mode. When only the WAKEUP power domain is active (ie, OFF mode), the following signals can be used to generate a direct wake-up event:

    - GPIO_1 (T2_CLKREQ) – Available on J2.231
    - GPIO_9 (uP_SYS_OFF_MODE) – Not routed externally
    - GPIO_10 (uP_CLKOUT1_26Mhz) – Available on J2.233
    - GPIO_11 (uP_GPIO_1) – Available on J1.216
    - GPIO_30 (SYS_nRESWARM) – Available on J1.225
    - GPIO_31 (uP_GPIO_2) – Available on J1.166

    For the rest of the GPIOs in the GPIO1 module (GPIO_0-31, not including the ones above), they can only generate wakeup events if the CORE power domain is active.

    For the GPIOs in module GPIO2-6 (ie, GPIO_32-191), they can only generate wakeup events if the PER power domain is active.

    Ensure that if you intend to use a GPIO as a wakeup event, you connect it to the appropriate GPIO signal.

    For GPIOs not listed above as wake-up sources, the processor provides a wake-up scheme controlled by the I/O daisy chain. This scheme allows GPIOs to be monitored while the PER power domain is off. GPIOs must be properly enabled before the PER power domain is disabled to function correctly as wake-up sources. Please reference "Section 3.5.7.2.2" of TI's *AM/DM37x Multimedia Device TRM* for more information on how to enable this feature.

11. VPLL2 supplies power to the GPIO signals listed in Table 2.4. Logic PD software only enables VPLL2 as part of the LCD initialization. Therefore, systems that do not use an LCD and require access to any of the GPIO signals in the table must enable the VPLL2 supply domain for the GPIO signals to work.

[4] http://focus.ti.com/docs/prod/folders/print/dm3730.html#technicaldocuments
[5] http://processors.wiki.ti.com/index.php/SD-MMC_Usage_Notes_on_OMAP35x_and_AM37x

Table 2.4: GPIO Signals

uP GPIO Signal	SOM-LV Signal	SOM-LV Pin
GPIO_70	LCD_D0	J1.211
GPIO_71	LCD_D1	J1.213
GPIO_72	LCD_D2	J1.215
GPIO_73	LCD_D3	J1.217
GPIO_74	LCD_D4	J1.219
GPIO_75	LCD_D5	J1.197
GPIO_80	LCD_D10	J1.207
GPIO_81	LCD_D11	J1.185
GPIO_82	LCD_D12	J1.187
GPIO_83	LCD_D13	J1.191
GPIO_84	LCD_D14	J1.193
GPIO_85	LCD_D15	J1.195
GPIO_92	LCD_D22	J2.176
GPIO_93	LCD_D23	J2.174

12. Verify balls connected to GPIO_6 and GPIO_7 are not pulled high or low during reset. These GPIO signals are shared with SYS_BOOT signals that are polled at reset to set the boot sequence.

Table 2.5: SYS_BOOT Signals

uP GPIO Signal	SOM-LV Signal	SOM-LV Pin
GPIO_6	uP_PCC_RESET	J2.34
GPIO_7	uP_UARTA_DTR	J1.156

13. When using signals associated to GPIO_128 and GPIO_156, be sure to use the connections as indicated in the table below. These signals are incorrectly labeled on the baseboard.

Table 2.6: GPIO_128 and GPIO_156

DM37x Processor		SOM-LV Schematics		Baseboard Schematic	
Ball	**Alt. Functions**	**Label**	**Pin**	**Label**	**Pin**
Y21	McBSP1_CLKR/McSPI4_CLK/SIM_CD/GPIO_156	SIM0_nDETECT	J2.126	SIM0_VEN	J2.126
R27	SIM_PWRCTRL/GPIO_128	SIM0_VEN	J2.13, J2.15, J2.124	SIM0_nDETECT	J2.124

2.8 LCD

1. The recommended LCD interface is to support 16-bit (5:6:5) or 24-bit (8:8:8) color. Please post a question on the Logic PD TDG forum for additional information about supporting other color depths.
2. Verify that the targeted LCD works by using LogicLoader scripts to interface with the Zoom™ DM3730 SOM-LV Development Kit. Please post a question on the Logic PD TDG forum if assistance is needed.

3. Add 10 ohm series termination resistors to all data lines, HSYNC, VSYNC, ACBIAS, and PCLK.
4. See TI's *AM37x/DM37x Schematic Checklist* wiki page[6] for additional information about the Display Sub-System.

2.9 Debug

1. Serial: Logic PD recommends all designs have a debug serial port. This port is used for terminal access to LogicLoader and Linux. Also, Windows CE debug messages can be enabled to output to the debug serial port. uP_UARTA_TX and uP_UARTA_RX are the dedicated debug port signals used on the DM3730/AM3703 SOM-LV.
2. JTAG: The JTAG interface and voltage required for your tools may be different than those used on the SDK2 Baseboard. Verify that the JTAG connector interface for your design will interface to the emulator that is planned for software development.
3. Ethernet: Logic PD recommends putting down a WLAN Ethernet port on the first phase of baseboards; this port can be used for development and download purposes.
4. Serial-to-USB: Logic PD recommends copying this reference from the SDK2 Baseboard only if the host PC does not have a RS232 serial interface.
5. Reset: Logic PD recommends designing in a debounced MSTR_nRST button to the DM3730/AM3703 SOM-LV to aid in debug.
6. GPIO: Connect LED to GPIO_0 and GPIO_1 to act as status indicators during board bring-up. At a minimum, provide test-point access to these signals.

2.10 I/O Interface

Verify that any signal driven from the DM3730/AM3703 SOM-LV has no more than one load. A buffer must be used if more than one load is required to be driven from the SOM-LV in your design.

2.11 USB OTG VBUS

A 4.7 uF capacitor must connect J1.21 (USB1_VBUS) to ground.

USB1_VBUS (J1.21) is driven by the TPS65950 and can only supply 100 mA of current on VBUS. If more than 100 mA is required, it is possible to design an external VBUS supply to coexist with the USB1_VBUS signal. When using an external VBUS supply, the OTG_CTRL[DRVVBUS] signal in the TPS65950 must be cleared at all times. The USB1_VBUS signal must also be tied to the output of the external VBUS supply to allow for detection of the TPS65950 VBUS.

2.12 Secure Digital/MicroSD Card Detect

When Secure Digital (SD) or MicroSD cards are used in a system design, signal J1.113 (CSI_D11) is configured by LogicLoader as a card detect signal. For card sockets that do not have a card detect pin, J1.113 (CSI_D11) must be grounded on the customer baseboard for LogicLoader to work properly. Example source code changes when using a MicroSD card with Linux are provided in Appendix A.

J1.115 (uP_nIRQC) is also designated as an SD write-protection signal when SD is used; this signal must be grounded on the custom baseboard for writes to work properly in LogicLoader. If write access is not desired, this signal should be connected to VMMC1 through a pull-up resistor to enable write protection of the card.

[6] http://processors.wiki.ti.com/index.php/AM37x/DM37x_Schematic_Checklist#DSS

Voltage-level translation is required to support 3.0V cards on the MMC2 interface. An 8-bit, bidirectional voltage-level translator for open-drain and push-pull applications allows for voltage translation without the need of direction control signals. Logic PD has used the TXS0108E[7] from TI in several designs.

2.13 Ethernet

1. The Ethernet controller on the DM3730/AM3703 SOM-LV is an SMSC LAN9221 component. SMSC's *Application Note 8.13*[8] lists magnetics that are suggested for use with their SMSC LANxxxx components.

   The RJ-45 Ethernet connector on the SDK2 Baseboard (reference designator P1; Pulse J0026) was chosen to support multiple SOM-LV configurations with different Ethernet controllers. While not electrically identical to the magnetics suggested by SMSC, it has proven to be functional under all testing performed by Logic PD. Logic PD has not verified full functionality of the J0026 magnetics with the SMSC 9221 Ethernet controller under the IEEE 802.3 speciation. Logic PD recommends customers design-in magnetics, or their electrical equivalent, as suggested by SMSC. Figure 2.1 below is an example magnetics design suggested by SMSC.

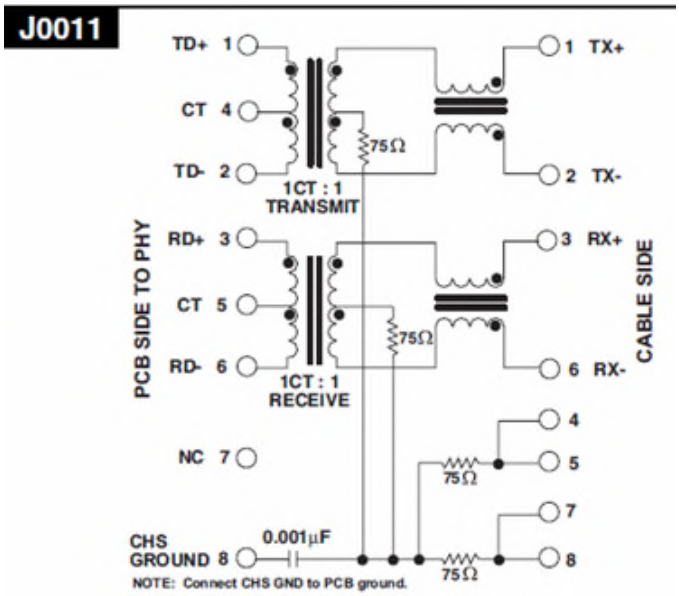

Figure 2.1: Example Magnetics Design, Pulse J0011

2. When connecting the magnetics to the SMSC LAN9221 on the DM3730/AM3703 SOM-LV, the following connections must be followed to match the SMSC LAN9221 reference design:

   a. Connect the transmit and receive center taps together.

   b. Tie a 10 ohm (1/8W 1%) resistor between VREF_ETHERNET (J1.26) and the center tap signals of the magnetics.

   c. Connect a 0.22 uF (0805) capacitor from center tap signal to digital ground.

3. SMSC recommends adding 15 pF, 50V capacitors to ground on all four TPx lines to minimize EMI. Place these capacitors as close as possible to the magnetics.

4. If you plan to directly connect the Ethernet port to another Ethernet device, such as a hub, magnetics are not required. Proper differential signaling layout rules must still be followed; contact SMSC for the proper passives configuration.

[7] http://www.ti.com/product/txs0108e
[8] http://www.smsc.com/Downloads/SMSC/Downloads_Public/Application_Notes/an813.pdf

2.14 Real-Time Clock Battery Backup

If your design uses a rechargeable battery to back up the real-time clock (RTC) on the TPS65950, do not place any capacitors on the BACKUP_BATT rail. Doing so will prevent the TPS65950 from charging the backup battery.

Verify the rechargeable backup battery targeted for your design can be adequately charged by the DM3730/AM3703 SOM-LV PMIC. The PMIC provides a constant current that can be set at 25 uA, 150 uA, 500 uA, or 1 mA. The available cutoff voltages for the backup battery are 2.5V, 3.0V, 3.1V or 3.2V. Inadequate charging could prevent the backup battery from being fully charged.

If your design uses a non-rechargeable battery, place a diode on BACKUP_BATT to prevent accidental charging of the battery.

Current consumption on BACKUP_BATT has been measured as high as 50 uA but is typically 10 uA. Choose a battery, rechargeable or not, that can supply sufficient power for the entire length of time required by your usage model. For example, if your usage model leaves MAIN_BATT disconnected for a total of six months over a product life cycle, a backup battery of at least 216 mAh is required, such as a CR2032.

Please refer to *AN 488 DM3730/AM3703 SOM-LV Power Management* for details on connections.

If your design is not powering the BACKUP_BATT signal it must be connected to ground.

2.15 McBSP

The DM3730/AM3703 SOM-LV can support up to five McBSP ports. Of the five McBSP ports, McBSP2 and McBSP3 are connected to the TPS65950; McBSP3 is connected to the Bluetooth module.

- McBSP2 is connected to the TPS65950 audio interface. To use McBSP2 externally, the AUDIO_IF[AIF_TRI_EN] bit must be set to program the audio interface on the TPS65950 for high impedance.
- McBSP3 is connected to the TPS65950 PCM interface and Bluetooth radio. For DM3730/AM3703 SOM-LV configurations that do not have Bluetooth components populated, McBSP3 can be used externally by setting the VOICE_IF[VIF_TRI_EN] bit to program the PCM interface on the TPS65950 for high impedance.

2.16 UARTs

When using high-speed or continuous data transmission, consider implementing hardware flow control to guarantee correct delivery of data. Transitioning in and out of low-power modes or high processor utilization may cause first in, first out (FIFO) errors.

2.17 Wireless

For designs requiring the use of Bluetooth and Wi-Fi concurrently, please post a question on the Logic PD TDG forum for assistance.

2.18 GPMC Bus

Customers looking to use the GPMC bus or alternate functions of the GPMC bus must consider the current reserved usage of the GPMC signals. Customers must consider signals dedicated for NAND access for modules populated with NAND memory. See Table 5.2 for information describing signals used for NAND access.

2.19 Reduce Boot Time

Customers looking to boot from NAND can reduce boot time by over one second simply by changing the boot order. The current boot order positions NAND as the last boot device. To change NAND to the first boot device, pull down SYS_BOOT5 during power up. This may be done through Logic PD's New Product Introduction (NPI) process or on the customer baseboard. This boot-time savings is in addition to what is offered by Logic PD's Zip™[9] technology. Contact Logic PD[10] for assistance in further reducing boot time.

3 Layout Checklist

Items listed in this section should be reviewed by the layout designers prior to releasing the Gerber design files for board production.

3.1 USB

Verify that the following USB differential pairs have an impedance match of 90 ohms:

- USB1_D+/USB1_D-
- USB2_D+/USB2_D-
- USB4_D+/USB4_D-
- USB5_D+/USB5_D-

3.2 Ethernet

Verify that the following Ethernet differential signals have an impedance match of 100 ohms:

- ETHER_RX+/ETHER_RX-
- ETHER_TX+/ETHER_TX-

3.3 Decoupling Caps

Decoupling caps must be placed as close as possible to the targeted component.

3.4 Silkscreen

1. Logic PD recommends that the silkscreen display dots for every ten J1/J2 connector edge pins (e.g., 10, 20, 30, … 240).
2. Review all silkscreen markings to make sure nothing is covered due to vias or part placement.

3.5 SOM-LV Placement

1. Verify sufficient baseboard space exists in terms of height, width, and length for the DM3730/AM3703 SOM-LV per the recommended baseboard footprint in the *DM3730/AM3703 SOM-LV Hardware Specification*.[11]
2. Verify that mounting holes on the baseboard are present per the recommended baseboard footprint in the *DM3730/AM3703 SOM-LV Hardware Specification.*

[9] http://www.logicpd.com/products/software/zip/
[10] http://www.logicpd.com/contact/inquiry/
[11] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=706

4 Software Checklist

Items listed in this section should be reviewed by the software engineer prior to releasing software for testing.

1. Pull-ups/downs: Verify that software configures all signals that are not pull-ups, pull-downs, or present in hardware. A common oversight is to not use software to configure the pull-ups for nIRQx signals since they are not controlled by hardware.
2. Power management: Verify the targeted BSP has the required power-management support to meet your system requirements.
3. If using GPI signals listed in Table 2.2, verify the VAUX4 supply is enabled at the correct voltage. Details can be found in *AN 488 DM3730/AM3703 SOM-LV Power Management*.

5 Board Bring-Up Checklist

Items listed in this section can aid in system bring-up. Check the items in the order provided below. If you experience problems booting, proceed through Section 5.1 to troubleshoot this issue.

1. Know your boot sequence. The default for the DM3730/AM3703 SOM-LV is USB, UART3, MMC1, NAND. See page 10 of the *DM3730/AM3703 SOM-LV Schematics* for available boot sequences.
2. Verify that LogicLoader boots to the `losh>` prompt using the Zoom™ DM3730 SOM-LV Development Kit. If it does not, continue checking the steps below.
    a. Power: Verify adequate power is applied to MAIN_BATTERY.
    b. Reset In: Verify the MSTR_nRST (J1.227) signal goes high.
    c. Reset Out: Verify the SYS_nRESWARM (J1.225) signal goes high.
    d. Verify uP_UARTB_TX (J1.134) toggles since the internal boot ROM will attempt to boot from UART3 before SD or NAND.
    e. GPIO: Verify that GPIO_0 (J1.218) and GPIO_1 (J1.216) toggle opposite of each other, as this is an indication that the LogicLoader idle thread is running.
    f. UARTA: Verify that serial output from the debug serial port shows the LogicLoader `losh>` prompt (the serial port must be set at: baud rate: **115200**; data: **8-bit**; parity: **none**; stop: **1-bit**; flow control: **none**).

5.1 Bootloader Does Not Boot Successfully

If the bootloader does not boot successfully and everything through Step 2d above is working correctly, the boot ROM internal to the DM3730/AM3703 processor is failing to access your bootloader due to other problems.

By default, the DM3730/AM3703 SOM-LV signals the internal boot ROM to boot USB, UART, MMC1, and then NAND using the SYS_BOOT signals. This default configuration can be changed by populating R73 (SYS_BOOT5), R45 (SYS_BOOT0), or R44 (SYS_BOOT3); or by changing the default state at the reset of SYS_BOOT4 or SYS_BOOT5 on the baseboard. Changes to the SYS_BOOT sequence could also prevent the bootloader from running.

If all SYS_BOOT signals are connected as expected and the bootloader still does not boot, check for possible problems with the signals listed in the sections below.

5.1.1 SOM Does Not Boot from SD Card

1. Verify that SD1_CLK is toggling. This is an indication that the internal boot ROM is trying to access the SD card.
2. Verify that your SD card is configured correctly and check to see that it boots in your Zoom™ DM3730 SOM-LV Development Kit. If not, see information provided in the Logic PD FAQ: Why doesn't my OMAP3-based Development Kit boot from the SD card?[12]

   The default boot order positions SD before NAND. In order for the processor to boot successfully, no shorts can exist for the connections associated with the signals listed in Table 5.1.

Table 5.1: MMC/SD Signals

SOM-LV SD Signal	uP Signal	SOM-LV Pin
VREF_SD1/MMC	VMMC1	J2.80
SD1_CLK	MMC1_CLK	J2.94
SD1_CMD	MMC1_CMD	J2.90
SD1_DATA0	MMC1_DAT0	J2.88
SD1_DATA1	MMC1_DAT1	J2.86
SD1_DATA2	MMC1_DAT2	J2.84
SD1_DATA3	MMC1_DAT3	J2.82
CSI_D11 (uP_nIRQD)	GPIO_110	J1.113, J2.157

[12] http://www.logicpd.com/faqs/answer/why-doesnt-my-omap3-based-development-kit-boot-from-the-sd-card/

5.1.2 SOM Boots from SD Card but Not NAND Flash

Table 5.2 is a complete list of signals used to access the NAND flash on the DM3730/AM3703 SOM-LV; some signals are not accessible through the SOM-LV connectors. If any of the signals in this table below have a short, the bootloader will not boot. Verify all signals are clear of shorts to successfully boot your system.

Table 5.2: NAND Signals

NAND Signal	uP Top Ball	uP Bottom Ball	uP Signal	SOM-LV Signal	SOM-LV Pin
I/O0	M2	K1	gpmc_d0	uP_D0	J1.40
I/O1	M1	L1	gpmc_d1	uP_D1	J1.42
I/O2	N2	L2	gpmc_d2	uP_D2	J1.44
I/O3	N1	P2	gpmc_d3	uP_D3	J1.46
I/O4	R2	T1	gpmc_d4	uP_D4	J1.48
I/O5	R1	V1	gpmc_d5	uP_D5	J1.50
I/O6	T2	V2	gpmc_d6	uP_D6	J1.54
I/O7	T1	W2	gpmc_d7	uP_D7	J1.56
I/O8	AB3	H2	gpmc_d8	uP_D8	J1.58
I/O9	AC3	K2	gpmc_d9	uP_D9	J1.60
I/O10	AB4	P1	gpmc_d10	uP_D10	J1.62
I/O11	AC4	R1	gpmc_d11	uP_D11	J1.64
I/O12	AB6	R2	gpmc_d12	uP_D12	J1.66
I/O13	AC6	T2	gpmc_d13	uP_D13	J1.68
I/O14	AB7	W1	gpmc_d14	uP_D14	J1.70
I/O15	AC7	Y1	gpmc_d15	uP_D15	J1.74
WE#	V1	F4	gpmc_nwe	uP_nWE	J1.127, J2.40
RE#	V2	G2	gpmc_noe	uP_nOE	J1.125, J2.14
ALE	W1	F3	gpmc_nadv_ale	uP_nADV_ALE	J2.87
CE0#	Y2	G4	gpmc_ncs0	uP_nCS0	No connection
LOCK	AB9	AG11	POP_INT0_FT	uP_DREQ0	J1.133
WP#	AB10	H1	gpmc_nwp	uP_nWP	J2.85
R/B#	AB12	M8	gpmc_wait0	Pulled up 1.8V	No connection
CLE	AC12	G3	gpmc_nbe0_cle	uP_nBE0	J1.137
VCC	U1	A15	Feed through pins	VIO_1V8	VIO_1V8

6 TI Schematic Checklists

Additional schematic checklist information for the DM3730/AM3703 processor and TPS65950 PMIC can be found on TI's *AM37x/DM37x Schematic Checklist* wiki page[13] and in TI's *TPS65950 Schematic Checklist*[14] document. Although information provided in the TI checklists may not apply specifically to Logic PD hardware, it can be used as a reference. If conflicts exist between TI's checklists and this Logic PD design checklist, please post a comment on the Logic PD TDG forum.

7 Summary

This application note is provided as a guide to use during the development and bring-up of your platform. The ideas provided within this document may help reduce debug time and limit or eliminate future re-spins of your embedded system. Information provided in the *DM3730/AM3703 SOM-LV Hardware Specification* or any specification document for onboard components takes precedence over the information within this application note.

[13] http://processors.wiki.ti.com/index.php/AM37x/DM37x_Schematic_Checklist
[14] http://www.ti.com/product/tps65950#technicaldocuments

Appendix A

The information below provides recommended source code changes in Linux for customers looking to use a MicroSD card instead of an SD card.

```
--- arch/arm/mach-omap2/board-omap3logic.c.orig    2014-01-22
14:56:32.616383999 -0600
+++ arch/arm/mach-omap2/board-omap3logic.c    2014-01-23
13:45:26.614619292 -0600
@@ -1116,20 +1116,21 @@
 };
 #endif

 static struct omap2_hsmmc_info __initdata board_mmc_info[] = {
     {
         .name        = "external",
         .mmc        = 1,
         .caps        = MMC_CAP_4_BIT_DATA,
         .gpio_cd    = -EINVAL,
         .gpio_wp    = -EINVAL,
+        .cover_only    = 1,
     },
     {
         .name        = "wl1271",
         .mmc        = 3,
         .caps        = MMC_CAP_4_BIT_DATA | MMC_CAP_POWER_OFF_CARD,
         .gpio_cd    = -EINVAL,
         .gpio_wp    = -EINVAL,
         .nonremovable    = true,
     },
     {}      /* Terminator */
@@ -1328,25 +1329,25 @@
 }

 static void __init board_mmc_init(void)
 {
     int ret;

     omap3torpedo_fix_pbias_voltage();

     if (machine_is_omap3530_lv_som() || machine_is_dm3730_som_lv()) {
         /* OMAP35x/DM37x LV SOM board */
-        board_mmc_info[0].gpio_cd = OMAP3530_LV_SOM_MMC_GPIO_CD;
-        board_mmc_info[0].gpio_wp = OMAP3530_LV_SOM_MMC_GPIO_WP;
+        //board_mmc_info[0].gpio_cd = OMAP3530_LV_SOM_MMC_GPIO_CD;
+        //board_mmc_info[0].gpio_wp = OMAP3530_LV_SOM_MMC_GPIO_WP;
         /* gpio_cd for MMC wired to CAM_STROBE; cam_strobe and
          * another pin share GPIO_126. Mux CAM_STROBE as GPIO. */
-        omap_mux_init_signal("cam_strobe.gpio_126", OMAP_MUX_MODE4 |
OMAP_PIN_INPUT_PULLUP);
+        //omap_mux_init_signal("cam_strobe.gpio_126", OMAP_MUX_MODE4 |
OMAP_PIN_INPUT_PULLUP);
     } else if (machine_is_omap3_torpedo() ||
machine_is_dm3730_torpedo()) {
         /* OMAP35x/DM37x Torpedo board */
         board_mmc_info[0].gpio_cd = OMAP3_TORPEDO_MMC_GPIO_CD;
```



```
    } else {
        /* unsupported board */
        printk(KERN_ERR "%s(): unknown machine type\n", __func__);
        return;
    }

    /* Check the SRAM for valid product_id data(put there by u-boot).
*/
```

After making this change, you will need to edit the */etc/fstab* file for your SD card and mount and umount from the command line.

