OMAP35x Torpedo™ SOM Design Checklist

Application Note 417

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Abstract

This application note provides a list of items to verify when designing the OMAP35x Torpedo SOM into an embedded system. Reviewing this checklist prior to releasing design files and software for production can help reduce the probability of future board spins.

Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	RAH	-Initial release of document.	JCA	03/12/10
B	JCA	-Section 2.11: Corrected pin number for USB1_VBUS; -Added Section 2.12 about SD/MMC card detect	BSB	05/28/10
C	BSB, JCA	-Section 2.7: Added item 11 about VPLL2 supply and added Table 2.3; -Added Section 5 about TI OMAP35x processor schematic checklist	BSB	07/09/10
D	BSB	-Section 2.7: Removed wake-up signals not accessible to the user; -Section 2.11: Added information about 100mA limit on VBUS; -Added Section 2.13 about McBSP	BSB	09/03/10
E	BSB, NJK	-Section 2.7: #8 Added dampening resistor requirement; Added item #12 about SYS_BOOT signals; -Section 5: Added link for TPS65950 schematic checklist	BSB	12/15/10
F	SMC, BSB	-Section 2.6: Minor updates to peripheral interfaces; -Section 2.15: Added UART information; -Section 5: Expanded Board Bring-Up Checklist	NJK	06/09/11
G	BSB, NJK	-Section 2.4: Added list number 2 and 3 regarding minimum battery threshold for device to power OFF and ON; added list number 8 regarding the BQ27000 fuel gauge; -Section 2.5: Added list number 2 regarding TRS3386 RS-232 transceiver; -Section 2.7: Removed LCD_D18 – LCD_D21 from the signals affected by VPPL2; -Added Section 2.13; -Added Section 2.18	RAH, SO	01/25/13
H	HJS	-Throughout: Updated template - no change to content; updated links for new support site	SO	09/19/13
I	SO	-Section 3.4: Updated list number 5 with additional recommendation to add outline of CPU and debug connectors	RAH	11/26/13

Table of Contents

1 Introduction

When using the OMAP35x Torpedo SOM in an embedded system, reviewing some specifics during the design phases can minimize or even eliminate future board spins. Information provided in this application note should be reviewed prior to releasing a design for fabrication and assembly. It is also critical that software teams review Sections 4 and 5 to ensure a trouble-free first board boot.

2 Schematic Checklist

Items in this section should be reviewed by the system designer prior to releasing the design for layout.

2.1 Analog-to-digital Converter Signals

Analog-to-digital converter (ADC) signals that are not used must have the following connections per the TPS65950 specification:

Table 2.1: Connections for Unused ADC Signals

ADC Signal	SOM Signal Name	SOM Pin	Connection	Maximum Voltage Input
PMIC.ADCIN0	CONFIG11	J1.76	GND	1.5V
PMIC.ADCIN1	CONFIG10	J1.78	GND	1.5V
PMIC.ADCIN2	CONFIG9	J1.80	GND	2.5V
PMIC.ADCIN3	CONFIG8	J1.82	GND	2.5V

2.2 Clocks

Verify that series termination is available for all clock signals that do not have internal drive strength control.

2.3 Reset

The MSTR_nRST signal is driven by the on-board power management IC (PMIC); therefore, Logic PD recommends avoiding an external power-on reset sequence.

2.4 Power

1. Verify all power and ground signals are connected correctly and are at the correct voltage level.
2. For battery-powered designs, the minimum voltage supplied to MAIN_BATTERY at which the device will power ON is 3.2V +/- 100 mV. Note that 2.7V is the minimum threshold for the battery at which the device will power OFF once the system is running.
3. For non-battery-powered designs (i.e., MAIN_BATTERY is supplied by a fixed-voltage supply), the minimum voltage supplied to MAIN_BATTERY at which the device will power ON may be as high as 3.3V, depending on silicon variances. The fixed-voltage supply to MAIN_BATTERY must guarantee a minimum voltage of 3.3V, including any tolerance in the fixed-voltage supply or IR drop from the supply to the SOM. Note that once the system is running, the SOM will power off if MAIN_BATTERY falls below 2.7V.

4. Review Logic PD's *AN 416 OMAP35x Torpedo SOM Power Management*[1] for specific power interface connections.
5. Verify the recommended bulk capacitance is used; refer to the OMAP35x Torpedo SOM Power Management Application Note for requirements.
6. Verify the regulator provides sufficient current to meet demands, including any peripherals powered by the OMAP35x Torpedo SOM.
7. Note that VAUX4 is not enabled by default in Logic PD software. This supply must be enabled before using the signals in Table 2.2. Refer to the OMAP35x Torpedo SOM Power Management Application Note for details.
8. The battery fuel gauge shown in the reference design, a TI BQ27000, requires 21V to program some of the registers for the best performance. There is currently no software support for this fuel gauge in Logic PD's board support packages (BSPs). Please refer to the Texas Instruments (TI) BQ27000 product page[2] for more information on this fuel gauge.

2.5 Level Shifters

1. Verify if any of the signals or busses used from the OMAP35x Torpedo SOM need level shifting for your specific design. In general, the SOM is a 1.8V I/O module.
2. The TRS3386 RS-232 transceiver is no longer qualified to work at 1.8V. The TRS3253 is an alternative device that does support 1.8V operation.
3. Verify the correct reference voltage from the OMAP35x Torpedo SOM is used for signal level shifting or pull-ups.
4. Verify that the reference voltage is not used as a power source, except within the limits allowed.
5. Verify that the direction signal has the proper direction control.
6. Verify that unused level-shifter input signals are tied per the level-shifter specification and are not left floating (unless required by the specification).
7. For interface signals that have different directions (e.g., RX and TX), verify that the level shifters also have different direction signals.

2.6 Peripheral Interfaces

1. Verify peripheral interface connections are equivalent to those on the OMAP35x Torpedo Launcher Baseboard, such as USB, serial, MMC/SD, and CompactFlash.
2. If you plan to use a custom population option of the CONFIG resistors, note that on the schematics and contact Logic PD[3] to begin the new product introduction (NPI) process. Be sure to include the NPI turn-around time in your schedule.

2.7 GPIO

1. Verify the signal selected to be a GPIO is actually available as an alternative function or is a dedicated GPIO, GPI, or GPO function needed for the design.
2. Do not use MCSPI2_SOMI and MCSPI2_SIMO as input or output signals in your design, as they are used to drive status LEDs from LogicLoader. Even if your system design will not use LogicLoader, it is recommended to use other available GPIO signals and avoid MCSPI2_SOMI and MCSPI2_SIMO.
3. Verify that no contention occurs on GPIO signals during reset and low-power mode states.

[1] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=964
[2] http://www.ti.com/product/bq27000
[3] http://support.logicpd.com/TechnicalSupport/AskAQuestion.aspx

4. Verify that signals designated as GPIO have reset states with the desired direction and level.
5. BT_PCM_DR and BT_PCM_DX from the OMAP35x Torpedo SOM are actually connected to the PMIC. Use all of the processor GPIO pins before using GPIO pins connected to the PMIC. If your design absolutely requires the use of PMIC GPIO pins, please contact Logic PD for programming suggestions.
6. uP_DREQ0 should be left floating at power on; it is tied to the NAND flash LOCK pin and is read at power on.
7. Verify the GPIO signals in Table 2.2 are used as input only (GPI) signals.

Table 2.2: GPI Signals

uP GPIO Signal	SOM Signal Name	SOM Pin
gpio_99	CSI_D0	J2.85
gpio_100	CSI_D1	J2.87

8. Verify balls corresponding to signals gpio_120 to gpio_129 (when muxed with MMC signals) have series termination due to buffer strength on these pads; TI recommends starting with a 30 ohm dampening resistor. Changes to the resistor value may be necessary to reduce overshoot and undershoot signals, depending on the specific design requirements. See Section 24.2 in TI's *OMAP35x Technical Reference Manual (TRM)*[4] and TI's *SD-MMC Usage Notes on OMAP35x and AM37x* wiki page[5] for additional information.
9. Verify that GPIO signals used to wake up the processor have power to the I/O pads within the processor at the time the processor is in low-power mode. The following signals can be used to generate a direct wake-up event:
    - uP_CLKOUT1_26MHz
    - GPIO_30 (SYS_nRESWARM)
10. The other GPIO1 pins (gpio_[31:0]) cannot be used to generate a direct wake-up event because they are connected to the device I/O pad logic in the CORE power domain (VDD2). When the CORE power domain is off, the I/O pins of the GPIO1 module, which are supplied by VDD2, cannot generate a wake-up event. The wake-up capabilities of the GPIO2 to GPIO6 modules are operational only when the PER power domain is active.
11. VPLL2 supplies power to the GPIO signals listed in Table 2.3. Logic PD software only enables VPLL2 as part of the LCD initialization. Therefore, systems that do not use LCD and require access to any of the GPIO signals in the table must enable the VPLL2 supply domain for the GPIO signals to work.

Table 2.3: GPIO Signals

uP GPIO Signal	SOM Signal	SOM Pin
gpio_70	LCD_D0	J2.98
gpio_71	LCD_D1	J2.83
gpio_72	LCD_D2	J2.79
gpio_73	LCD_D3	J2.81
gpio_74	LCD_D4	J2.94
gpio_75	LCD_D5	J2.96
gpio_80	LCD_D10	J2.82
gpio_81	LCD_D11	J2.84

[4] http://focus.ti.com/docs/prod/folders/print/omap3530.html#technicaldocuments
[5] http://processors.wiki.ti.com/index.php/SD-MMC_Usage_Notes_on_OMAP35x_and_AM37x

uP GPIO Signal	SOM Signal	SOM Pin
gpio_82	LCD_D12	J2.70
gpio_83	LCD_D13	J2.68
gpio_84	LCD_D14	J2.66
gpio_85	LCD_D15	J2.78
gpio_92	LCD_D22	J2.80
gpio_93	LCD_D23	J1.87 (CONFIG2)

12. Verify balls connected to gpio_2 and gpio_7 are not pulled high or low during reset. These GPIO signals are shared with SYS_BOOT signals that are polled at reset to set the boot sequence.

Table 2.4: SYS_BOOT Signals

uP GPIO Signal	SOM Signal	SOM Pin
gpio_2	SYS_BOOT0	J2.100
gpio_7	SYS_BOOT5	J2.89

2.8 LCD

1. The recommended LCD interface is to support 16-bit (5:6:5) color. Contact Logic PD about supporting other color depths.
2. Verify that the targeted LCD works by using LogicLoader scripts to interface with the OMAP35x Torpedo Launcher Baseboard. Contact Logic PD for assistance, if needed.
3. If your LCD requires a specific power supply startup sequence, use LCD_PANEL_PWR to initiate the sequence and use LCD_BACKLIGHT_PWR to control the backlight. This will align with the OS software provided by Logic PD.

2.9 Debug

1. Serial: Logic PD recommends all designs have a debug serial port. This port is used for terminal access to LogicLoader and Linux. Also, Windows CE debug messages can be enabled to output to the debug serial port. uP_UARTA_TX and uP_UARTA_RX are the dedicated debug port signals used on the OMAP35x Torpedo SOM.
2. JTAG: The JTAG interface and voltage required for your tools may be different than those used on the OMAP35x Torpedo SOM. Verify that the JTAG connector interface on the OMAP35x Torpedo SOM will interface to the emulator that is planned for software development.
3. Ethernet: Logic PD recommends putting down a WLAN Ethernet port on the first pass of baseboards. This port can be used for development and download purposes and can be copied from the OMAP35x Torpedo Launcher Baseboard.
4. Reset: Logic PD recommends designing in a debounced MSTR_RST button to the OMAP35x Torpedo SOM to aid in debug.
5. GPIO: Connect LEDs to MCSPI2_SOMI and MCSPI2_SIMO to act as status indicators during board bring-up.
6. Test Points: Place test points for all power supplies and reset signals going into the OMAP35x Torpedo SOM. Label them with descriptive names on the silkscreen.
7. R-packs: Avoid use of R-packs on the first pass of a custom baseboard. Using discrete resistors will allow for easy rework.

2.10 I/O Interface

Verify that any signal driven from the OMAP35x Torpedo SOM has no more than one load. A buffer must be used if driving more than one load from the OMAP35x Torpedo SOM in your design.

2.11 USB OTG VBUS

A 4.7 uF capacitor must connect J2.11 and J2.13 (USB1_VBUS) to ground.

USB1_VBUS is driven by the TPS65950 and can only supply 100 mA of current on VBUS. If more than 100 mA is required, it is possible to design an external VBUS supply to coexist with the USB1_VBUS signal. When using an external VBUS supply, the OTG_CTRL[DRVVBUS] signal in the TPS65950 must be cleared at all times. The USB1_VBUS signal must also be tied to the output of the external VBUS supply to allow for detection of the TPS65950 VBUS.

2.12 SD/MMC Card Detect

Connect J2.54 (SD1_DATA5) to ground if it is not being used for MMC card detect.

2.13 Real-Time Clock Battery Backup

If your design uses a rechargeable battery to back up the real-time clock (RTC) on the TPS65950, do not place any capacitors on the BACKUP_BATT rail. Doing so will prevent the TPS65950 from charging the backup battery.

Verify the rechargeable backup battery targeted for your design can be adequately charged by the OMAP35x Torpedo SOM PMIC. The PMIC provides a constant current that can be set at 25 uA, 150 uA, 500 uA, or 1 mA. The available cutoff voltages for the backup battery are 2.5V, 3.0V, 3.1V or 3.2V. Inadequate charging could prevent the backup battery from being fully charged.

If your design uses a non-rechargeable battery, place a diode on BACKUP_BATT to prevent accidental charging of the battery.

Current consumption on BACKUP_BATT has been measured as high as 50 uA but is typically 10 uA. Choose a battery, rechargeable or not, that can supply sufficient power for the entire length of time required by your usage model. For example, if your usage model leaves MAIN_BATT disconnected for a total of six months over a product life cycle, a backup battery of at least 216 mAh is required, such as a CR2032.

Please refer to the *AN 416 OMAP35x Torpedo SOM Power Management* for details on connections.

2.14 McBSP

The OMAP35x Torpedo SOM can support up to four McBSP ports (McBSP2 – McBSP5). Of the four McBSP ports, two are connected to the TPS65950 (McBSP2 and McBSP3).

McBSP2 is connected to the TPS65950 audio interface. To use McBSP2 externally, the AUDIO_IF[AIF_TRI_EN] bit must be set to program the audio interface on the TPS65950 for high impedance.

McBSP3 is connected to the TPS65950 PCM interface. To use McBSP3 externally, the VOICE_IF[VIF_TRI_EN] bit must be set to program the audio interface on the TPS65950 for high impedance.

2.15 UARTs

When using high-speed or continuous data transmission, consider implementing hardware flow control to guarantee correct delivery of data. Transitioning in and out of low power modes or high processor utilization may cause first in, first out (FIFO) errors.

2.16 Audio

The OMAP35x Torpedo SOM does not have onboard muting capability. External FETs must be added to CODEC_OUTL and CODEC_OUTR to provide muting capability. Use N-channel FETs and follow the design on the Torpedo Launcher Baseboard, using J1.88/CONFIG3 (default MCSPI3_CLK) to turn on the FETs.

2.17 Ethernet

If you plan to use the SMSC Ethernet chip on the Torpedo Launcher Baseboard, SMSC recommends adding 15 pF 50V capacitors to ground on all four TPx signals to minimize EMI. Place these caps as close as possible to the magnetics.

When directly connecting the Ethernet port to another Ethernet device, such as a hub, magnetics are not required. Proper differential signaling layout rules must still be followed; contact SMSC for the proper passives configuration.

NOTE: Always put down a serial EEPROM to hold the MAC address. Contact IEEE to obtain MAC addresses.

2.18 Reduce Boot Time

Customers looking to boot from NAND can reduce boot time by over one second simply by changing the boot order. The current boot order positions NAND as the last boot device. To change NAND to the first boot device, pull down SYS_BOOT5 during power up. This may be done through Logic PD's New Product Introduction (NPI) process or on the customer baseboard. This boot-time savings is in addition to what is offered by Logic PD's Zip™[6] technology. Contact Logic PD for assistance in further reducing boot time.

3 Layout Checklist

Items listed in this section must be reviewed by the layout designers prior to releasing the Gerber design files for board production.

3.1 USB

Verify that the following USB differential pairs have an impedance match of 90 ohms:

- USB1_D+/USB1_D-

3.2 Decoupling Caps

Decoupling caps must be placed as close as possible to the targeted component.

3.3 Probe points

1. Provide probe points for critical signals that do not have resistors or capacitors.
2. Provide access to ground near high-speed signals and at points across the board.

[6] http://www.logicpd.com/products/software/zip/

3.4 Silkscreen

1. Logic PD recommends that the silkscreen display dots for every ten J1/J2 connector edge pins (e.g., 10, 20, 30, … 100).
2. Review all silkscreen markings to make sure nothing is covered due to vias or part placement.
3. Place tables of all possible jumper configurations on the silkscreen.
4. Label probe points for power and ground with the voltage.
5. Mark the baseboard silkscreen to show proper positioning of the OMAP35x Torpedo SOM; this can be done by providing an outline of the SOM and showing the two notched corners. Additionally, include an outline of the CPU and debug connectors to assist with proper insertion.

3.5 OMAP35x Torpedo SOM Placement

1. Verify sufficient baseboard space exists (height, width, and length) for the OMAP35x Torpedo SOM per the recommended baseboard footprint in the *OMAP35x Torpedo SOM Hardware Specification*[7].
2. If planning to use a hold-down, verify that holes on the baseboard are present per the recommended baseboard footprint in the *WP 419 Torpedo SOM Mechanical Hold-Down Scenarios*.[8]

4 Software Checklist

Items listed in this section must be reviewed by the software engineer prior to releasing software for testing.

1. Pull-ups/downs: Verify that software configures all signals that are not pull-ups, pull-downs, or present in hardware. A common oversight is to not use software to configure the pull-ups for nIRQx signals since they are not controlled by hardware.
2. Power Management: Verify the targeted BSP has the required power management support to meet your system requirements.
3. If your LCD has power sequencing requirements, ensure these are completed correctly.
4. If using a non-rechargeable RTC backup battery or an always-on power source, disable charging the backup battery in the BSP.
5. If using a rechargeable RTC backup battery, make sure charging is enabled in the BSP and that the voltage is set appropriately using TI's *TPS65950 Technical Reference Manual (TRM)*.[9] See the *OMAP35x Torpedo SOM Power Management Application Note* for details.
6. If using GPIO_99 or GPIO_100, make sure VAUX4 is enabled.

[7] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=971
[8] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=984
[9] http://www.ti.com/product/tps65950

5 Board Bring-Up Checklist

Items listed in this section can aid in system bring-up. Check the items in the order provided below. If you experience problems with booting, proceed through Section 5.1 to troubleshoot this issue.

1. Know your boot sequence. The default for the OMAP35x Torpedo SOM is USB, UART3, MMC1, NAND. See the *OMAP35x Torpedo SOM Schematics* for available boot sequences.
2. Verify that LogicLoader boots to the losh> prompt using the Zoom™ OMAP35x Torpedo Development Kit. If it does not, continue checking through the steps below.
   a. Power: Verify adequate power is applied to MAIN_BATTERY.
   b. Reset In: Verify the MST_nRST (J1.227) signal goes high.
   c. Reset Out: Verify the SYS_nRESWARM (J1.227) signal goes high.
   d. Verify uP_UARTB_TX (J2.43) toggles since the internal boot ROM will attempt to boot from UART3 before SD or NAND.
   e. GPIO: Verify that MCSPI2_SOMI (J1.56) and MCSPI2_SIMO (J1.65) toggle opposite of each other, as this indicates that the LogicLoader idle thread is running.
   f. UARTA: Verify that serial output from the debug serial port shows the LogicLoader losh> prompt (the serial port must be set at: baud rate: **115200**; data: **8-bit**; parity: **none**; stop: **1-bit**; flow control: **none**).

5.1 Bootloader Does Not Boot

If the bootloader does not boot successfully and everything through Step 2d above is working correctly, the boot ROM internal to the OMAP35x processor is failing to access your bootloader due to other problems.

By default, the OMAP35x Torpedo SOM signals the internal boot ROM to boot USB, UART, MMC1, and then NAND using the SYS_BOOT signals. This default configuration can be changed by populating R44 (SYS_BOOT3) or by changing the default state at reset of SYS_BOOT0 or SYS_BOOT5 on the baseboard. Changes to the SYS_BOOT sequence could also prevent the bootloader from running.

If all SYS_BOOT signals are connected as expected and the bootloader still does not boot, check for possible problems with the signals listed in the sections below.

5.1.1 SOM Does Not Boot from SD Card

Verify that SD1_CLK is toggling. This is an indication that the internal boot ROM is trying to access the SD card.

Verify your SD card is configured correctly and check to see that it boots in your OMAP35x Torpedo Development Kit. If not, see information provided in Logic PD's FAQ: Why doesn't my OMAP3-based Development Kit boot from the SD Card?[10]

The default boot order positions SD before NAND. In order for the processor to boot successfully, no shorts can exist for the connections associated with the signals listed in Table 5.1.

[10] http://www.logicpd.com/faqs/answer/why-doesnt-my-omap3-based-development-kit-boot-from-the-sd-card/

Table 5.1: MMC/SD Signals

SOM SD Signal	uP Signal	SOM Pin
VREF_SD1/MMC	VMMC1	J1.3
SD1_CLK	MMC1_CLK	J2.32
SD1_CMD	MMC1_CMD	J2.42
SD1_DATA0	MMC1_DAT0	J2.48
SD1_DATA1	MMC1_DAT1	J2.46
SD1_DATA2	MMC1_DAT2	J2.44
SD1_DATA3	MMC1_DAT3	J2.50
SD1_DATA5	GPIO_127	J2.54

5.1.2 SOM Boots from SD Card but Not NAND Flash

Table 5.2 provides a complete list of signals used to access the NAND flash on the OMAP35x Torpedo SOM; some signals are not accessible through the SOM connectors. If any of the signals in this table have a short, the bootloader will not boot. Verify all signals are clear of shorts to successfully boot your system.

Table 5.2: NAND Signals

NAND Signal	uP Top Ball	uP Bottom Ball	uP Signal	SOM Signal	SOM Pin
I/O0	M2	K1	gpmc_d0	uP_D0	J1.35
I/O1	M1	L1	gpmc_d1	uP_D1	J1.37
I/O2	N2	L2	gpmc_d2	uP_D2	J1.33
I/O3	N1	P2	gpmc_d3	uP_D3	J1.39
I/O4	R2	T1	gpmc_d4	uP_D4	J1.49
I/O5	R1	V1	gpmc_d5	uP_D5	J1.57
I/O6	T2	V2	gpmc_d6	uP_D6	J1.53
I/O7	T1	W2	gpmc_d7	uP_D7	J1.55
I/O8	AB3	H2	gpmc_d8	uP_D8	J1.29
I/O9	AC3	K2	gpmc_d9	uP_D9	J1.31
I/O10	AB4	P1	gpmc_d10	uP_D10	J1.43
I/O11	AC4	R1	gpmc_d11	uP_D11	J1.45
I/O12	AB6	R2	gpmc_d12	uP_D12	J1.41
I/O13	AC6	T2	gpmc_d13	uP_D13	J1.47
I/O14	AB7	W1	gpmc_d14	uP_D14	J1.59
I/O15	AC7	Y1	gpmc_d15	uP_D15	J1.63
WE#	V1	F4	gpmc_nwe	uP_nWE	J1.1
RE#	V2	G2	gpmc_noe	uP_nOE	J1.15
ALE	W1	F3	gpmc_nadv_ale	uP_nADV_ALE	J1.23
CE0#	Y2	G4	gpmc_ncs0	uP_nCS0	J1.9
LOCK	AB9	AG15	Feed Through Pins	DGND	DGND
WP#	AB10	H1	gpmc_nwp	No connection	No connection
R/B#	AB12	M8	gpmc_wait0	Pulled up 1.8V	J1.26
CLE	AC12	G3	gpmc_nbe0_cle	uP_nBE0	J1.25
VCC	U1	A15	Feed Through Pins	VIO_1V8	J2.4, J2.7

6 TI Schematic Checklists

Additional schematic checklist information for the OMAP35x processor and TPS65950 PMIC can be found in the *TPS65950 Schematic Checklist*[11] or on TI's *OMAP35x Schematic Checklist* wiki page.[12] Although information provided in the TI checklist may not apply specifically to Logic PD hardware, it can be used as a reference. If there are any conflicts between the TI wiki checklist and this Logic PD design checklist, please contact Logic PD.

7 Summary

This application note is provided as a guide to use during development and bring-up of your platform. The ideas provided within this document may help reduce debug time and limit or eliminate future re-spins of your embedded system. Information provided in the *OMAP35x Torpedo SOM Hardware Specification* or any specification document for onboard components takes precedence over the information within this application note.

[11] http://www.ti.com/product/tps65950
[12] http://processors.wiki.ti.com/index.php/OMAP35x_Schematic_Checklist