AM1808 SOM-M1 Design Checklist

Application Note 477

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Abstract

This application note provides a list of items to verify when designing the AM1808 SOM-M1 into an embedded system. Reviewing this checklist prior to releasing design files and software for production can help reduce the probability of future board spins.

Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	SK	Initial release	JCA	04/01/11
B	SMC, JCA	-Section 3.4: Added instruction for baseboard connector layout; -Section 4: Added item about touch interface	JCA, NJK	05/04/11
C	SO	-Section 2.4: Added list number 4 stating that the RTC power rail should always be powered; added list number 5 regarding VRTC_IN power supplies; -Section 2.5: Added list number 2 about how the TRS3386 RS-232 transceiver is no longer qualified to work at 1.8V; -Section 2.12: Changed signal name in list number 1 to reflect signal on SOM, rather than signal on baseboard; corrected signal in list number 2 from J1.75 to J1.71; changed signal name in list number 2 to reflect signal on SOM, rather than signal on baseboard	BSP	10/31/12
D	SO	-Throughout: Updated template; updated links for new support site; -Table 2.1: Corrected SOM-M1 signal names to contain underscores rather than hyphens; -Section 2.13: Fixed broken link to SMSC's AN 8.13	SWE	10/10/13

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1 Introduction

When using the AM1808 SOM-M1 in an embedded system, reviewing some specifics during the design phases can minimize or even eliminate future board spins. Information provided in this application note should be reviewed prior to releasing a design for fabrication and assembly. It is also critical that software teams review the “Software Checklist” and “Board Bring-Up Checklist” sections to ensure a trouble-free first board boot.

2 Schematic Checklist

Items in this section should be reviewed by the system designer prior to releasing the design for layout.

2.1 ADC

The touch sensors on the TPS65070 Power Management IC (PMIC) can be used as Analog-to-digital converter (ADC) signals. Input voltages to these pins should not exceed 2.25V per the TPS65070 specification. A list of pin specifications can be found in Table 2.1 below.

Table 2.1: ADC Signals

ADC Signal	SOM-M1 Signal Name	SOM-M1 Pin	Resolution	Maximum Voltage Input
TSX1 (AD_IN1)	TOUCH_X1	J1.68	10 bit	2.25V
TSX2 (AD_IN2)	TOUCH_X2	J1.70	10 bit	2.25V
TSY1 (AD_IN3)	TOUCH_Y1	J1.72	10 bit	2.25V
TSY2 (AD_IN4)	TOUCH_Y2	J1.74	10 bit	2.25V

2.2 Clocks

Verify that series termination is available for all clock signals that do not have internal drive strength control.

2.3 Reset

1. There is an internal pull-up resistor contained in the uP_RESETn signal; therefore, pull-up resistors or active drivers are not required to drive the uP_RESETn signal.
2. Logic PD suggests placing a 0.1uF capacitor near the reset pin; this can help reduce ESD-induced resets.

2.4 Power

1. Verify all power and ground signals are connected correctly and at the correct voltage level.
2. Pin J1.37 selects between 3.3V or 1.8V supply—if left floating, a 3.3V supply is implied.
3. Verify the regulators provide sufficient current demands.
4. Ensure the real-time clock (RTC) rail (VRTC_IN) is always powered.
5. Expected current draw on VRTC_IN can be up to 55 uA due to quiescent current on the TPS79912 LDO. Use an RTC battery large enough to guarantee functionality for your required time.

2.5 Level Shifters

1. Verify that all pins are connected at the correct voltage levels. Many of the pins on the AM1808 SOM-M1 can be operated at both 3.3V and 1.8V.
2. The TRS3386 RS-232 transceiver is no longer qualified to work at 1.8V. The TRS3253 is an alternative device that does support 1.8V operation.
3. Verify the correct reference voltage from the AM1808 SOM-M1 is used for signal level shifting or pull-ups.
4. Verify that the reference voltage is not used as a power source.
5. Verify that the direction signal has the proper direction control.
6. Verify that unused level shifter input signals are tied per the level shifter specification and are not left floating.
7. For interface signals that have different directions (e.g., RX and TX), verify that the level shifters also have different direction signals.

2.6 Peripheral Interfaces

Verify peripheral interface connections are equivalent to those on the Zoom AM1808 EVM or eXperimenter Kit baseboard, such as USB, serial, and SD/MMC.

2.7 GPIO

1. Verify the signal selected to be a GPIO is actually available as an alternative function or is a dedicated GPIO, GPI, or GPO function needed for the design.
2. Verify that no contention occurs on GPIO signals during reset and low-power mode states.
3. Verify that signals designated as GPIO have reset states with the desired direction and level.
4. If using boot pins as a GPIO, verify that the boot pins are at the proper levels when a reset occurs. The device will not boot correctly if the correct values are not latched in on reset.

2.8 LCD

The recommended LCD interface is to support 16-bit (5:6:5) color. Contact Logic PD[1] about supporting other color depths.

2.9 Debug

1. Serial: Logic PD recommends all designs have a debug serial port. This port is used for terminal access to Linux. UART2 is the designated debug port signal used on the AM1808 SOM-M1.
2. JTAG: The JTAG interface and voltage required for your tools may be different than those used on the AM1808 SOM-M1. Verify that the JTAG connector interface for your design will interface to the emulator that is planned for software development.
3. Ethernet: Logic PD recommends putting down a WLAN Ethernet port on the first phase of baseboards; this port can be used for development and download purposes.
4. Reset: Logic PD recommends designing-in a debounced reset button to the AM1808 SOM-M1 to aid in debug.

[1] http://support.logicpd.com/TechnicalSupport/AskAQuestion.aspx

2.10 I/O Interface

Verify that any signal driven from the AM1808 SOM-M1 has no more than one load. A buffer must be used if driving more than one load from the AM1808 SOM-M1 in your design.

2.11 USB Interface

Unused signals should be connected as shown in Table 2.2below.

Table 2.2: Unused USB Signals

Signal Name	SOM-M1 Signal Name	SOM-M1 Pin	Configuration (when USB0 and USB1 are not used)	Configuration (when USB1 is not used)
USB0_DM	uP_USB0_DM	J1.82	No Connect	USB0 function
USB0_DP	uP_USB0_DP	J1.84	No Connect	USB0 function
USB0_ID	uP_USB0_ID	J1.86	No Connect	USB0 function
USB0_VBUS	USB_VBUS	J1.87, J1.88	No Connect	USB0 function
USB0_DRVVBUS	uP_USB0_DRVVBUS	J1.25	No Connect	USB0 function
USB0_VDDA33	—	—	No Connect	3.3V
USB0_VDDA18	—	—	No Connect	1.8V
USB0_VDDA12	—	—	No Connect	External filter cap
USB1_DM	uP_USB1_DM	J1.81	No Connect	VSS
USB1_DP	uP_USB1_DP	J1.83	No Connect	VSS
USB1_VDDA33	—	—	No Connect	No Connect
USB1_VDDA18	—	—	No Connect	No Connect
USB_REFCLKIN	uP_UART1_CTSn	J1.89	No Connect or other peripheral	USB0 function or other peripheral
USB_CVDD	—	—	1.2V	1.2V

2.12 Secure Digital/MicroSD

1. When Secure Digital (SD) or MicroSD cards are used in a system design, signal J1.73 (uP_EMIFA_A16) is used as a card detect signal.
2. Signal J1.71 (uP_EMIFA_A17) is also used as a write protect signal.

2.13 Ethernet Magnetics

1. The Ethernet controller on the AM1808 SOM-M1 is an SMSC LAN8710 component. SMSC provides *AN 8.13*[2] that lists suggested magnetic for use with their SMSC LANxxxx components.
2. When connecting the magnetic to the SMSC LAN8710 on the AM1808 SOM-M1, the following connections must be followed to match the SMSC LAN8710 reference design:
   - □ Separate the transmit and receive center taps.
   - □ Tie a 10 ohm (1/8W 1%) resistor between 3.3V and the center tap signals of the magnetic.

[2] http://www.microchip.com/wwwproducts/Devices.aspx?product=LAN8710A#documentation

3 Layout Checklist

Items listed in this section should be reviewed by the layout designers prior to releasing the Gerber design files for board production.

3.1 USB

Verify that the USB differential pairs listed below have an impedance match of 90 ohms:

- uP_USB0_DP/uP_USB0_DP
- uP_USB1_DP/uP_USB1_DP

3.2 Ethernet

Verify that the Ethernet differential signals listed below have an impedance match of 100 ohms:

- ETHER_TX+/ETHER_TX-
- ETHER_RX+/ETHER_RX-

3.3 Decoupling Caps

Decoupling caps must be placed as close as possible to the targeted component.

3.4 Baseboard Connectors & Silkscreen

1. Verify that baseboard connectors are positioned in the correct order where J1 and J2 are the outside connectors. The silkscreen should display pins 1, 2, 99, and 100 for each connector to show their orientation on the board. See Figure 3.1 below.

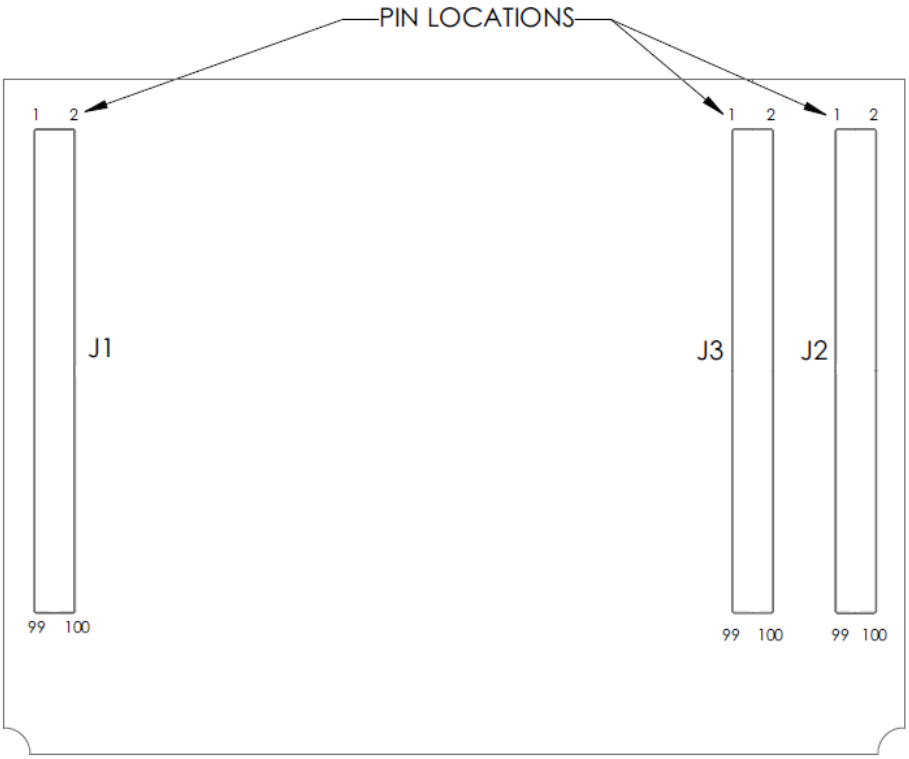

Figure 3.1: Recommended Baseboard Footprint

2. Logic PD recommends that the silkscreen display dots for every ten J1/J2/J3 connector edge pins (e.g., 10, 20, 30, …100).
3. Review all silkscreen markings to make sure nothing is covered due to vias or part placement.

3.5 SOM-M1 Placement

1. Verify sufficient baseboard space exists (height, width, and length) for the AM1808 SOM-M1 per the recommended baseboard footprint in Appendix A of the *AM1808 SOM-M1 Hardware Specification*.[3]
2. If planning to use the Logic PD hold down clips, verify that holes on the baseboard are present per the recommended baseboard footprint in Appendix B of the *AM1808 SOM-M1 Hardware Specification.*

4 Software Checklist

Items listed in this section should be reviewed by the software engineer prior to releasing software for testing.

1. Pull-ups/downs: Verify that software configures all signals that are not pull-ups, pull-downs, or present in hardware.
2. Power management: Verify the targeted BSP has the required power management support to meet your system requirements.
3. Touch interface: If your design runs off battery, verify that software enables VREF. An issue internal to the Texas Instruments (TI) TPS65070 PMIC keeps the ADC from automatically enabling VREF.

5 Board Bring-Up Checklist

Items listed in this section can aid in system bring-up. Check the items in the order provided below.

1. Power: Verify adequate power is applied to MAIN_BATT_IN.
2. Reset: Verify the uP_RESETn signal goes high.
3. UART2: Verify that the serial output from the debug serial powers is operational (the serial port must be set at: baud rate: 115200; data: 8-bit; parity: none; stop: 1-bit; flow controls: none).

6 TI AM1808 Processor Schematic Checklist

Additional AM1808 processor schematic checklist information can be found on TI's *OMAP-L13x/C674x/AM1x Schematic Review Checklist* wiki page[4]. Though information provided in the TI checklist may not apply specifically to Logic PD hardware, it can be used as a reference. If there are any conflicts between the TI wiki checklist and this Logic PD design checklist, please contact Logic PD.

[3] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=786
[4] http://processors.wiki.ti.com/index.php/OMAP-L13x_/_C674x_/_AM1x_Schematic_Review_Checklist

7 Summary

This application note is provided as a guide to use during development and bring-up of your platform. The ideas provided within this document may help reduce debug time and limit or eliminate future re-spins of your embedded system. Information provided in the *AM1808 SOM-M1 Hardware Specification* or any specification document for onboard components takes precedence over the information within this application note.