OLED Display Integration with OMAP35x Development Kits

Application Note 462

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Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	RAH	-Initial release	BSB	04/07/11
B	HJS	-Throughout: Updated template; updated links for new support site; -Added Section 1.1	SO	09/19/13

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Table of Contents

1 Introduction 1
1.1 Nomenclature 1
2 Background 1
2.1 Zoom OMAP35x Development Kit Baseboard and LCD Interface 1
2.2 Display Type 1
2.3 Display Signals 1
2.4 Reference Datasheets 3
3 Integrating CMEL Display with LogicLoader 4
3.1 Power-on Sequence 4
3.2 Set Up SPI Port on OMAP35x Development Kit 5
3.2.1 Configure McSPI3 5
3.2.2 Configure Port to Transmit and Receive Data 5
3.2.3 Configure OLED Display to Communicate Over SPI 6
3.2.4 Configure LCD Controller 7
3.2.5 OLED Display Setup LogicLoader Script 8
4 Debug Tips 10
4.1 Power-up Requirements and Timing 10
4.2 SPI Data 10
4.3 OLED Device Code Read 10
4.4 SPI Writes to GRAM 10
4.5 Lessons Learned 10
5 Summary 10
Appendix A: Schematics for the OLED Display Adaptor Board 11

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1 Introduction

This application note guides users through the necessary steps to interface an Organic Light Emitting Diode (OLED) display to Logic PD's Zoom™ Development Kit baseboards. Since each LCD, System on Module (SOM) LCD controller, and software configuration is unique, it is beyond the scope of this document to provide details for every conceivable scenario. Therefore, the intention of this document is to point users in the right direction so that they may confidently approach their particular situation.

1.1 Nomenclature

- This document covers the OMAP35x SOM-LV and OMAP35x Torpedo SOM. Use of "OMAP35x SOM" suggests text that applies to both platforms; information specific to one platform will call out the precise name.
- Use of "Zoom OMAP35x Development Kit" suggests text that applies to both the OMAP35x SOM-LV Development Kit and OMAP35x Torpedo Development Kit; information specific to one development kit will call out the precise name.

2 Background

2.1 Zoom OMAP35x Development Kit Baseboard and LCD Interface

The Zoom OMAP35x Development Kit baseboards have a 60-pin 0.100" header (Tyco 1-761606-6) located at reference designator J11 that connects LCD signals directly from the OMAP 35x SOM LCD controller. Depending on your specific display, only a few of the LCD signals may be needed.

2.2 Display Type

For this application note, Logic PD has interfaced a 2.4" Active-Matrix OLED display from CMEL (C0240QGLA-T) that uses a Samsung S6E63D6 driver IC.

- Driving Mode: Active Matrix
- Color Mode: Full color (65K color) for 16-bit mode
- Drive IC: S6E63D6, COG Assembly
- Interface: FGB 16-bit bus interface (DOTCLK, VSYNC, HSYNC, DE, DB17-0)
- SPI: (SCL, SDIN, SDOUT, CBS)

2.3 Display Signals

The display signals provided by the OMAP35x SOM are adequate for any OLED display. Table 2.1 below provides an example of the connections used for this OLED display type. Because the baseboard LCD connector does not have a serial peripheral interface (SPI) port, the SPI signals used to configure the panel are routed to test points and jumpered to the baseboard expansion connector.

NOTE: This scenario represents the OMAP35x SOM-LV Development Kit. The OMAP35x Torpedo Development Kit scenario is similar; however, a different SPI port must be used.

Table 2.1: OLED Display Signals

OLED Display Pin	OLED Display Signal	Connection on OLED Display Board	Description
1	AR_VDD	AR_VDD_4.6	Positive voltage for OLED

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OLED Display Pin	OLED Display Signal	Connection on OLED Display Board	Description
2	AR_VSS	AR_VSS_-4.4	Negative voltage for OLED
3	VCI	3.3V_LCD	Power supply for analog circuit
4	VCI1	VCI1OUT	A reference voltage for first booster
5	GND	GND	Ground
6	C12M	C12M	External capacitance connect pin between C12M and C12P
7	C12P	C12P	—
8	C11P	C11P	External capacitance connect pin between C11M and C1P
9	C11M	C11M	—
10	VLOUT1	VLOUT1	First booster output pin
11	C31P	C31P	External capacitance connect pin between C31M and C31P
12	C31M	C31M	—
13	C32P	C32P	External capacitance connect pin between C32M and C32P
14	C32M	C32M	—
15	VLOUT3	VLOUT3	Third booster output pin
16	VLOUT2	VLOUT2	Second booster output pin
17	C21P	C21P	External capacitance connect pin between C21M and C21P
18	C21M	C21M	—
19	GND	GND	Ground
20	VGS	3.3V_LCD	A reference level for the grayscale voltage generation circuit
21	SPB	SPB	Select the CPU interface mode
22	ID_MIB	ID_MIB	Select the CPU type
23	DB17	S_R_LCD_R5	16-bit interface : DB 17-10, DB 8-1
24	DB16	S_R_LCD_R4	—
25	DB15	S_R_LCD_R3	—
26	DB14	S_R_LCD_R2	—
27	DB13	S_R_LCD_R1	—
28	DB12	S_R_LCD_R0_B	—
29	DB11	S_R_LCD_G5	—
30	DB10	S_R_LCD_G4	—
31	DB9	S_R_LCD_G3	—
32	DB8	S_R_LCD_G2	—
33	DB7	S_R_LCD_G1	—
34	DB6	S_R_LCD_G0	—
35	DB5	S_R_LCD_B5	—
36	DB4	S_R_LCD_B4	—

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OLED Display Pin	OLED Display Signal	Connection on OLED Display Board	Description
37	DB3	S_R_LCD_B3	—
38	DB2	S_R_LCD_B2	—
39	DB1	S_R_LCD_B1	—
40	DB0	S_R_LCD_B0_B	—
41	VSYNC	S_R_LCD_VSYNC	Frame-synchronizing signal
42	HSYNC	S_R_LCD_HSYNC	Line-synchronizing signal
43	DOT_CLK	S_R_LCD_DCLK	Input pin for clock signal of external interface: dot clock
44	ENABLE	LCD_MDISP	Data enable signal pin for RGB interface
45	SDI	TP1	For SPI input data
46	SDO	TP2	For SPI output data
47	CSB	TP3	Chip select signal input pin
48	SCL	TP4	The synchronous clock signal
49	RS	RS	Register select pin
50	E_RDB	E_RDB	When SPI mode is selected, fix this pin at VDD3 level
51	RESETB	RESETB	Reset pin initializes the IC when low
52	MVDD	VDD	Internal power for RAM
53	VREG1OUT	VREG1OUT	A reference level for the grayscale voltage
54	VCI1OUT	VCI1OUT	Power supply for analog circuit
55	VGH	VGH	The positive voltage used in the gate driver
56	VGL	VGL	The negative voltage used in the gate driver
57	GND	GND	Ground
58	X-	OPEN	For touchscreen
59	Y-	OPEN	For touchscreen
60	X+	OPEN	For touchscreen
61	Y+	OPEN	For touchscreen

2.4 Reference Datasheets

NOTE: Logic PD is not responsible for the validity of the following links or the content of the following websites or datasheets.

- *CMEL C0240QGLA-T Datasheet* (This document is no longer available directly from Data Module's website; please contact Data Module.[1])
- *CMEL C0240QGL Series Integration Application Note* (This document is no longer available directly from Data Module's website; please contact Data Module.)
- *Samsung S6E63D6 Driver Chip Datasheet*[2]
- *Texas Instruments (TI) OMAP35x Technical Reference Manual (TRM)*[3]

[1] http://www.datamodul.com/us/home.html
[2] http://www.datasheetarchive.com/S6E63D6-datasheet.html

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3 Integrating CMEL Display with LogicLoader

The instructions in this section will work as expected if the following assumptions are met:

- LogicLoader 2.4.9 or later is running
- The display and all cables are connected correctly
- The display is properly powered
- The user knows how to write to a register inside an IC
- The user understands LCD controllers and LCD timing signals
- The user knows how to write to the SPI registers of the OMAP35x SOM

3.1 Power-on Sequence

The power supplies must meet the power-up sequencing requirements of the *CMEL C0240QGL Series Integration Application Note*; Figure 3.1 shows the correct power-on sequence. The signals that are most important are VCI (3.3V), ARVDD (4.6V), and ARVSS (-4.4V).

For more information on all the other signals, please refer to the OLED datasheet. Instructions for programming LogicLoader to control the power supply pins is not included in this application note.

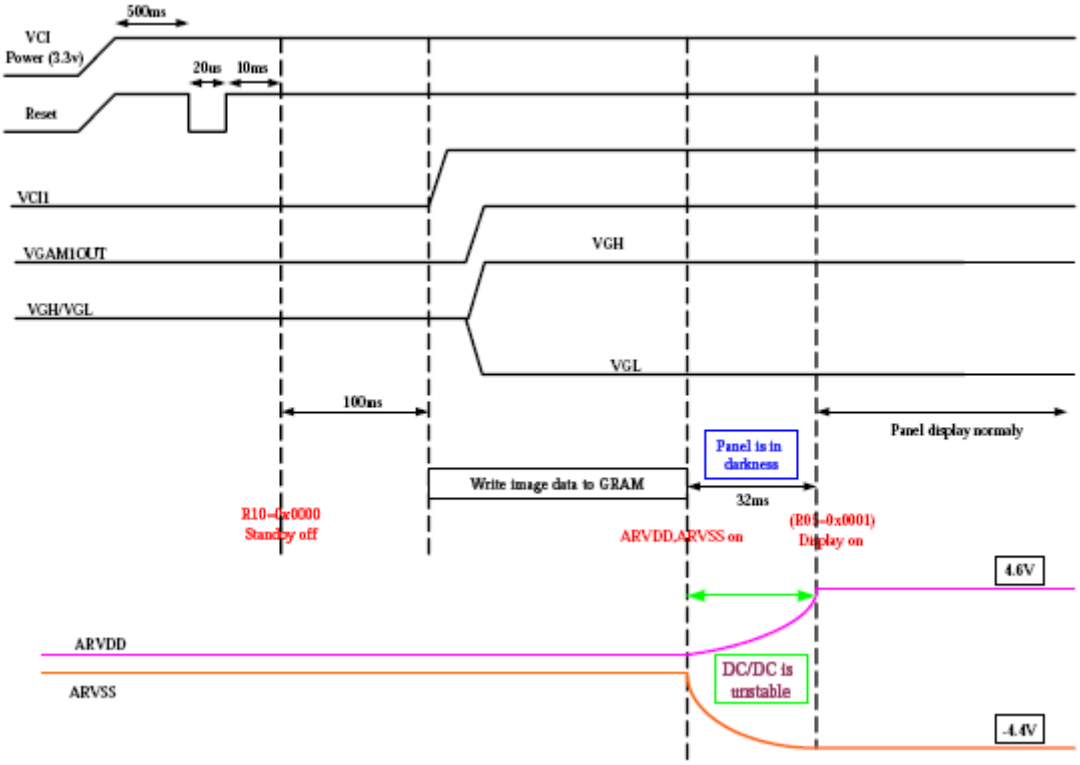

Figure 3.1: Power-on Sequence Timing Diagram

[3] http://www.ti.com/product/omap3530

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3.2 Set Up SPI Port on OMAP35x Development Kit

3.2.1 Configure McSPI3

We will configure McSPI3 for the SPI interface since it is available on the OMAP35x Development Kit and can be used with the breakout board.

NOTE: The breakout board is not available for the OMAP35x Torpedo Development Kit; Logic PD recommends using SPI2 on the OMAP35x Torpedo Development Kit.

Configure the following multiplexor control registers (CONTROL_PADCONF registers in the OMAP35x) to use McSPI3. All register addresses, values, and signal names are from TI's *OMAP35x TRM*.

Table 3.1: Control Registers Configured for McSPI3

Register Address	Value	Signal Name
0x4800_2158	0x0101	McSPI3_CLK
0x4800_215a	0x0101	McSPI3_SIMO
0x4800_215c	0x0101	McSPI3_SOMI
0x4800_2162	0x0101	McSPI3_CS0

Writing these registers in LogicLoader will look like this:

```
losh> w /h 0x48002158 0x0101 #Select McSPI3_CLK from pad config
losh> w /h 0x4800215a 0x0101 #Select McSPI3_SIMO from pad config
losh> w /h 0x4800215c 0x0101 #Select McSPI3_SOMI from pad config
losh> w /h 0x48002162 0x0101 #Select McSPI3_CS0 from pad config
```

3.2.2 Configure Port to Transmit and Receive Data

Now that the development kit is set up to use these GPIOs as a McSPI port, we must configure and initialize the port to transmit and receive data using the steps below.

1. Initiate a SPI module reset on the OMAP35x for McSPI3.
2. Read the status register for the SPI module to see that a reset was done.
3. Configure the McSPI3 channel.
4. Configure the channel to be in functional master mode.
5. Enable the channel.

Table 3.2 shows what register addresses and values are being accessed.

Table 3.2: McSPI Register Addresses and Values

Action	Register Address	Value	Signal Name
Reset module	0x480b_8010	0x0001	#MCSPI_SYSCONFIG
Read Status	0x480b_8014	(read)	#MCSPI_SYSSTATUS
Configure channel	0x480b_802c	0x00012bdc	#MCSPI_CHxCONF
Configure for master mode	0x480b_8028	0x0000	#MCSPI_MODULCTRL
Enable channel	0x480b_8034	0x0001	#MCSPI_CHxCTRL

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Writing these registers in LogicLoader will look like this:

```
losh> w /h 0x480b8010 0x0001    #MCSPI_SYSCONFIG
losh> x /h 0x480b8014        #MCSPI_SYSSTATUS
losh> w /w 0x480b802c 0x00012bdc  #MCSPI_CHxCONF
losh> w /h 0x480b8028 0x0000    #MCSPI_MODULCTRL
losh> w /h 0x480b8034 0x0001    #MCSPI_CHxCTRL
```

Testing and debugging the SPI port can be done by attaching the breakout board to the OMAP35x SOM-LV Development Kit and connecting the following signals on J4 to the respective OLED display board pin.

Table 3.3: Test and Debug Pins

J4 Pin	Signal Name	OLED Display Board Pin
1	SPI SCLK	TP4
3	SPI TX	TP2
5	SPI RX	TP1
7	SPI CS0	TP3

LogicLoader is now configured for the CPU to talk to the SPI port on the OMAP35x Development Kit.

3.2.3 Configure OLED Display to Communicate Over SPI

The next step is to configure the OLED display over the SPI port to send display data over the SPI port.

"Section 1.4" of the *CMEL C0240QGL Series Integration Application Note* shows the relationship of a host SPI interface to the OLED display along with the following initialization code to turn on the display. Index writes to the panel are prefixed with 0x74 and parameter writes are prefixed with 0x76 (as indicated in the OLED display data sheet). For our OLED display board, the ID pin is high. Details on the registers can be found in the *Samsung S6E63D6 Driver Chip Datasheet*.

Below is the initialization code from the *CMEL C0240QGL Series Integration Application Note.*

```
Index_out(0x10);
Parameter_out(0x0000);
Index_out(0x03);
Parameter_out(0x0130);
Index_out(0x05); // display on
Parameter_out(0x0001);
Index_out(0x22);
```

Below is an example of how the initialization code will look in LogicLoader.

```
losh> w /w 0x480b8038 0x740010;
losh> w /w 0x480b8038 0x760000;
losh> w /w 0x480b8038 0x740003;
losh> w /w 0x480b8038 0x760130;
losh> w /w 0x480b8038 0x740005;
```

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```
losh> w /w 0x480b8038 0x760001;
losh> w /w 0x480b8038 0x740022;
```

3.2.4 Configure LCD Controller

After establishing communication with the OLED display, the next step is to configure the OMAP35x LCD controller in LogicLoader.

Using Logic PD's *AN 298 Integrating Custom Displays with LogicLoader*,[4] TI's *OMAP35x TRM*, and timing diagrams from CMEL's *C0240QGLA-T Datasheet* and *C0240QGL Series Integration Application Note*, the following registers were calculated:

Table 3.4: LCD Registers

LCD signal name	Register	Value
DISPC_CONTROL	0x48050440	0x00018129
DISPC_SIZE_LCD	0x4805047C	0x013F00EF
DISPC_GFX_SIZE	0x4805048C	0x013F00EF
DISPC_TIMING_H	0x48050464	0x01901F1F
DISPC_TIMING_V	0x48050468	0x00700303
DISPC_DIVISOR	0x48050470	0x00010010
DISPC_CONFIG	0x48050444	0x00000000
DISPC_POL_FREQ	0x4805046C	0x00007000
CM_CLKSEL_DSS	0x48004E40	0x00010008

Before entering the values in LogicLoader, the display hardware must be initialized with default values.

```
losh> video-init 5 16
```

Now the customized values for the CMEL display can be entered as shown below.

```
losh> w /w 0x48050440 0x00018129
losh> w /w 0x4805047C 0x013F00EF
losh> w /w 0x4805048C 0x013F00EF
losh> w /w 0x48050464 0x01901F1F
losh> w /w 0x48050468 0x00700303
losh> w /w 0x48050470 0x00010010
losh> w /w 0x48050444 0x00000000
losh> w /w 0x4805046C 0x00007000
losh> w /w 0x48004E40 0x00010008
```

[4] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1495

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These register values can then be saved in the *video config* space. **NOTE:** For details on the configuration space, please refer to LogicLoader documentation for your product on the Logic PD support site.[5]

```
losh> config V test 320 240
```

Now the SPI port must tell the OLED LCD display to enable the RGB interface. "Section 1.4" of the CMEL's *C0240QGL Series Integration Application Note* shows the relationship of the host SPI interface, OLED display, and RGB 16-bit data, along with the initialization code.

The initialization code below enables RGB mode.

```
Index_out(0x02);
Parameter_out(0x0192);
Index_out(0x03);
Parameter_out(0x0130);
Index_out(0x10);
Parameter_out(0x0000);
Index_out(0x05); // display on
Parameter_out(0x0001);
Index_out(0x22);
```

Below is an example of the LogicLoader commands to initialize the RGB interface in 16-bit 65K color mode.

```
losh> w /w 0x480b8038 0x740002
losh> w /w 0x480b8038 0x760192
losh> w /w 0x480b8038 0x740003
losh> w /w 0x480b8038 0x760130
losh> w /w 0x480b8038 0x740010
losh> w /w 0x480b8038 0x760000
losh> w /w 0x480b8038 0x740005
losh> w /w 0x480b8038 0x760001
losh> w /w 0x480b8038 0x740022
```

All of these commands can now be saved as a single LogicLoader script (the OMAP35x LCD controller initialization is already saved in the *config* space).

3.2.5 OLED Display Setup LogicLoader Script

The text below can be saved as a LogicLoader *autoexec.losh* script to automatically set up the OLED display board.

```
#Initialize SPI pinmux registers
w /h 0x48002158 0x0101 #Select McSPI3_CLK from pad config
w /h 0x4800215a 0x0101 #Select McSPI3_SIMO from pad config
w /h 0x4800215c 0x0101 #Select McSPI3_SOMI from pad config
w /h 0x48002162 0x0101 #Select McSPI3_CS0 from pad config

#Setup SPI port
```

[5] http://support.logicpd.com/Home.aspx

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```
w /h 0x480b8010 0x0001       #MCSPI_SYSCONFIG
x /h 0x480b8014              #MCSPI_SYSSTATUS
w /w 0x480b802c 0x00012bdc   #MCSPI_CHxCONF
w /h 0x480b8028 0x0000       #MCSPI_MODULCTRL
w /h 0x480b8034 0x0001       #MCSPI_CHxCTRL

#Setup SPI on OLED display
w /w 0x480b8038 0x740010;
w /w 0x480b8038 0x760000;
w /w 0x480b8038 0x740003;
w /w 0x480b8038 0x760130;
w /w 0x480b8038 0x740005;
w /w 0x480b8038 0x760001;
w /w 0x480b8038 0x740022;

#Turn on LCD controller
video-open test 16;  #test video config must already be saved

#Setup SPI for RGB interface
w /w 0x480b8038 0x740002;
w /w 0x480b8038 0x760192;
w /w 0x480b8038 0x740003;
w /w 0x480b8038 0x760130;

w /w 0x480b8038 0x740010;
w /w 0x480b8038 0x760000;
w /w 0x480b8038 0x740005;
w /w 0x480b8038 0x760001;
w /w 0x480b8038 0x740022;

draw-test
```

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4 Debug Tips

These debug tips detail our findings during the integration of the CMEL OLED display with the OMAP35x Development Kit.

4.1 Power-up Requirements and Timing

OLED displays are much more demanding on their power-up requirements and timing than a typical TFT display. Failure to meet those timings may result in the OLED power supply circuit shutting down, the OLED failing to display data, or causing damage to the OLED display. Make sure any power supplies provided to the OLED display are configurable by a GPIO on the processor so that proper supply sequencing can be guaranteed.

This same requirement also applies to the OLED reset signal. Tie this signal to a GPIO pin on the processor so that it can be sequenced correctly during power up. Once proper operation has been confirmed, the reset signal can be attached to the system reset in the final design.

4.2 SPI Data

During our development, we discovered that the SPI data returned by the Samsung was offset by 8 bits from what we expected from the datasheet.

4.3 OLED Device Code Read

During our development, we were attempting to use a Device Code Read (command 0x0F) to verify our SPI connection to the OLED display. Our expectation was that the Device Code would return data based on command 0x0F from the datasheet, 0xC3D3.

However, we discovered that the device code was returning 6E63D6. Once we discovered this matched the part number, we were able to proceed with our integration under the assumption that the datasheet was incorrect.

4.4 SPI Writes to GRAM

Once we confirmed we were reading and writing correctly to the SPI port, we proceeded with the device initialization process. We used the SPI port to write test data into the graphics RAM of the display controller. This was done by using device commands *0x20 GRAM Address Set* and *0x22 GRAM Write* to place data in the GRAM. We then confirmed that the panel initialized successfully.

4.5 Lessons Learned

- Place all control signals at easily accessible test points, including power supply enable pins and reset pins.
- Follow device power-up and reset sequencing.
- Datasheets for OLED devices are currently in a major state of flux; inaccurate and out of date information is common.

5 Summary

The information in this application note is meant to provide a sample process that can be used to begin integrating OLED displays into OMAP35x SOM-LV and OMAP35x Torpedo SOM-based designs. If you encounter problems with your integration, Logic PD offers design support packages[6] through our Applications Engineering team in order to assist you.

[6] http://www.logicpd.com/support/support-packages/

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Appendix A: Schematics for the OLED Display Adaptor Board

The following pages contain the schematic of the OLED Display Adaptor Board created by Logic PD to integrate the CMEL C0240QGLA-T to the OMAP35x Development Kit.

IMPORTANT NOTE: Please be aware that during development we discovered the EN pin for the NCP5810 must be controlled by a GPIO. That change is not reflected in these schematics.

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TABLE OF CONTENTS	
PAGE	DESCRIPTION
1	TITLE PAGE
2	BASEBOARD CONNECTOR
3	OLED CIRCUITRY

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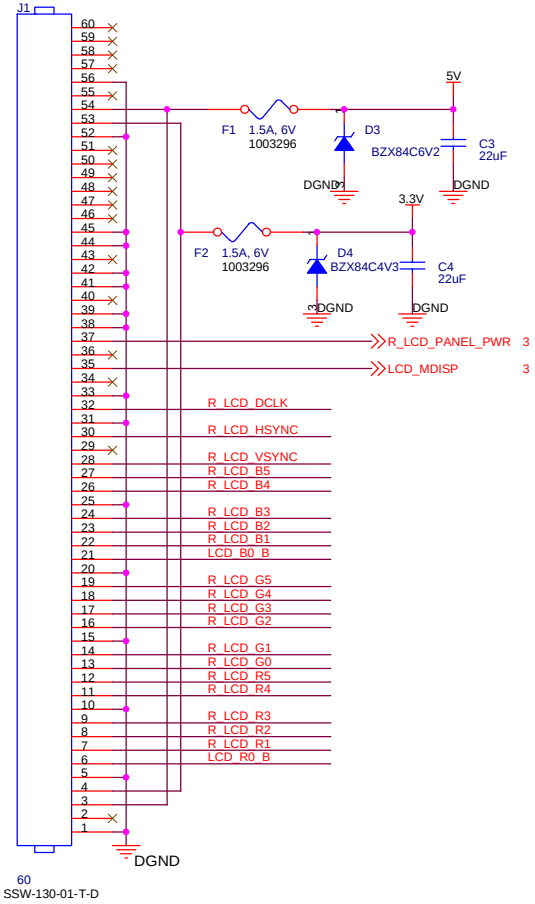
Title OLED DISPLAY ADAPTOR BOARD		Project	
Number	Thursday, February 03, 2011	Rev A	Sheet 1 Of 3

BASE BOARD CONNECTOR



LCD SELECT RESISTORS

NOTE: Keep the trace length between resistors to an absolute minimum

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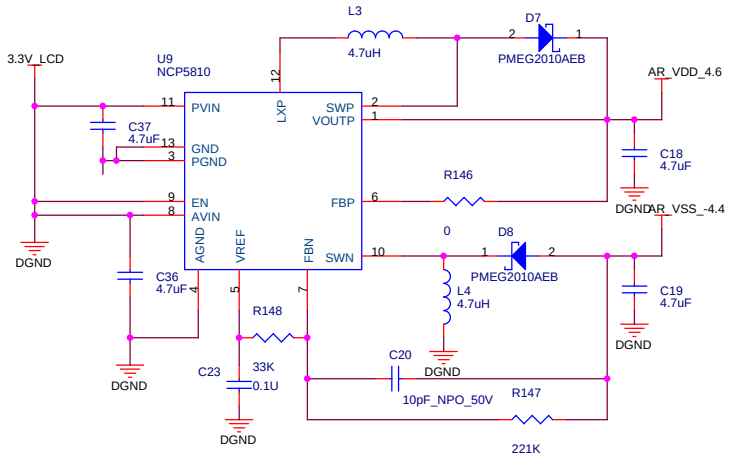
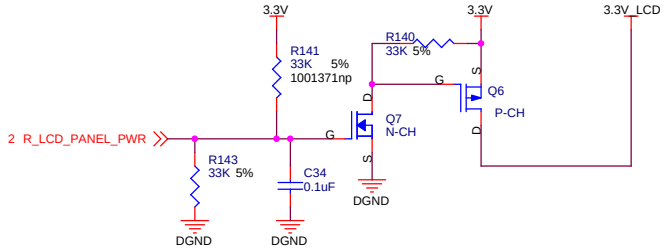
Number	Thursday, February 03, 2011	Rev A	Sheet 2 Of 3

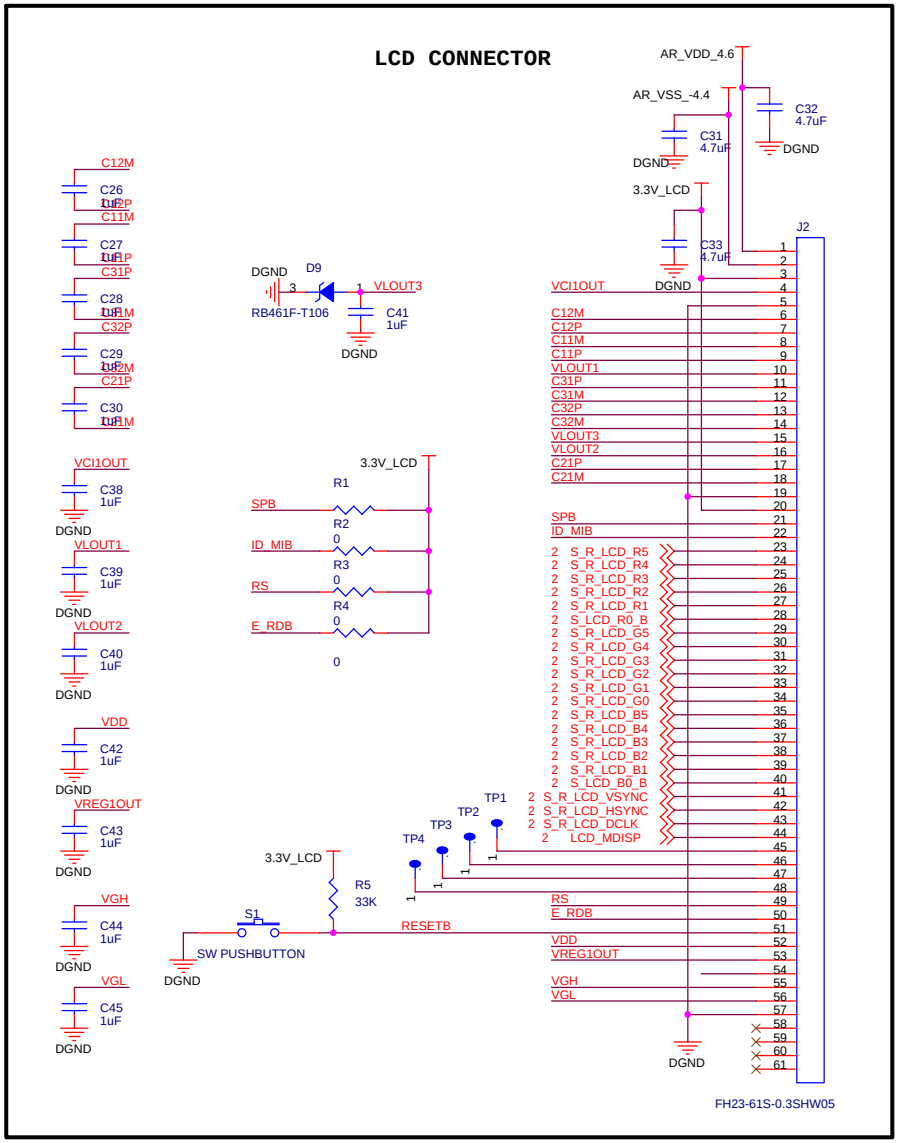
4.6V POWER SUPPLY



3.3V FOR LCD



LCD CONNECTOR



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Title OLED DISPLAY ADAPTOR BOARD		Project
Number	Thursday, February 03, 2011	Rev A / Sheet 3 Of 3