Selecting and Using GPIO Signals on OMAP35x SOMs

Application Note 421

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Abstract

This document provides information on how to select, access, and test general purpose input/output (GPIO) signals on the OMAP35x SOM-LV and OMAP35x Torpedo SOM.

Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	BSB	Initial release	NJK	10/08/10
B	SMC	-Table 2.1: Clarified that note 2 only applies to gpio_120-gpio_129 when muxed with MMC signals; -Table 2.2: Clarified that note 3 only applies to gpio_120-gpio_129 when muxed with MMC signals; -Section 3.1.1: Corrected address in GPIO output command	JCA	12/16/10
C	HJS	-Throughout: Updated template; updated links for new support site; -Table 2.2: Corrected information in *Torpedo SOM Signal* and *uP Signal* columns for J1.70	SO, RAH	09/05/13

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1 Introduction

This document provides information about how to select, access, and test general purpose input/output (GPIO) signals on the OMAP35x SOM-LV and OMAP35x Torpedo SOM.

1.1 Nomenclature, Notices, and Conventions Used in This Document

- Within this document OMAP35x is used to denote both the OMAP3530 and OMAP3503 processors.
- This document covers both the OMAP35x SOM-LV and OMAP35x Torpedo SOM. Use of "OMAP35x SOM" suggests text that applies to both platforms; information specific to one platform will call out the precise name.
- When referring to specific pins for signals, the connector/processor reference designator is called out first and then the pin number. For example, J1.115 represents pin 115 on connector J1; similarly, U4.D25 represents pin D25 on the OMAP processor (reference designator U4).

2 Selecting GPIO Signals

Many signals on the OMAP35x SOM can be used as GPIOs in an embedded system design. When designating a signal as a GPIO, it is important to verify that designation will not cause conflicts when trying to use other devices with the OMAP35x SOM. This section explains how to avoid those potential conflicts; however, it is the responsibility of the system engineer to confirm that the chosen GPIO signal does not conflict with the system design.

Voltage levels for all the signals recommended in this section are 1.8V; each signal is capable of being used as either an input or an output.

2.1 OMAP35x SOM-LV GPIO Selection

Table 2.1 shows a list of available GPIO signals after being filtered using the following criteria:

- The OMAP35x SOM-LV Schematic (PN 1014465A) was used in creating this document. In the unlikely event that an I/O is changed on a future revision of the schematic, that change will need to be evaluated to determine its impact, if any, on Table 2.1.
- Signals were removed from the list if they touch more than two nodes within the schematic net list. All recommended signals connect directly between the OMAP processor (U4) and one of the SOM-LV connectors (J1 or J2).
- GPIO_133 (uP_GPIO_0) and GPIO_11 (uP_GPIO_1) were removed since they are designated as output from LogicLoader; however, they can be used for testing purposes as demonstrated in this document.
- GPIO_60/GPMC_nBE0_CLE was removed since it connects to the Package-on-Package (PoP) NAND flash memory.
- The GPIO signals in Table 2.1 are all available on the OMAP processor. Additional GPIO signals may be available through the TPS65950 power management IC (PMIC); please see Appendix B: Configuring a TPS65950 PMIC Signal as a GPIO for more information.

Be sure to consider the following items when selecting a GPIO for your embedded system:

- Verify available GPIOs based on the specific SOM-LV schematic and system baseboard used in the final design.
- This list is based on the standard OMAP35x SOM-LV configuration (SOMOMAP3530-11-1672IFCR-A) and does not take into account signals that may become available when certain components are not populated, such as Bluetooth and Wi-Fi.

- Verify the voltage levels of each GPIO signal are compatible with the receiving signal.
- Verify availability for reset configuration and internal pull-up/down using the Texas Instruments (TI) *OMAP35x Applications Processor Technical Reference Manual*[1] (hereafter, *OMAP35x TRM*).
- Verify the GPIO you select is used in only one location in the pin mux of the OMAP35x processor; some GPIO signals can be found in multiple locations of the pin mux. These signals include but are not limited to: GPIO_120, GPIO_121, GPIO_122, GPIO_124, GPIO_125, GPIO_126, GPIO_130, and GPIO_131.

Table 2.1: OMAP35x SOM-LV Filtered GPIOs

J1/J2 Connection	U4 Connection	SOM-LV Signal	uP Signal	Notes
J1.15	U4.W21	nSUSPEND	McBSP1_CLKX/McBSP3_CLKX/GPIO_162	
J1.17	U4.K26	nSTANDBY	McBSP1_FSX/McSPI4_CS0/McBSP_FSX/GPIO_161	
J1.115	U4.D25	uP_nIRQC	CAM_STROBE/GPIO_126	
J1.117	U4.B23	uP_nIRQB	CAM_WEN/CAM_SHUTTER/GPIO_167	
J1.119	U4.C23	uP_nIRQA	CAM_FLD/CAM_GLOBAL_RESET/GPIO_98	
J1.132	U4.H20	uP_UARTB_RX	UART3_RX_IRRX/GPIO_165	
J1.134	U4.H21	uP_UARTB_TX	UART3_TX_IRTX/GPIO_166	
J1.136	U4.H18	uP_UARTB_CTS	UART3_CTS_RCTX/GPIO_163	
J1.138	U4.H19	uP_UARTB_RTS	UART3_RTS_SD/GPIO_164	
J1.139	U4.U3	uP_nBE1	GPMC_nBE1/GPIO_61	
J1.142	U4.B26	GPIO_111	CAM_XCLKB/GPIO_111	
J1.154	U4.U21	uP_UARTA_DSR	McBSP1_DR/McSPI4_SOMI/McBSP3_DR/GPIO_159	
J1.158	U4.Y8	uP_UARTA_RX	UART1_RX/MCBSP1_CLKR/MCSPI4_CLK/GPIO_151	
J1.160	U4.AA8	uP_UARTA_TX	UART1_TX/SSI1_DAT_TX/GPIO_148	
J1.162	U4.W8	uP_UARTA_CTS	UART1_CTS/SSI1_RDY_TX/HSUSB3_TLL_CLK/GPIO_150	
J1.164	U4.AA9	uP_UARTA_RTS	UART1_RTS/SSI1_FLAG_TX/GPIO_149	
J1.165	U4.D26	LCD_HSYNC	DSS_HSYNC/GPIO_67	
J1.167	U4.D27	LCD_VSYNC	DSS_VSYNC/GPIO_68	
J1.171	U4.D28	LCD_DCLK	DSS_PCLK/GPIO_66	
J1.175	U4.E27	LCD_MDISP	DSS_ACBIAS/GPIO_69	
J1.185	U4.AD27	LCD_D11	DSS_D11/SDI_DAT1P/GPIO_81	1
J1.187	U4.AB28	LCD_D12	DSS_D12/SDI_DAT2N/GPIO_82	1
J1.191	U4.AB27	LCD_D13	DSS_D13/SDI_DAT2P/GPIO_83	1
J1.193	U4.AA28	LCD_D14	DSS_D14/SDI_DAT3N/GPIO_84	1
J1.195	U4.AA27	LCD_D15	DSS_D15/SDI_DAT3P/GPIO_85	1
J1.197	U4.AH24	LCD_D5	DSS_D5/UART3_TX_IRTX/DY2/GPIO_75	1
J1.199	U4.E26	LCD_D6	DSS_D6/UART1_TX/GPIO_76	
J1.201	U4.F28	LCD_D7	DSS_D7/UART1_RX/GPIO_77	
J1.203	U4.F27	LCD_D8	DSS_D8/GPIO_78	
J1.205	U4.G26	LCD_D9	DSS_D9/GPIO_79	
J1.207	U4.AD28	LCD_D10	DSS_D10/SDI_DAT1N/GPIO_80	1
J1.211	U4.AG22	LCD_D0	DSS_D0/UART1_CTS/DX0/GPIO_70	1

[1] www.ti.com/product/omap3530

J1/J2 Connection	U4 Connection	SOM-LV Signal	uP Signal	Notes
J1.213	U4.AH22	LCD_D1	DSS_D1/UART1_RTS/DY0/GPIO_71	1
J1.215	U4.AG23	LCD_D2	DSS_D2/DX1/GPIO_72	1
J1.217	U4.AH23	LCD_D3	DSS_D3/DY1/GPIO_73	1
J1.219	U4.AG24	LCD_D4	DSS_D4/UART3_RX_IRRX/DX2/GPIO_74	1
J1.220	U4.AG4	uP_SPI_CS1	MMC2_DAT2/McSPI3_CS1/GPIO_134	
J1.222	U4.AF4	uP_SPI_CS0	MMC2_DAT3/McSPI3_CS0/GPIO_135	
J1.224	U4.AH5	uP_SPI_SOMI	MMC2_DAT0/McSPI3_SOMI/GPIO_132	
J1.226	U4.AG5	uP_SPI_SIMO	MMC2_CMD/McSPI3_SIMO/GPIO_131	
J2.10	U4.AE22	uP_CLKOUT2_26Mhz	SYS_CLKOUT2/GPIO_186	
J2.126	U4.Y21	SIM0_nDETECT	McBSP1_CLKR/McSPI4_CLK/SIM_CD/GPIO_156	
J2.127	U4.A24	CSI_HSYNC	CAM_HS/SSI2_DAT_TX/GPIO_94	
J2.128	U4.P26	SIM0_CLK	MMC1_DAT5/SIM_CLK/GPIO_127	2, 3
J2.131	U4.A23	CSI_VSYNC	CAM_VS/SSI2_FLAG_TX/GPIO_95	
J2.132	U4.P27	SIM0_IO/TX	MMC1_DAT4/SIM_IO/GPIO_126	2, 3
J2.133	U4.AG17	CSI_D0	CAM_D0/CSI2_DX2/GPIO_99	4
J2.135	U4.AH17	CSI_D1	CAM_D1/CSI2_DY2/GPIO_100	4
J2.136	U4.R25	SIM0_nRESET	MMC1_DAT7/SIM_RST/GPIO_129	2, 3
J2.137	U4.B24	CSI_D2	CAM_D2/SSI2_RDY_TX/GPIO_101	
J2.139	U4.C24	CSI_D3	CAM_D3/SSI2_DAT_RX/GPIO_102	
J2.141	U4.D24	CSI_D4	CAM_D4/SSI2_FLAG_RX/GPIO_103	
J2.143	U4.A25	CSI_D5	CAM_D5/SSI2_RDY_RX/GPIO_104	
J2.145	U4.K28	CSI_D6	CAM_D6/GPIO_105	
J2.147	U4.L28	CSI_D7	CAM_D7/GPIO_106	
J2.151	U4.K27	CSI_D8	CAM_D8/GPIO_107	
J2.153	U4.L27	CSI_D9	CAM_D9/GPIO_108	
J2.155	U4.B25	CSI_D10	CAM_D10/SSI2_WAKE/GPIO_109	
J2.167	U4.C25	CSI_MCLK	CAM_XCLKA/GPIO_96	
J2.171	U4.C27	CSI_PCLK	CAM_PCLK_GPIO_97	
J2.174	U4.AC28	LCD_D23	DSS_D23/SDI_CLKN/GPIO_93	1
J2.176	U4.AC27	LCD_D22	DSS_D22/SDI_CLKP/GPIO_92	1
J2.178	U4.J26	LCD_D21	DSS_D21/SDI_STP/McSPI3_CS0/DSS_DATA3/GPIO_91	1
J2.180	U4.E28	LCD_D20	DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_DATA2/GPIO_90	1
J2.181	U4.AH18	CSI1_DY1	CSI2_DY1/GPIO_115	4
J2.182	U4.H25	LCD_D19	DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_DATA1/GPIO_89	1
J2.183	U4.AG18	CSI1_DX1	CSI2_DX1/GPIO_114	4
J2.184	U4.H26	LCD_D18	DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_DATA0/GPIO_88	1
J2.185	U4.AH19	CSI1_DY0	CSI2_DY0/GPIO_113	4
J2.186	U4.H27	LCD_D17	DSS_D17/GPIO_87	1
J2.187	U4.AG19	CSI1_DX0	CSI2_DX0/GPIO_112	4
J2.188	U4.G25	LCD_D16	DSS_D16/GPIO_86	1

TABLE NOTES:

1. VPLL2 must be enabled to use GPIO_70 through GPIO_75, GPIO_80 through GPIO_85, GPIO_92, and GPIO_93 GPIO signals. VPLL2 is enabled by default when the signals are used by the LCD controller in LogicLoader, Windows CE BSP, and Linux BSP. See Appendix C: Enabling VPLL2 LogicLoader I2C Commands for more details.
2. Due to buffer strength, an external serial resistor must be connected to the BGA balls where GPIO_120 through GPIO_129 are muxed with MMC signals; the resistor value is dependent on the implementation in the final system design. More information about this requirement can be found in the "General-Purpose Interface Environment" chapter of the *OMAP35x TRM.*
3. GPIO_120 through GPIO_129 require setting up special registers in the OMAP35x that control PBIAS settings; please refer to the *OMAP35x TRM* for more information.
4. GPIO_99, GPIO_100, and GPIO_112 through GPIO_115 can only be used as GPI (input only) and require that VAUX4 be enabled. See "Section 7: Power Supplies" in Logic PD's *AN 388 OMAP35x SOM-LV Power Management*[2] for information on how to enable the VAUX4 power supply.

2.2 OMAP35x Torpedo SOM GPIO Selection

Table 2.2 shows a list of available GPIO signals after being filtered using the following criteria:

- The *OMAP 3 Torpedo Schematic* (PN 1013989A) was used in creating this document. In the unlikely event that an I/O is changed on a future revision of the schematic, that change will need to be evaluated to determine its impact, if any, on Table 2.2.
- Signals were removed from the list if they touch more than two nodes within the schematic net list. All recommended signals connect directly between the OMAP processor (U4) and one of the SOM connectors (J1 or J2).
- GPIO_179 (MCSPI2_SIMO) and GPIO_180 (MCSPI2_SOMI) were removed since they are designated as output from LogicLoader; however, they can be used for testing purposes as demonstrated in this document.
- GPIO_60/GPMC_nBE0_CLE was removed since it connects to the Package-on-Package (PoP) NAND flash memory.
- The GPIO signals in Table 2.2 are all available on the OMAP processor. Additional GPIO signals may be available through the TPS65950 power management IC (PMIC); please see Appendix A: OMAP35x SOM-LV to Breakout Board Signal Mapping for more information.

Be sure to consider the following items when selecting a GPIO for your embedded system:

- Verify available GPIOs based on the specific SOM schematic and system baseboard used in the final design.
- This list is based on the standard OMAP35x Torpedo SOM configuration (SOMOMAP3530-21-1670AGCR-A) and does not take into account signals that may become available when certain resistor packs are populated.
- Verify the voltage levels of each GPIO signal are compatible with the receiving signal.
- Verify availability for reset configuration and internal pull-up/down using the Texas Instruments (TI) *OMAP35x Applications Processor Technical Reference Manual*[3] (hereafter, *OMAP35x TRM*).

[2] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1108
[3] www.ti.com/product/omap3530

- Verify the GPIO you select is used in only one location in the pin mux of the OMAP35x processor; some GPIO signals can be found in multiple locations of the pin mux. These signals include but are not limited to: GPIO_120, GPIO_121, GPIO_122, GPIO_124, GPIO_125, GPIO_126, GPIO_130, and GPIO_131.

Table 2.2: OMAP35x Torpedo SOM Filtered GPIOs

J1/J2 Connection	U4 Connection	Torpedo SOM Signal	uP Signal	Notes
J1.7	U4.L3	UP_A9	GPMC_A9/SYS_nDMAREQ2/GPIO_42	1
J1.11	U4.H3	uP_nCS1	GPMC_nCS1/GPIO_52	
J1.13	U4.M3	UP_A8	GPMC_A8/GPIO_41	1
J1.19	U4.T4	uP_BUS_CLK	GPMC_CLK/GPIO_59	1
J1.21	U4.U3	uP_nBE1	GPMC_nBE1/GPIO_61	
J1.28	U4.P8	uP_nCS6	GPMC_nCS6/SYS_nDMAREQ3/McBSP4_DX/GPT11_PWM_EVT/GPIO_57	
J1.29	U4.H2	UP_D8	GPMC_D8/GPIO_44	1, 2
J1.31	U4.K2	UP_D9	GPMC_D9/GPIO_45	1, 2
J1.32	U4.R8	uP_nCS5	GPMC_nCS5/SYS_nDMAREQ2/McBSP4_DR/GPT10_PWM_EVT/GPIO_56	
J1.34	U4.T8	uP_nCS4	GPMC_nCS4/SYS_nDMAREQ1/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55	
J1.36	U4.U8	uP_nCS3	GPMC_nCS3/SYS_nDMAREQ0/GPIO_54	
J1.38	U4.K3	UP_A10	GPMC_A10/SYS_nDMAREQ3/GPIO_43	1
J1.40	U4.V8	uP_nCS2	GPMC_nCS2/GPIO_53	
J1.41	U4.R2	UP_D12	GPMC_D12/GPIO_48	1, 2
J1.42	U4.K4	UP_A4	GPMC_A4/GPIO_37	1
J1.43	U4.P1	UP_D10	GPMC_D10/GPIO_46	1, 2
J1.44	U4.L4	UP_A3	GPMC_A3/GPIO_36	1
J1.45	U4.R1	UP_D11	GPMC_D11/GPIO_47	1, 2
J1.46	U4.M4	UP_A2	GPMC_A2/GPIO_35	1
J1.47	U4.T2	UP_D13	GPMC_D13/GPIO_49	1, 2
J1.48	U4.N4	UP_A1	GPMC_A1/GPIO_34	1
J1.50	U4.N3	UP_A7	GPMC_A7/GPIO_40	1
J1.51	U4.V3	MCSPI2_CS1	McSPI2_CS1/GPT8_PWM_EVT/HSUSB2_TLL_DATA3/USUSB2_DATA3/MM2_TXEN_N/GPIO_182	
J1.52	U4.R3	UP_A6	GPMC_A6/GPIO_39	1
J1.54	U4.T3	UP_A5	GPMC_A5/GPIO_38	1
J1.58	U4.Y4	MCSPI2_CS0	McSPI2_CS0/GPT11_PWM_EVT/HSUSB2_TLL_DATA6/HSUSB2_DATA6/GPIO_181	
J1.59	U4.W1	UP_D14	GPMC_D14/GPIO_50	1, 2
J1.60	U4.AA4	MCSPI1_SOMI	McSPI1_SOMI/MMC2_DAT6/GPIO_173	
J1.62	U4.AD1	MCBSP4_DR	McBSP4_DR/SSI1_FLAG_RX/HSUSB3_TLL_DATA0/MM3_RXRCV/GPIO_153	
J1.63	U4.Y1	UP_D15	GPMC_D15/GPIO_51	1, 2
J1.64	U4.AB3	MCSPI1_CLK	McSPI1_CLK/MMC2_DAT4GPIO_171	
J1.66	U4.AB4	MCSPI1_SIMO	McSPI1_SIMO/MMC2_DAT5/GPIO_172	
J1.67	U4.AA3	MCSPI2_CLK	McSPI2_CLK/HSUSB2_TLL_DATA7/HSUSB2_DATA7/GPIO_178	

J1/J2 Connection	U4 Connection	Torpedo SOM Signal	uP Signal	Notes
J1.68	U4.W8	uP_UARTA_CTS	UART1_CTS/SSI1_RDY_TX/HSUSB3_TLL_CLK/GPIO_150	
J1.69	U4.AC3	MCSPI1_CS1	McSPI1_CS1/ADPLLV2D_DITHERING_EN2/MMC3_CMD/GPIO_175	
J1.70	U4.Y8	uP_UARTA_RX	UART1_RX/MCBSP1_CLKR/MCSPI4_CLK/GPIO_151	
J1.71	U4.AC2	MCSPI1_CS0	McSPI1_CS0/MMC2_DAT7/GPIO_174	
J1.72	U4.AA8	uP_UARTA_TX	UART1_TX/SSI1_DAT_TX/GPIO_148	
J1.73	U4.AC1	LCD_PANEL_PWR	McBSP4_FSX/SSI1_WAKE/HSUSB3_TLL_DATA3/MM3_TXEN_n/GPIO_155	
J1.74	U4.AA9	uP_UARTA_RTS	UART1_RTS/SSI1_FLAG_TX/GPIO_149	
J1.75	U4.AD2	LCD_BACKLIGHT_PWR	McBSP4_DX/SSI1_RDY_RX//HSUSB3_TLL_DATA2/MM3_TXDAT/GPIO_154	
J1.84	U4.AH5	SD2_DATA0	MMC2_DAT0/McSPI3_SOMI/GPIO_132	
J1.91	U4.AF4	SD2_DATA3	MMC2_DAT3/McSPI3_CS0/GPIO_135	
J1.93	U4.AG4	SD2_DATA2	MMC2_DAT2/McSPI3_CS1/GPIO_134	
J1.95	U4.AH4	SD2_DATA1	MMC2_DAT1/GPIO_133	
J1.97	U4.AG5	SD2_CMD	MMC2_CMD/McSPI3_SIMO/GPIO_131	
J1.98	U4.N8	uP_IODIR	GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58	
J2.12	U4.D26	LCD_HSYNC	DSS_HSYNC/GPIO_67	
J2.14	U4.D27	LCD_VSYNC	DSS_VSYNC/GPIO_68	
J2.16	U4.E27	LCD_MDISP	DSS_ACBIAS/GPIO_69	
J2.18	U4.E26	LCD_D6	DSS_D6/UART1_TX/GPIO_76	
J2.20	U4.E28	LCD_D20	DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_DATA2/GPIO_90	
J2.22	U4.G26	LCD_D9	DSS_D9/GPIO_79	
J2.24	U4.F27	LCD_D8	DSS_D8/GPIO_78	
J2.26	U4.F28	LCD_D7	DSS_D7/UART1_RX/GPIO_77	
J2.29	U4.A25	CSI_D5	CAM_D5/SSI2_RDY_RX/GPIO_104	
J2.31	U4.B24	CSI_D2	CAM_D2/SSI2_RDY_TX/GPIO_101	
J2.33	U4.C24	CSI_D3	CAM_D3/SSI2_DAT_RX/GPIO_102	
J2.34	U4.H25	LCD_D19	DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_DATA1/GPIO_89	
J2.35	U4.D24	CSI_D4	CAM_D4/SSI2_FLAG_RX/GPIO_103	
J2.36	U4.H26	LCD_D18	DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_DATA0/GPIO_88	
J2.37	U4.H18	uP_UARTB_CTS	UART3_CTS_RCTX/GPIO_163	
J2.39	U4.H19	uP_UARTB_RTS	UART3_RTS_SD/GPIO_164	
J2.40	U4.J26	LCD_D21	DSS_D21/SDI_STP/McSPI3_CS0/DSS_DATA3/GPIO_91	
J2.41	U4.H20	uP_UARTB_RX	UART3_RX_IRRX/GPIO_165	
J2.42	U4.M27	SD1_CMD	MMC1_CMD/MS_BS/GPIO_121	3, 4, 5
J2.43	U4.H21	uP_UARTB_TX	UART3_TX_IRTX/GPIO_166	
J2.44	U4.N25	SD1_DATA2	MMC1_DAT2/MS_DAT2/GPIO_124	3, 4, 5
J2.45	U4.K26	MCSPI4_CS0	McBSP1_FSX/McSPI4_CS0/McBSP_FSX/GPIO_161	
J2.46	U4.N26	SD1_DATA1	MMC1_DAT1/MS_DAT1/GPIO_123	3, 4, 5
J2.48	U4.N27	SD1_DATA0	MMC1_DAT0/MS_DAT0/GPIO_122	3, 4, 5

J1/J2 Connection	U4 Connection	Torpedo SOM Signal	uP Signal	Notes
J2.50	U4.P28	SD1_DATA3	MMC1_DAT3/MS_DAT3/GPIO_125	3, 4, 5
J2.52	U4.P27	SD1_DATA4	MMC1_DAT4/SIM_IO/GPIO_126	3, 5
J2.54	U4.P26	SD1_DATA5	MMC1_DAT5/SIM_CLK/GPIO_127	3, 5
J2.56	U4.R27	SD1_DATA6	MMC1_DAT6/SIM_PWRCTRL/GPIO_128	3, 5
J2.58	U4.R25	SD1_DATA7	MMC1_DAT7/SIM_RST/GPIO_129	3, 5
J2.66	U4.AA28	LCD_D14	DSS_D14/SDI_DAT3N/GPIO_84	6
J2.68	U4.AB27	LCD_D13	DSS_D13/SDI_DAT2P/GPIO_83	6
J2.70	U4.AB28	LCD_D12	DSS_D12/SDI_DAT2N/GPIO_82	6
J2.72	U4.AA25	uP_UARTC_TX	UART2_TX/MCBSP3_CLKX/GPT11_PWM_EVT/GPIO_146	
J2.74	U4.AB25	uP_UARTC_RTS	UART2_RTS/MCBSP3_DR/GPT10_PWM_EVT/GPIO_145	
J2.76	U4.AB26	uP_UARTC_CTS	UART2_CTS/MCBSP3_DX/GPT9_PWM_EVT/GPIO_144	
J2.78	U4.AA27	LCD_D15	DSS_D15/SDI_DAT3P/GPIO_85	6
J2.79	U4.AG23	LCD_D2	DSS_D2/DX1/GPIO_72	6
J2.80	U4.AC27	LCD_D22	DSS_D22/SDI_CLKP/GPIO_92	6
J2.81	U4.AH23	LCD_D3	DSS_D3/DY1/GPIO_73	6
J2.82	U4.AD28	LCD_D10	DSS_D10/SDI_DAT1N/GPIO_80	6
J2.83	U4.AH22	LCD_D1	DSS_D1/UART1_RTS/DY0/GPIO_71	6
J2.84	U4.AD27	LCD_D11	DSS_D11/SDI_DAT1P/GPIO_81	6
J2.85	U4.AG17	CSI_D0	CAM_D0/CSI2_DX2/GPIO_99	7
J2.86	U4.AD25	uP_UARTC_RX	UART2_RX/MCBSP3_FSX/GPT8_PWM_EVT/GPIO_147	
J2.87	U4.AH17	CSI_D1	CAM_D1/CSI2_DY2/GPIO_100	7
J2.88	U4.AG25	uP_CLKOUT1_26Mhz	SYS_CLKOUT1/GPIO_10	
J2.94	U4.AG24	LCD_D4	DSS_D4/UART3_RX_IRRX/DX2/GPIO_74	6
J2.96	U4.AH24	LCD_D5	DSS_D5/UART3_TX_IRTX/DY2/GPIO_75	6
J2.98	U4.AG22	LCD_D0	DSS_D0/UART1_CTS/DX0/GPIO_70	6

TABLE NOTES:

1. These signals also have a possible connection to the top PoP BGA footprint. Caution must be used when considering these signals as alternative GPIO function.
2. These signals are not available when using PoP memories with 16-bit NAND memory.
3. Due to buffer strength, an external serial resistor must be connected to the BGA balls where GPIO_120 through GPIO_129 are muxed with MMC signals; the resistor value is dependent on the implementation in the final system design. More information about this requirement can be found in the “General-Purpose Interface Environment” chapter of the *OMAP35x TRM*.
4. VMMC1 must be enabled to use GPIO_120 through GPIO_125. Note that VMMC1 can be enabled for 1.8V or 3.0V operation.
5. GPIO_120 through GPIO_129 require setting up special registers in the OMAP35x that control PBIAS settings; please refer to the *OMAP35x TRM* for more information.
6. VPLL2 must be enabled to use GPIO_70 through GPIO_75, GPIO_80 through GPIO_85, GPIO_92, and GPIO_93 GPIO signals. VPLL2 is enabled by default when the signals are used by the LCD controller in LogicLoader, Windows CE BSP, and Linux BSP. See Appendix C: Enabling VPLL2 LogicLoader I2C Commands.

7. GPIO_99, GPIO_100, and GPIO_112 through GPIO_115 can only be used as GPI (input only) and require that VAUX4 be enabled. See the “Section 7: Power Supplies” in Logic PD’s *AN 416 OMAP35x Torpedo SOM Power Management*[4] for information on how to enable the VAUX4 power supply.

[4] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=964

3 Configuring GPIO Examples

This section will describe how to program GPIO_111 on the OMAP35x SOM using LogicLoader, Windows CE, and Linux. Each example will show how to configure GPIO_111 as an output or an input. To access GPIO_111 on the Zoom™ OMAP35x SOM-LV Development Kit or the Zoom OMAP35x Torpedo Development Kit, use the following connections.

- OMAP35x SOM-LV Development Kit
  - GPIO_111 access is through J17.36 on the breakout board.
  - Ground reference in the examples below is J17.1 on the breakout board.
  - 1.8V reference in the examples below is J18.68 (VIO_1V8) on the breakout board.
- OMAP35x Torpedo Development Kit
  - GPIO_111 access is through J6.20 on the baseboard.
  - Ground reference in the examples below is J6.25 on the baseboard.
  - 1.8V reference in the examples below is J30.22 on the baseboard.

3.1 Configuring GPIO Signals using LogicLoader

It is possible to set up and configure GPIOs on both the OMAP35x processor and TPS65950 PMIC by using scripting functionality provided in LogicLoader. Examples of how to use processor GPIO functionality are provided in this section (there is an example in Appendix B: Configuring a TPS65950 PMIC Signal as a GPIO that shows how to access TPS65950 GPIO signals using LogicLoader).

In this example of accessing a GPIO signal on the OMAP35x processor, signal GPIO_111 will be driven high and low. According to Logic PD's *OMAP35x SOM-LV Schematic* and *High-Density Expansion Breakout Board Schematic*, GPIO_111 is tied to the OMAP35x processor CAM_XCLKB/GPIO_111 signal and is routed to pin J17.36 on the breakout board. If you wish to monitor the output from the breakout board, attach a digital voltmeter, oscilloscope probe, or logic analyzer to J17.36.

First, we need to determine which of the pin mux registers within the OMAP35x processor correspond to the CAM_XCLKB signal; this information can be found in "Chapter 7: System Control Module" of TI's *OMAP35x TRM*. Locate the CAM_XCLKB signal in "Table 7-4: Core Control Module Pad Configuration Register Field." On the row with CAM_XCLKB, notice the Mode 4 column corresponds with GPIO_111. In other words, we want to change the MUXMODE to 4 to enable the GPIO function. Also notice that the CAM_XCLKB pad configuration can be found in the CONTROL_PADCONF_CAM_D11[31:16] register at address 0x4800_212C; this means that CAM_XCLKB control is in the upper half of that register.

1. At the losh> prompt in LogicLoader, enter the command below.

```
losh> x /w 0x4800212c                  # Read contents of
CONTROL_PADCONF_CAM_D11 0x4800212c  010f011c
....
```


2. Returning to TI's *OMAP35x TRM*, "Table 7-74: CONTROL_PADCONF_X" indicates we want to set MUXMODE to 0x4; the rest of the bits can remain the same.

```
losh> temp = $@                          # Set temp equal to value seen in
previous command
losh> temp = $temp & 0x0000ffff          # Clear upper 16 bit
losh> temp = $temp | 0x00040000          # Set upper 16 bits for MUXMODE 4
losh> w /w 0x4800212c $temp             # Set the MUXMODE of CAM_XCLKB
for GPIO_111
writing: (8) *4800212c = 0004011c
```

Next, we'll look at "Chapter 24: General-Purpose I/O (GPIO) Interface" of the *OMAP35x TRM* to configure GPIO_111. The OMAP35x processor has six banks of GPIOs; each bank contains thirty-two GPIOs. GPIO_111 can be found in bank GPIO4 as bit number 15 (see "Table 24-5: GPIO Channel Description" in the *OMAP35x TRM*).

3.1.1 GPIO Output

Building on the steps in the section above, it is now possible to configure the GPIO as an output. GPIOs are inputs by default; if you need the GPIO to be an output, it is best to configure the appropriate output level before changing the signal direction.

1. Write to GPIO4 GPIO_SETDATAOUT to set the signal high.

```
losh> w /w 0x49054094 0x00008000       # Write the SETDATAOUT with bit 15
set, GPIO_111
                                         # high
writing: (8) *49058094 = 00008000
```

2. Next, we need to set the GPIO direction with GPIO4 GPIO_OE.

```
losh> x /w 0x49054034                  # Set temp equal to value seen in
previous command
0x49058034  ffffffff
losh> temp = $@                         # Clear upper 32 bit
losh> temp = $temp & 0xffff7fff          # Clear just the bit associated
to GPIO_111
losh>  w /w 0x49054034 $temp            # Write the modified value of
GPIO_OE with bit 15,
                                         # GPIO_111 set as output
writing: (8) *49054034 = 0ffff7fff
```

At this point, the GPIO signal will be high on the measuring instrumentation.

3. To send it low, write to GPIO4 GPIO_CLEARDATAOUT.

```
losh>  w /w 0x49054090 0x00008000       # Write the CLEARDATAOUT with bit
15 set, GPIO_111
                                         # low
writing: (8) *49054090 = 00008000
```


3.1.2 GPIO Input

To read the value of GPIO_111, reset the board, tie the pin ground reference stated at the beginning of Section 0, and perform the steps below.

1. At the losh> prompt in LogicLoader, enter the command below.

```
losh> x /w 0x4800212c                # Read contents of
CONTROL_PADCONF_CAM_D11 0x4800212c  010f011c
```

2. Returning to TI's *OMAP35x TRM*, "Table 7-74: CONTROL_PADCONF_X" indicates we want to set MUXMODE to 0x4; the rest of the bits can remain the same.

```
losh> temp = $@                      # Set temp equal to value seen in
previous command
losh> temp = $temp & 0x0000ffff      # Clear upper 16 bit
losh> temp = $temp | 0x01040000      # Set upper 16 bits for MUXMODE 4
losh> w /w 0x4800212c $temp         # Set the MUXMODE of CAM_XCLKB for
GPIO_111 and the input
writing: (8) *4800212c = 0104011c
```

3. Now tie the pin to 1.8V reference.

```
losh> x /w 0x49054038          #Read the values on GPIO bank 4
0x49054038  00008000                          ....
```

3.2 Configuring GPIO Signals in Windows CE

This section describes how to access GPIO signals on the OMAP35x processor using Logic PD's OMAP35x Windows CE 6.0 BSP version 2.0.0 or later. Logic PD provides an application programming interface (API) in the BSP. The API header information can be found in the following directory:

.\WINCE600\PLATFORM\COMMON\SRC\SOC\OMAP35XX_TPS659XX_TI_V1\inc\gpio.h

As previously stated, GPIO_133 and uP_GPIO_1 signals on the OMAP35x SOM-LV are not recommended for use in a production system. However, they can be used for testing purposes. For additional information on how uP_GPIO_1 is used within the Windows CE BSP, refer to the code in the following BSP routine:

src\oal\oallib\debug.c OEMWriteDebugLED()

3.2.1 GPIO_Win32 Sample Application

A Visual Studio 2005 GPIO_Win32 sample application is available for download from Logic PD's website. Using this application you can drive GPIO_133 on the OMAP35x SOM. At this time, please download the Logic PD GPIO_Win32 sample application.[5]

After the download has completed, extract the ZIP file and locate the *gpio_win32_readme.txt* file. Please read this file for specific system requirements and instructions on how to use the sample application before continuing further in this application note.

[5] http://support.logicpd.com/DesktopModules/Bring2mind/DMX/Download.aspx?portalid=0&EntryId=1137

3.2.2 Modifying Sample Application for GPIO_111

The following sections will describe how to change the GPIO_Win32 sample application to toggle GPIO_111 instead of GPIO_133.

To verify the GPIO_111 signal is truly toggling, measure the voltage on the appropriate pin for your development kit:

- J6.20 on the OMAP35x Torpedo Development Kit baseboard
- J17.36 on the breakout board connected to the OMAP35x SOM-LV Development Kit

NOTE: If a different GPIO signal is desired, please refer to Section 2. If you are using the OMAP35x SOM-LV Development Kit, please refer to Appendix A: OMAP35x SOM-LV to Breakout Board Signal Mapping to determine which breakout board pin must be probed for testing.

3.2.2.1 Build Modified GPIO_Win32 Sample Application

Before modifying the GPIO_Win32 sample application, the OMAP35x processor must be configured for pin muxing.

1. Locate the *platform.c* file in the OMAP35x Windows CE 6.0 BSP Source at *platform\logic_som_omap35x\src\oal\oallib\platform.c*.
2. In the *platform.c* file, add the following line to the */*Specific GPIO*/* section.

```
OUTREG16(&pConfig->CONTROL_PADCONF_CAM_XCLKB, (INPUT_DISABLE |
PULL_INACTIVE | MUX_MODE_4)); /*CAM_XCLKB*/
```

On the OMAP35x SOM-LV, this section begins at line #568; on the OMAP35x Torpedo SOM, this section begins at line #461. If using an OMAP35x Torpedo SOM, you will have to add the specific GPIO pin into the pin mux section.

The change to this line is highlighted in blue in Figure 3.1 below.

```
00599: /*CAMERA*/
00600: OUTREG16(&pConfig->CONTROL_PADCONF_CAM_XCLKA,    (INPUT_DISABLE | PULL_INACTIVE | MUX_MODE_7)); /*SAFE MODE          : CAM_XCLKA/GPIO_96
00601: OUTREG16(&pConfig->CONTROL_PADCONF_CAM_XCLKB,    (INPUT_DISABLE | PULL_INACTIVE | MUX_MODE_4)); /*GPIO_111           : CAM_XCLKB/GPIO_111
00602: OUTREG16(&pConfig->CONTROL_PADCONF_CAM_FLD,     (INPUT_ENABLE | PULL_UP    | MUX_MODE_4)); /*GPIO_98          : CAM_FLD/CAM_GLOBAL_RESET/GPIO_9
00603: OUTREG16(&pConfig->CONTROL_PADCONF_CAM_WEN,     (INPUT_ENABLE | PULL_UP    | MUX_MODE_4)); /*GPIO_167           : CAM_WEN/CAM_SHUTTER/GPIO_167
00604: OUTREG16(&pConfig->CONTROL_PADCONF_CAM_STROBE,  (INPUT_ENABLE | PULL_UP    | MUX_MODE_4)); /*GPIO_126           : CAM_STROBE/GPIO_126
```

Figure 3.1: Platform.c Example

3. Perform a build by selecting Build > Advance Build Commands > Build Current BSP and Subprojects.

4. Next, change line 35 in the *GPIO_Win32.cpp* file of the GPIO_Win32 sample application to **`#define GPIO_LED 111 //SOM-LV GPIO_111`** as shown in Figure 3.2 below.

```
#ifdef BSP_TORPEDO
#define GPIO_DEVICE_NAME        L"TWL1:"
#define GPIO_LED                17 //Torpedo PMIC GPIO 17 - J31.15
#else
#define GPIO_DEVICE_NAME        L"GIO1:"
//#define GPIO_LED              133 //SOM-LV uP_GPIO_0
#define GPIO_LED                111 //SOM-LV uP_GPIO_3

#endif
```

Figure 3.2: GPIO_Win32 Sample Application (GPIO_Win32.cpp)

5. Next, select Build > Build Solution in your GPIO_Win32 sample application to build in the changes.
6. Copy your newly modified GPIO_Win32 sample application from the build directory.

   The location of the build directory can be seen in the Visual Studio 2005 Output window as shown in Figure 3.3 below.

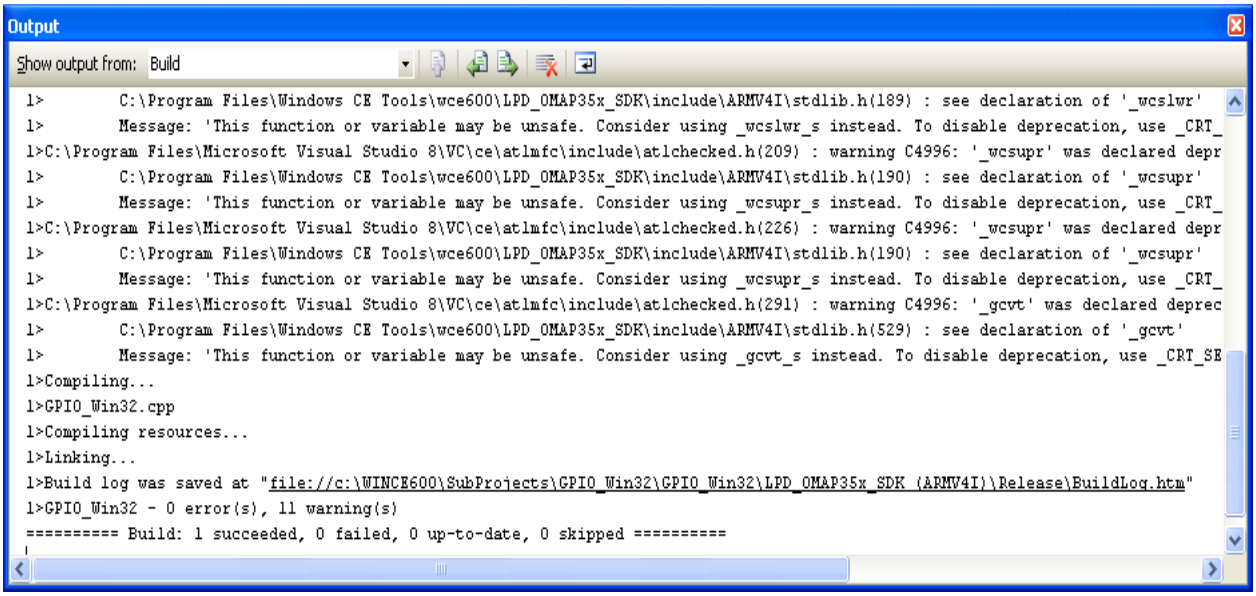

Figure 3.3: Visual Studio 2005 Output Window

Your application will exist in the same location as the *BuildLog.htm* file. The location of the *BuildLog.htm* file is seen in the Visual Studio 2005 Output window as the third line from the bottom. Figure 3.4 shows the files in the GPIO_Win32 sample application build directory.

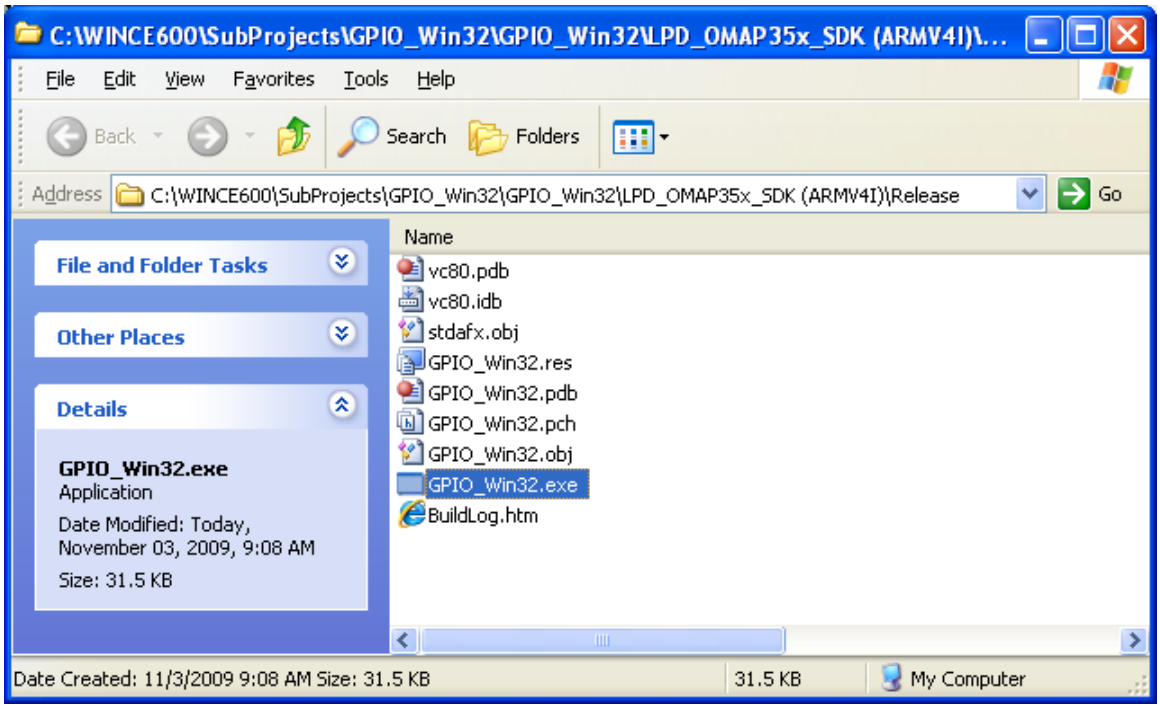

Figure 3.4: GPIO_Win32 Application Build Directory

7. Paste the copied GPIO_Win32 sample application to an SD card.

3.2.2.2 Run Modified GPIO_Win32 Sample Application from SD Card

1. Insert the SD card containing the modified GPIO_Win32 sample application into your OMAP35x Development Kit.
2. Power on your OMAP35x Development Kit. After Windows CE launches, select Start > Programs > Windows Explorer > SD_Card > GPIO_Win32.exe to run the application. Figure 3.5 shows the window prior to running the GPIO_Win32 application.

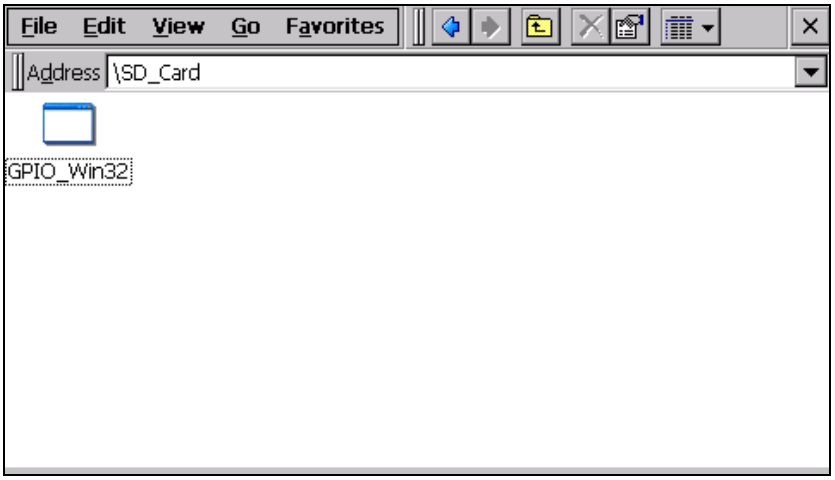

Figure 3.5: Windows Explorer (SD_Card files)

3. After running the GPIO_Win32 sample application, your LCD will display a red box with two buttons below the box (see Figure 3.6). This is considered the “OFF” state. By selecting the “ON” button on the touchscreen, the box will turn green.

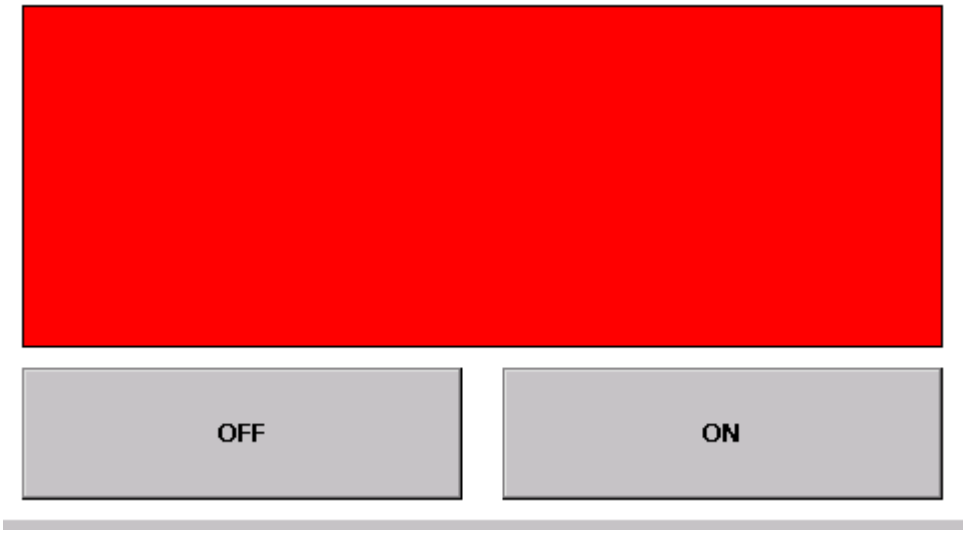

Figure 3.6: GPIO_Win32 Application Initial LED Off State Screen

This sample application was originally written to drive GPIO_133 (LED D3), so an illuminated LED D3 signifies “ON.” However, if you are monitoring the GPIO_111 signal, you will notice a low signal for “ON” and a high signal for “OFF.” This is because the LED does not come on until the signal is driven low.

3.2.3 Using GPIO_111 as Input

The information above described how to drive GPIO_133 and GPIO_111. For a reference on how to use the API calls for accessing GPIOs as inputs, see GPIOGetIrq() routing in the *Powerbutton.cpp* source code found in Logic PD's OMAP35x Windows CE 6.0 BSP (*.\PLATFORM\LPD_OMAP35X_SOM\SRC\CSP\OMAP\POWERBTN*).

To use GPIO_111 as an input, add the following line (that includes the *input_enable* parameter) to the *platform.c* file.

```
OUTREG16(&pConfig->CONTROL_PADCONF_CAM_XCLKB, (INPUT_ENABLE |
PULL_INACTIVE | MUX_MODE_4)); /*CAM_XCLKB*/
```

3.3 Configuring GPIO Signals in Linux

This section describes how to access GPIO signals on the OMAP35x processor using Logic PD’s OMAP35x Linux BSP version 2.0.0 or later.

1. First, mount *debugfs* to access the pin mux information.

```
OMAP-35x# mkdir -p /debug; mount -t debugfs debug /debug
```


2. We will be using GPIO_111 in this example. Locate the pin in the OMAP mux files by searching for the string *gpio_111* in the debug data provided by the kernel, then *grep* for the pin.

```
OMAP-35x# grep gpio_111 /debug/omap_mux/*
/debug/omap_mux/cam_xclkb:signals: cam_xclkb | NA | NA | NA | gpio_111
| NA | NA | safe_mode
```

From this output, we find that */debug/omap_mux/cam_xclkb* is the file associated with the GPIO_111 pin.

3. Verify what mode the pin is in.

```
OMAP-35x# cat /debug/omap_mux/cam_xclkb
name: cam_xclkb.cam_xclkb (0x4800212e/0x0fe = 0x0000), b b26, t NA
mode: OMAP_PIN_OUTPUT | OMAP_MUX_MODE0
signals: cam_xclkb | NA | NA | NA | gpio_111 | NA | NA | safe_mode
```

4. Since the pin is in *MODE0* (cam_xclkb), change it to MODE4 and then set GPIO_111 as an output.

```
OMAP-35x# echo 0x4 > /debug/omap_mux/cam_xclkb
```

5. Verify the pin is in the new mode.

```
OMAP-35x# cat /debug/omap_mux/cam_xclkb
name: cam_xclkb.gpio_111 (0x4800212e/0x0fe = 0x0004), b b26, t NA
mode: OMAP_PIN_OUTPUT | OMAP_MUX_MODE4
signals: cam_xclkb | NA | NA | NA | gpio_111 | NA | NA | safe_mode
```

6. Now we can use the gpiolib interface to manipulate the pin.

```
OMAP-35x# echo 111 > /sys/class/gpio/export
```

3.3.1 GPIO Output

Note that the steps above created a */sys/class/gpio/gpio111* directory and populated it with files to allow us to manipulate the pin.

1. Now we can set it as an output.

```
OMAP-35x# echo out > /sys/class/gpio/gpio111/direction
```

2. Set it high.

```
OMAP-35x# echo 1 > /sys/class/gpio/gpio111/value
```

3. Set it low.

```
OMAP-35x# echo 0 > /sys/class/gpio/gpio111/value
```


3.3.2 GPIO Input

The GPIO_111 pin can be configured as an input in the GPIO controller. This requires changing the pin mux value that was previously set. "Section 7.4.4" in the *OMAP35x TRM* provides details on how to set up the pin as an input with pull-up.

1. First, set the following bits: bit 8 (INPUTENABLE), bit 4 (PULLTYPESELECT) and bit 3 (PULLUDENABLE). Then set bits 2 through 0 representing MODE4 (GPIO). This will change the pin to *OMAP_PIN_INPUT_PULLUP* | *OMAP_MUX_MODE4.*

```
OMAP-35x# echo 0x11c > /debug/omap_mux/cam_xclkb
OMAP-35x# cat /debug/omap_mux/cam_xclkb
name: cam_xclkb.gpio_111 (0x4800212e/0x0fe = 0x011c), b b26, t NA
mode: OMAP_PIN_INPUT_PULLUP | OMAP_MUX_MODE4
signals: cam_xclkb | NA | NA | NA | gpio_111 | NA | NA | safe_mode
```

2. Next, reverse the direction.

```
OMAP-35x# echo in > /sys/class/gpio/gpio111/direction
```

3. Then check its value.

```
OMAP-35x# cat /sys/class/gpio/gpio111/value
1
```

Since the pin mux is set up with a pull-up, the value will be 1.

4. Ground the pin (J17.36 on the breakout board) and check the value again.

```
OMAP-35x# cat /sys/class/gpio/gpio111/value
0
```

5. Finally, free the pin.

```
OMAP-35x# echo 111 > /sys/class/gpio/unexport
```

Note that */sys/class/gpio/gpio111* is no longer there.

4 Summary

This application note has provided information about how to use GPIO signals on the OMAP35x SOM. For additional support, please contact Logic PD.[6]

[6] http://support.logicpd.com/TechnicalSupport/AskAQuestion.aspx

Appendix A: OMAP35x SOM-LV to Breakout Board Signal Mapping

Software engineers using the OMAP35x SOM-LV Development Kit can use the information in the table below to determine which pin on the expansion breakout board to monitor or drive when testing their software to access GPIO signals. Review the *OMAP35x SOM-LV Schematics* to determine which OMAP35x SOM-LV signal connects to the processor signal that is being used. Then the engineer can use this table to match the signal name/location on the OMAP35x SOM-LV with the pin location on the breakout board.

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J1.1	RFU	J17.64	MFP_B114
J1.2	RFU	J18.73	MFP_A114
J1.3	RFU	J18.70	MFP_B113
J1.4	RFU	J18.76	MFP_A113
J1.5	RFU	J17.63	MFP_B112
J1.6	RFU	J18.74	MFP_A112
J1.7	RFU	J18.69	MFP_B111
J1.8	RFU	J18.75	MFP_A111
J1.9	RFU	J18.72	MFP_B110
J1.10	RFU	J18.71	MFP_A110
J1.11	DGND	J16.1	DGND
J1.12	DGND	J17.80	DGND
J1.13	uP_nWAKEUP	J17.76	uP_nWAKEUP
J1.14	ETHER_TX+	J16.5	MFP_C2
J1.15	nSUSPEND	J15.78	nSUSPEND
J1.16	ETHER_TX-	J16.5	MFP_C2
J1.17	nSTANDBY	J15.77	nSTANDBY
J1.18	ETHER_RX+	J15.3	MFP_D2
J1.19	USB1_ID	J16.78	USB1_ID
J1.20	ETHER_RX-	J16.13	MFP_D18
J1.21	USB1_VBUS	J16.77	USB1_VBUS
J1.22	ACT_nLNK_LED/LAN_LED2	J15.80	LAN_LED2
J1.23	USB1_nOC	J15.76	USB1_nOC
J1.24	SPD_LED_n100M_10M/LAN_LED1	J18.78	LAN_LED1
J1.25	USB1_PWR_nEN	J15.75	USB1_PWR_nEN
J1.26	VREF_ETHERNET (3.3V_A)	J17.78	VREF_ETHERNET
J1.27	USB1_D+	J16.6	MFP_C1
J1.28	RFU	J18.77	uP_AUX_CLK
J1.29	USB1_D-	J16.6	MFP_C1
J1.30	RFU	J17.77	MFP_A101
J1.31	DGND	J18.1	DGND
J1.32	DGND	J16.2	DGND
J1.33	USB2_D+	J16.57	MFP_D1
J1.34	uP_GPIO_7	J16.76	uP_GPIO_7
J1.35	USB2_D-	J16.57	MFP_D1

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J1.36	uP_GPIO_6	J16.75	uP_GPIO_6
J1.37	USB2_nOC	J15.73	USB2_nOC
J1.38	uP_GPIO_5	J15.74	uP_GPIO_5
J1.39	USB2_PWR_nEN	J16.74	USB2_PWR_nEN
J1.40	uP_D0	J9.15	UP_D0
J1.41	RFU		
J1.42	uP_D1	J9.13	UP_D1
J1.43	RFU		
J1.44	uP_D2	J9.11	UP_D2
J1.45	RFU	J16.73	USB3_VBUS
J1.46	uP_D3	J9.9	UP_D3
J1.47	RFU	J15.72	USB3_PWR_nEN
J1.48	uP_D4	J9.7	UP_D4
J1.49	3.3V_nEN (DGND)	J15.71	3.3V_nEN
J1.50	uP_D5	J9.5	UP_D5
J1.51	DGND	J18.2	DGND
J1.52	DGND	J18.79	DGND
J1.53	A0 (DGND)	J11.15	UP_A0
J1.54	uP_D6	J9.3	UP_D6
J1.55	A1 (uP_LA1)	J11.13	UP_A1
J1.56	uP_D7	J9.1	UP_D7
J1.57	A2 (uP_LA2)	J11.11	UP_A2
J1.58	uP_D8	J7.15	UP_D8
J1.59	A3 (uP_LA3)	J11.9	UP_A3
J1.60	uP_D9	J7.13	UP_D9
J1.61	A4 (uP_LA4)	J11.7	UP_A4
J1.62	uP_D10	J7.11	UP_D10
J1.63	A5 (uP_LA5)	J11.5	UP_A5
J1.64	uP_D11	J7.9	UP_D11
J1.65	A6 (uP_LA6)	J11.3	UP_A6
J1.66	uP_D12	J7.7	UP_D12
J1.67	A7 (uP_LA7)	J11.1	UP_A7
J1.68	uP_D13	J7.5	UP_D13
J1.69	A8 (uP_LA8)	J10.15	UP_A8
J1.70	uP_D14	J7.3	UP_D14
J1.71	DGND	J18.80	DGND
J1.72	DGND	J19.31	DGND
J1.73	A9 (uP_LA9)	J10.13	UP_A9
J1.74	uP_D15	J7.1	UP_D15
J1.75	A10 (uP_LA10)	J10.11	UP_A10
J1.76	D16 (RFU)	J5.15	UP_D16
J1.77	A11 (uP_LA11)	J10.9	UP_A11
J1.78	D17 (RFU)	J5.13	UP_D17

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J1.79	A12 (uP_LA12)	J10.7	UP_A12
J1.80	D18 (RFU)	J5.11	UP_D18
J1.81	A13 (uP_LA13)	J10.5	UP_A13
J1.82	D19 (RFU)	J5.9	UP_D19
J1.83	A14 (uP_LA14)	J10.3	UP_A14
J1.84	D20 (RFU)	J5.7	UP_D20
J1.85	A15 (uP_LA15)	J10.1	UP_A15
J1.86	D21 (RFU)	J5.5	UP_D21
J1.87	A16 (uP_LA16)	J8.15	UP_A16
J1.88	D22 (RFU)	J5.3	UP_D22
J1.89	A17 (uP_A1)	J8.13	UP_A17
J1.90	D23 (RFU)	J5.1	UP_D23
J1.91	DGND	J19.32	DGND
J1.92	DGND	J3.10	DGND
J1.93	A18 (uP_A2)	J8.11	UP_A18
J1.94	D24 (RFU)	J3.15	UP_D24
J1.95	A19 (uP_A3)	J8.9	UP_A19
J1.96	D25 (RFU)	J3.13	UP_D25
J1.97	A20 (uP_A4)	J8.7	UP_A20
J1.98	D26 (RFU)	J3.11	UP_D26
J1.99	A21 (uP_A5)	J8.5	UP_A21
J1.100	D27 (RFU)	J3.9	UP_D27
J1.101	A22 (uP_A6)	J8.3	UP_A22
J1.102	D28 (RFU)	J3.7	UP_D28
J1.103	A23 (uP_A7)	J8.1	UP_A23
J1.104	D29 (RFU)	J3.5	UP_D29
J1.105	A24 (uP_A8)	J6.15	UP_A24
J1.106	D30 (RFU)	J3.3	UP_D30
J1.107	A25 (uP_A9)	J6.13	UP_A25
J1.108	D31 (RFU)	J3.1	UP_D31
J1.109	uP_nWAIT	J4.15	uP_nWAIT
J1.110	VREF_DATA_BUS (VIO_1V8)	J18.68	VREF_DATA_BUS
J1.111	DGND	J3.12	DGND
J1.112	DGND	J3.14	DGND
J1.113	uP_nIRQD (CSI_D11)	J18.59	uP_nIRQD
J1.114	RFU	J17.62	CF_nCE
J1.115	uP_nIRQC	J17.53	uP_nIRQC
J1.116	RFU	J17.65	CF_nWE
J1.117	uP_nIRQB	J18.64	uP_nIRQB
J1.118	RFU	J17.61	CF_nOE
J1.119	uP_nIRQA	J17.54	uP_nIRQA
J1.120	RFU	J18.67	nCHRDY
J1.121	RFU	J6.7	BUFF_nOE_DATA

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J1.122	uP_UARTC_CTS	J17.48	uP_UARTC_CTS
J1.123	BUFF_DIR_DATA	J6.5	BUFF_DIR_DATA
J1.124	uP_UARTC_RTS	J17.47	uP_UARTC_RTS
J1.125	uP_nOE	J6.3	uP_nOE
J1.126	uP_UARTC_RX	J17.46	uP_UARTC_RX
J1.127	uP_nWE	J6.1	uP_RnW
J1.128	uP_UARTC_TX	J17.43	uP_UARTC_TX
J1.129	DGND	J3.16	DGND
J1.130	DGND	J3.2	DGND
J1.131	uP_BUS_CLK	J4.13	uP_BUS_CLK
J1.132	uP_UARTB_RX	J17.31	uP_UARTB_RX/IRDA_RX
J1.133	uP_DREQ0	J17.45	uP_DREQ0
J1.134	uP_UARTB_TX	J17.30	uP_UARTB_TX/IRDA_TX
J1.135	RFU	J17.44	RFU
J1.136	uP_UARTB_CTS	J17.29	uP_UARTB_CTS
J1.137	uP_nBE0	J4.11	uP_nBLE0
J1.138	uP_UARTB_RTS	J17.28	uP_UARTB_RTS
J1.139	uP_nBE1	J4.9	uP_nBLE1
J1.140	uP_GPO_4	J17.37	uP_GPIO_4
J1.141	uP_nCS_B_EXT	J17.35	uP_nCS3
J1.142	GPIO_111	J17.36	GPIO_111
J1.143	uP_nCS_A_EXT	J17.34	uP_nCS1
J1.144	VREF_I2C2 (VIO_1V8)	J17.17	VREF_I2C1
J1.145	FAST_nCS (uP_nCS_A_EXT)	J17.33	SLOW_nCS
J1.146	uP_I2C2_SDA	J17.16	I2C1_DATA
J1.147	FAST_nCS (uP_nCS_A_EXT)	J17.32	FAST_nCS
J1.148	uP_I2C2_SCL	J17.15	I2C1_CLK
J1.149	DGND	J3.4	DGND
J1.150	DGND	J3.6	DGND
J1.151	RFU	J18.53	LCD_SPL
J1.152	VREF_UARTA (VIO_1V8)	J17.14	VREF_UARTA
J1.153	LCD_DON (ICT_JTAG_TMS)	J18.52	LCD_DON
J1.154	uP_UARTA_DSR	J17.13	uP_UARTA_DSR
J1.155	RFU	J18.51	LCD_CLS
J1.156	uP_UARTA_DTR	J17.11	uP_UARTA_DTR
J1.157	RFU	J18.50	LCD_SPS
J1.158	uP_UARTA_RX	J17.12	uP_UARTA_RX
J1.159	RFU	J18.49	LCD_HRLP
J1.160	uP_UARTA_TX	J17.9	uP_UARTA_TX
J1.161	LCD_PANEL_PWR	J18.48	LCD_PANEL_PWR
J1.162	uP_UARTA_CTS	J17.8	uP_UARTA_CTS
J1.163	LCD_BACKLIGHT_PWR	J18.47	LCD_BACKLIGHT_PWR
J1.164	uP_UARTA_RTS	J17.10	uP_UARTA_RTS

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J1.165	LCD_HSYNC	J18.46	LCD_HSYNC
J1.166	uP_GPIO_2	J17.5	uP_GPIO_2
J1.167	LCD_VSYNC	J18.45	LCD_VSYNC
J1.168	PWM0	J17.7	PWM0
J1.169	DGND	J16.79	DGND
J1.170	DGND	J16.80	DGND
J1.171	LCD_DCLK	J18.42	LCD_DCLK
J1.172	BACKUP_BATT	J19.20	3.3V_uP_BATT
J1.173	RFU	J18.41	LCD_REV
J1.174	5V	J19.10	5V
J1.175	LCD_MDISP	J18.40	LCD_MDISP
J1.176	5V	J19.10	5V
J1.177	RFU	J18.39	LCD_PSAVE
J1.178	5V	J19.10	5V
J1.179	RFU	J18.38	LCD_CLK_RETURN
J1.180	3.3V	J16.3	3.3V
J1.181	RFU	J18.37	LCD_MOD
J1.182	3.3V	J19.19	3.3V
J1.183	LCD_VREF (VPLL2)	J18.54	VREF_LCD
J1.184	3.3V	J20.7	3.3V
J1.185	R1 (LCD_D11)	J18.28	LCD_R1
J1.186	TOUCH_LEFT	J19.17	TOUCH_LEFT
J1.187	R2 (LCD_D12)	J18.27	LCD_R2
J1.188	TOUCH_RIGHT	J19.15	TOUCH_RIGHT
J1.189	DGND	J15.1	DGND
J1.190	DGND	J15.2	DGND
J1.191	R3 (LCD_D13)	J18.26	LCD_R3
J1.192	TOUCH_BOTTOM	J19.13	TOUCH_BOTTOM
J1.193	R4 (LCD_D14)	J18.25	LCD_R4
J1.194	TOUCH_TOP	J19.11	TOUCH_TOP
J1.195	R5 (LCD_D15)	J18.20	LCD_R5
J1.196	A/D4	J19.7	A/D4
J1.197	G0 (LCD_D5)	J18.19	LCD_G0
J1.198	A/D3	J19.5	A/D3
J1.199	G1 (LCD_D6)	J18.18	LCD_G1
J1.200	A/D2	J19.3	A/D2
J1.201	G2 (LCD_D7)	J18.17	LCD_G2
J1.202	A/D1	J19.1	A/D1
J1.203	G3 (LCD_D8)	J18.24	LCD_G3
J1.204	MAIN_BATTERY	J19.9	MAIN_BATTERY
J1.205	G4 (LCD_D9)	J18.23	LCD_G4
J1.206	MAIN_BATTERY	J19.9	MAIN_BATTERY
J1.207	G5 (LCD_D10)	J18.22	LCD_G5

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J1.208	MAIN_BATTERY	J19.9	MAIN_BATTERY
J1.209	DGND	J15.79	DGND
J1.210	DGND	J17.1	DGND
J1.211	B1 (LCD_D0)	J18.21	LCD_B1
J1.212	MAIN_BATTERY	J19.9	MAIN_BATTERY
J1.213	B2 (LCD_D1)	J18.16	LCD_B2
J1.214	MAIN_BATTERY	J19.9	MAIN_BATTERY
J1.215	B3 (LCD_D2)	J18.15	LCD_B3
J1.216	uP_GPIO_1	J18.4	uP_GPIO_1
J1.217	B4 (LCD_D3)	J18.14	LCD_B4
J1.218	GPIO_133	J17.4	GPIO_133
J1.219	B5 (LCD_D4)	J18.13	LCD_B5
J1.220	uP_SPI_CS1	J18.3	uP_SPI_CS1
J1.221	ONE_WIRE (BATT_LINE)	J17.6	BATT_LINE
J1.222	uP_SPI_CS0	J4.7	uP_SPI_CS0
J1.223	uP_SW_nRESET (SYS_nRESWARM)	J17.3	uP_SW_nRESET
J1.224	uP_SPI_SOMI	J4.5	uP_SPI_RX
J1.225	RESET_nOUT (SYS_nRESWARM)	J6.11	RESET_nOUT
J1.226	uP_SPI_SIMO	J4.3	uP_SPI_TX
J1.227	MSTR_nRST	J6.9	MSTR_nRST
J1.228	uP_SPI_SCLK	J4.1	uP_SPI_SCLK
J1.229	DGND	J17.2	DGND
J1.230	DGND	J17.79	DGND
J1.231	VMMC2	J18.10	MFP_B5
J1.232	TOUCH_nIRQ	J18.7	MFP_A5
J1.233	SPI_MOSI	J18.12	MFP_B4
J1.234	RFU	J18.6	MFP_A4
J1.235	SPI_MISO	J18.9	MFP_B3
J1.236	RFU	J18.5	MFP_A3
J1.237	RFU	J18.11	MFP_B2
J1.238	RFU	J18.44	MFP_A2
J1.239	SPI_CLK	J18.8	MFP_B1
J1.240	SPI_CS	J18.43	MFP_A1
J2.1	RFU	J16.58	MFP_D114
J2.2	RFU	J17.73	MFP_C114
J2.3	RFU	J15.57	MFP_D113
J2.4	RFU	J17.72	MFP_C113
J2.5	RFU	J15.58	MFP_D112
J2.6	RFU	J17.74	MFP_C112
J2.7	WLAN_nIRQ	J16.55	MFP_D111
J2.8	RFU	J17.71	uP_nBLE3
J2.9	ICT_TEST_MODE	J16.56	MFP_D110
J2.10	uP_CLKOUT2_26MHz	J17.75	uP_nBLE2

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J2.11	DGND	J3.8	DGND
J2.12	DGND	J7.12	DGND
J2.13	PCC_POWER_nEN (SIM0_VEN)	J15.55	MFP_D109
J2.14	PCC_nOE (uP_nOE)	J17.70	PCC_nOE
J2.15	PCC_PCMCIA_nEN (SIM0_VEN)	J15.56	MFP_D108
J2.16	RFU	J16.72	PCC_RDYA
J2.17	HSUSB1_D7	J16.53	MFP_D107
J2.18	uP_PCC_nWAIT	J16.71	PCC_nWAIT
J2.19	HSUSB1_D6	J16.54	MFP_D106
J2.20	RFU	J15.70	PCC_BVD2
J2.21	HSUSB1_D5	J15.53	MFP_D105
J2.22	RFU	J15.69	PCC_BVD1
J2.23	HSUSB1_D4	J15.54	MFP_D104
J2.24	uP_PCC_CD2 (uP_PCC_CD1)	J16.70	PCC_CD2
J2.25	HSUSB1_D3	J16.51	MFP_D103
J2.26	uP_PCC_CD1	J16.69	PCC_CD1
J2.27	HSUSB1_D2	J16.52	MFP_D102
J2.28	RFU	J15.68	PCC_VS1
J2.29	HSUSB1_D1	J15.51	MFP_D101
J2.30	RFU	J15.67	PCC_VS2
J2.31	DGND	J7.14	DGND
J2.32	DGND	J5.10	DGND
J2.33	HSUSB1_CLK	J15.52	MFP_D99
J2.34	uP_PCC_RESET	J16.68	PCC_RESET
J2.35	HSUSB1_NXT	J16.49	MFP_D98
J2.36	PCC_nDRV (uP_nCS3)	J16.67	PCC_nDRV
J2.37	HSUSB1_STP	J16.50	MFP_D97
J2.38	PCC_nIOWR (VIO_1V8)	J15.66	PCC_nIOWR
J2.39	HSUSB1_DIR	J15.49	MFP_D96
J2.40	PCC_nWE (uP_nWE)	J15.65	PCC_nWE
J2.41	HSUSB1_D0	J15.50	MFP_D95
J2.42	PCC_nIORD (VIO_1V8)	J16.66	PCC_nIORD
J2.43	HSUSB2_STP	J16.47	MFP_D94
J2.44	PCC_REG (uP_LA12)	J16.65	PCC_REG
J2.45	EMU3	J16.48	MFP_D93
J2.46	RFU	J15.64	uP_PCC_nIOIS16
J2.47	HSUSB2_D0	J15.47	MFP_D92
J2.48	PCC_nCE1A (uP_nCS3)	J15.63	PCC_nCE1A
J2.49	MCSPI_CS1 (HSUSB2_D3)	J15.48	MFP_D91
J2.50	PCC_nCE2A (uP_nCS3)	J16.64	PCC_nCE2A
J2.51	DGND	J7.16	DGND
J2.52	DGND	J7.2	DGND
J2.53	MCSPI2_CS0 (HSUSB2_D6)	J16.45	MFP_D89

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J2.54	VREF_PCMCIA (VIO_1V8)	J16.63	VREF_PCMCIA
J2.55	MCSPI2_SOMI (HSUSB2_D5)	J16.46	MFP_D88
J2.56	A26 (uP_A10)	J15.62	MFP_C88
J2.57	MCSPI2_SIMO (HSUSB2_D4)	J15.45	MFP_D87
J2.58	USB4_nOC	J15.61	USB4_nOC
J2.59	MCSPI2_CLK (HSUSB2_D7)	J15.46	MFP_D86
J2.60	USB4_PWR_nEN	J16.62	USB4_PWR_nEN
J2.61	RFU	J16.43	MFP_D85
J2.62	USB4_D-		
J2.63	RFU	J16.44	MFP_D84
J2.64	USB4_D-		
J2.65	RFU	J15.43	MFP_D83
J2.66	RFU	J16.61	USB5_VBUS
J2.67	RFU	J15.44	MFP_D82
J2.68	RFU	J15.60	USB5_ID
J2.69	RFU	J16.41	MFP_D81
J2.70	USB5_nOC	J15.59	USB5_nOC
J2.71	DGND	J7.4	DGND
J2.72	DGND	J7.6	DGND
J2.73	RFU	J16.42	MFP_D79
J2.74	USB5_D+		
J2.75	VIBRA_M	J15.41	MFP_D78
J2.76	USB5_D-		
J2.77	VIBRA_P	J15.42	MFP_D77
J2.78	USB5_PWR_nEN	J18.66	USB5_PWR_nEN
J2.79	START_ADC	J16.39	MFP_D76
J2.80	VREF_MMC/SD1 (VMMC1)	J18.65	VREF_SD1/MMC
J2.81	RF_LED0	J16.40	MFP_D75
J2.82	SD1_DATA3	J17.69	SD1_DATA3
J2.83	RF_LED1	J15.39	MFP_D74
J2.84	SD1_DATA2	J17.68	SD1_DATA2
J2.85	uP_nWP	J15.40	MFP_D73
J2.86	SD1_DATA1	J17.67	SD1_DATA1
J2.87	uP_nADV_ALE	J16.37	MFP_D72
J2.88	SD1_DATA0	J17.66	SD1_DATA0
J2.89	RFID_EN	J16.38	MFP_D71
J2.90	SD1_CMD	J17.60	SD1_CMD
J2.91	DGND	J7.8	DGND
J2.92	DGND	J9.10	DGND
J2.93	KEY_COL7	J15.37	MFP_D69
J2.94	SD1_CLK	J17.59	SD1_CLK
J2.95	KEY_COL6	J15.38	MFP_D68
J2.96	VREF_I2C3 (VIO_1V8)	J17.58	VREF_I2C2

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J2.97	KEY_COL5	J16.35	MFP_D67
J2.98	uP_I2C3_SCL	J17.57	I2C2_CLK
J2.99	KEY_COL4	J16.36	MFP_D66
J2.100	uP_I2C3_SDA	J18.60	I2C2_DATA
J2.101	KEY_COL3	J15.35	MFP_D65
J2.102	RFU	J17.56	uP_TEST1
J2.103	KEY_COL2	J15.36	MFP_D64
J2.104	RFU	J17.55	uP_TEST2
J2.105	KEY_COL1	J16.33	MFP_D63
J2.106	RFU	J18.61	uP_DE
J2.107	KEY_COL0	J16.34	MFP_D62
J2.108	uP_TMS	J18.62	uP_TMS
J2.109	KEY_ROW7	J15.33	MFP_D61
J2.110	uP_TCK	J18.63	uP_TCK
J2.111	DGND	J9.12	DGND
J2.112	DGND	J9.14	DGND
J2.113	KEY_ROW6	J15.34	MFP_D59
J2.114	uP_TDO	J18.58	uP_TDO
J2.115	KEY_ROW5	J16.31	MFP_D58
J2.116	uP_nTRST	J17.52	uP_nTRST
J2.117	KEY_ROW4	J16.32	MFP_D57
J2.118	uP_TDI	J17.51	uP_TDI
J2.119	KEY_ROW3	J15.31	MFP_D56
J2.120	uP_RTCK	J18.57	uP_RTCK
J2.121	KEY_ROW2	J15.32	MFP_D55
J2.122	VREF_JTAG (VIO_1V8)	J17.50	VREF_JTAG
J2.123	KEY_ROW1	J16.29	MFP_D54
J2.124	SIM0_VEN	J17.49	SIM0_nDETECT
J2.125	KEY_ROW0	J16.30	MFP_D53
J2.126	SIM0_nDETECT	J18.56	SIM0_VEN
J2.127	CSI_HSYNC	J15.29	CSI_HSYNC
J2.128	SIM0_CLK	J18.55	SIM0_CLK
J2.129	DGND	J9.16	DGND
J2.130	DGND	J9.2	DGND
J2.131	CSI_VSYNC	J15.30	CSI_VSYNC
J2.132	SIM0_IO/TX	J17.42	SIM0_IO/TX
J2.133	CSI_D0	J16.27	CSI_D0
J2.134	RFU	J17.41	SIM0_RX
J2.135	CSI_D1	J16.28	CSI_D1
J2.136	SIM0_nRESET	J17.40	SIM0_nRESET
J2.137	CSI_D2	J15.27	CSI_D2
J2.138	VREF_SIM (VSIM)	J17.39	SIM0_VCC
J2.139	CSI_D3	J15.28	CSI_D3

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J2.140	RFU	J17.38	MFP_C46
J2.141	CSI_D4	J16.25	CSI_D4
J2.142	ICT_JTAG_TDO	J20.3	CPLD_TDO
J2.143	CSI_D5	J16.26	CSI_D5
J2.144	ICT_JTAG_TMS	J20.5	CPLD_TMS
J2.145	CSI_D6	J15.25	CSI_D6
J2.146	ICT_JTAG_TDI	J20.9	CPLD_TDI
J2.147	CSI_D7	J15.26	CSI_D7
J2.148	ICT_JTAG_CLK	J20.1	CPLD_TCK
J2.149	DGND	J9.4	DGND
J2.150	DGND	J9.6	DGND
J2.151	CSI_D8	J16.23	CSI_D8
J2.152	uP_GPIO_2	J17.27	MFP_C40
J2.153	CSI_D9	J16.24	CSI_D9
J2.154	uP_GPIO_1	J17.26	MFP_C39
J2.155	CSI_D10	J15.23	CSI_D10
J2.156	BT_PCM_DX	J17.25	MFP_C38
J2.157	CSI_D11	J15.24	CSI_D11
J2.158	BT_PCM_DR	J17.24	MFP_C37
J2.159	RFU	J16.21	CSI_D12
J2.160	BT_PCM_VFS	J17.23	MFP_C36
J2.161	RFU	J16.22	CSI_D13
J2.162	PCM_DX	J17.22	MFP_C35
J2.163	RFU	J15.21	CSI_D14
J2.164	PCM_DR	J17.21	MFP_C34
J2.165	RFU	J15.22	CSI_D15
J2.166	BT_PCM_CLK	J17.18	MFP_C33
J2.167	CSI_MCLK	J16.19	CSI_MCLK
J2.168	EXT_BOOT_nSELECT	J17.20	EXT_BOOT_nSELECT
J2.169	DGND	J5.12	DGND
J2.170	DGND	J5.14	DGND
J2.171	CSI_PCLK	J16.20	CSI_PCLK
J2.172	BOOT_nCS	J17.19	BOOT_nCS
J2.173	VIO_1V8	J15.19	VREF_CSI
J2.174	LCD_D23	J18.32	LCD_G7
J2.175	VAUX3	J15.20	MFP_D28
J2.176	LCD_D22	J18.31	LCD_G6
J2.177	TWL_CLK256FS	J16.17	MFP_D27
J2.178	LCD_D21	J18.30	LCD_B7
J2.179	RFU	J16.18	MFP_D26
J2.180	LCD_D20	J18.29	LCD_B6
J2.181	CSI1_DY1	J15.17	MFP_D25
J2.182	LCD_D19	J18.36	LCD_B0

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J2.183	CSI1_DX1	J15.18	MFP_D24
J2.184	LCD_D18	J18.35	LCD_R7
J2.185	CSI1_DY0	J16.15	MFP_D23
J2.186	LCD_D17	J18.34	LCD_R6
J2.187	CSI1_DX0	J16.16	MFP_D22
J2.188	LCD_D16	J18.33	LCD_R0
J2.189	DGND	J5.16	DGND
J2.190	DGND	J5.2	DGND
J2.191	MCSPI1_SOMI	J15.15	MFP_D20
J2.192	TV_OUT2	J19.29	MFP_C20
J2.193	T2_REGEN	J15.16	MFP_D19
J2.194	TV_OUT1	J19.30	MFP_C19
J2.195	ADCIN6	J16.13	MFP_D18
J2.196	ADCIN2	J19.28	MFP_C18
J2.197	WLAN_MMC3_DATA3	J16.14	MFP_D17
J2.198	ADCIN1	J19.27	MFP_C17
J2.199	WLAN_MMC3_DATA2	J15.14	MFP_D16
J2.200	ADCIN0	J19.26	MFP_C16
J2.201	WLAN_MMC3_DATA1	J15.13	MFP_D15
J2.202	IHF_RIGHT_M	J19.25	MFP_C15
J2.203	WLAN_MMC3_DATA0	J15.11	MFP_D14
J2.204	IHF_RIGHT_P	J19.24	MFP_C14
J2.205	WLAN_MMC3_CMD	J15.12	MFP_D13
J2.206	IHF_LEFT_M	J19.23	MFP_C13
J2.207	WLAN_MMC3_CLK	J16.12	MFP_D12
J2.208	IHF_LEFT_P	J19.22	MFP_C12
J2.209	DGND	J5.4	DGND
J2.210	DGND	J5.6	DGND
J2.211	MCSPI1_CLK	J16.11	MFP_D10
J2.212	MIC_IN	J19.21	MIC_IN
J2.213	MCSPI1_SIMO	J15.10	MFP_D9
J2.214	MIC_SUB_M	J19.18	MIC_INR
J2.215	MCSPI1_CS0	J15.9	MFP_D8
J2.216	MIC_SUB_P	J19.16	MIC_INL
J2.217	MICBIAS2	J15.7	MFP_D7
J2.218	MIC_MAIN_M	J19.14	HP_OUTL
J2.219	MICBIAS1	J15.8	MFP_D6
J2.220	MIC_MAIN_P	J19.12	HP_OUTR
J2.221	MCBSP2_CLKX	J16.10	I2S/AC97_CLK
J2.222	CODEC_INL	J19.8	CODEC_INL
J2.223	MCBSP2_FSX	J16.9	I2S/AC97_FRAME
J2.224	CODEC_INR	J19.6	CODEC_INR
J2.225	MCBSP2_DR	J16.8	I2S/AC97_RX

SOM-LV Pin#	SOM-LV Net Name	Breakout Board Pin#	Breakout Board Net Name
J2.226	CODEC_OUTL	J19.4	CODEC_OUTL
J2.227	MCBSP2_DX	J16.7	I2S/AC97_TX
J2.228	CODEC_OUTR	J19.2	CODEC_OUTR
J2.229	DGND	J5.8	DGND
J2.230	DGND	J7.10	DGND
J2.231	T2_CLKREQ	J15.6	MFP_D5
J2.232	BT_IRQ	J16.59	MFP_C5
J2.233	uP_CLKOUT1_26MHz	J16.60	MFP_C4
J2.234	TWL_32K_CLK_OUT	J16.60	MFP_C4
J2.235	RFU	J15.20	MFP_D28
J2.236	RFU	J15.5	MFP_D4
J2.237	VDD2_CORE	J16.4	MFP_C3
J2.238	VDD1_CORE	J16.4	MFP_C3
J2.239	NOR_nCS	J16.17	MFP_D27
J2.240	TWL_CLKEN	J15.4	MFP_D3

Appendix B: Configuring a TPS65950 PMIC Signal as a GPIO

Configuring GPIOs on the TPS65950 is a bit more complex than configuring the OMAP35x processor GPIOs. The TPS65950 requires access through the I2C and then access to the GPIO control registers within the TPS65950. LogicLoader version 2.4.12 added support for accessing registers through the I2C bus on the TPS65950 to simplify this task. The example below that shows how to enable and drive LCD_DON high can easily be modified to access any other GPIO or register within the TPS65950.

The following script programs the TPS65950 GPIO.1 to output high or low. This signal connects to pin J1.153 on the OMAP35x SOM-LV, signal ICT_JTAG_TMS (LCD_DON). LCD_DON is connected to J18.52 on the breakout board. **NOTE:** The TPS65950 GPIO.1 signal does not go external of the OMAP35x Torpedo SOM.

```
#TPS95650 is attached to I2C1
#I2C1 base address is 0x48070000
#Bitrate is 2.6 MHz
#High speed mode
#Procedure for setting LCD_DON to high

#Set GPIO_ON(bit 2), clear GPIO1CD2(bit1) in GPIO_CTRL, register 0xAA,
address_group
# 0x49, data 0x4
losh> w /b 0x004900AA 0x04 /dev/pm0

#Set GPIO1OUT to HIGH in SETGPIODATAOUT1, register 0xA4, address_group
0x49, data 0x2
losh> w /b 0x004900A4 0x02 /dev/pm0

#Set GPIO1DIR to HIGH in GPIODATADIR1, register 0x9B, address_group
0x49, data 0x2
losh> w /b 0x0049009b 0x02 /dev/pm0
```

To change the script so it sets LCD_DON low, change the write-to *SETGPIODATAOUT1* to *CLEARGPIODATAOUT1*, as shown below.

```
#Set GPIO1OUT to HIGH in CLEARGPIODATAOUT1, register 0xA1,
address_group 0x49, data 0x2
losh> w /b 0x004900a1 0x02 /dev/pm0
```

If you need to read a TPS65950 GPIO as an input within LogicLoader, contact Logic PD for assistance with creating a suitable script.

Appendix C: Enabling VPLL2 LogicLoader I2C Commands

The following commands in LogicLoader will enable VPLL2 to output 1.8V, thus making GPIOs that are powered by VPLL2 accessible.

```
losh> x /b 0x004b008E 1 /dev/pm0      # read VPLL2_DEV_GRP silicon
register 0x8E of the PMIC chip device ID 0x4b (address_group)
losh> x /b 0x004b008E 1 /dev/pm0     # read VPLL2_DEDICATED silicon
register 0x91 of the PMIC chip device ID 0x4b (address_group)
losh> w /b 0x004b008E 0x2e /dev/pm0   # write 0x2e (data) to
VPLL2_DEV_GRP silicon register 0x8E of the PMIC chip device ID 0x4b
(address_group)
losh> w /b 0x004b0091 0x5 /dev/pm0    # write 0x5 (data) to
VPLL2_DEDICATED silicon register 0x91 of the PMIC chip device ID 0x4b
(address_group)
```

