Selecting and Using GPIO Signals on DM3730/AM3703 SOMs

Application Note 527

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Abstract

This document provides information on how to select, access, and test general purpose input/output (GPIO) signals on the DM3730/AM3703 SOM-LV, DM3730/AM3703 Torpedo SOM, and DM3730/AM3703 Torpedo + Wireless SOM.

Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	RAH	-Initial release	NJK	03/20/12
B	SO	-Throughout: Added language for AM3703 configuration of the Torpedo + Wireless SOM	SO	06/14/12
C	BSB	-Section 3: Added requirement to populate R197 and remove R198 on Torpedo Launcher 3 Baseboard; -Added Section 3.4 to point users to available documentation about how to configure GPIO signals in Android	SWE, SO	08/02/13

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1 Introduction

This document provides information on how to select, access, and test general purpose input/output (GPIO) signals on the DM3730/AM3703 SOM-LV, DM3730/AM3703 Torpedo SOM, and DM3730/AM3703 Torpedo + Wireless SOM.

1.1 Nomenclature, Notices, and Conventions Used in This Document

- This document covers the DM3730/AM3703 SOM-LV, DM3730/AM3703 Torpedo SOM, and DM3730/AM3703 Torpedo + Wireless SOM. Use of "DM3730/AM3703 SOM" suggests text that applies to all three platforms; information specific to one platform will call out the precise name.
- Use of "DM3730 Development Kit" suggests text that applies to both the DM3730 SOM-LV Development Kit and DM3730 Torpedo SOM Development Kit; information specific to one development kit will call out the precise name.
- When referring to specific pins for signals, the connector/processor reference designator is called out first and then the pin number. For example, J1.115 represents pin 115 on connector J1; similarly, U4.D25 represents pin D25 on the DM3730 processor at reference designator U4.

2 Selecting GPIO Signals

Many signals on the DM3730/AM3703 SOM can be used as GPIOs in an embedded system design. When designating a signal as a GPIO, it is important to verify that designation will not cause conflicts when trying to use other devices with the DM3730/AM3703 SOM. This section explains how to avoid those potential conflicts; however, it is the responsibility of the system engineer to confirm that the chosen GPIO signal does not conflict with the system design.

Voltage levels for all the signals recommended in this section are 1.8V; each signal is capable of being used as either an input or an output.

2.1 DM3730/AM3703 SOM-LV GPIO Selection

Table 2.1 shows a list of available GPIO signals after being filtered using the following criteria:

- The *DM3730/AM3703 SOM-LV Schematic*[1] (PN 1017750A) was used in creating this document. In the unlikely event that an I/O is changed on a future revision of the schematic, that change will need to be evaluated to determine its impact, if any, on Table 2.1.
- Signals were removed from the list if they touch more than two nodes within the schematic net list. All recommended signals connect directly between the DM3730 processor (U4) and one of the SOM-LV connectors (J1 or J2).
- GPIO_133 (uP_GPIO_0) and GPIO_11 (uP_GPIO_1) were removed since they are designated as output from LogicLoader; however, they can be used for testing purposes as demonstrated in this document.
- GPIO_151 (uP_UARTA_RX) and GPIO_148 (uP_UARTA_TX) were removed since they are used for the debug serial port from LogicLoader.
- GPIO_165 (uP_UARTB_RX) and GPIO_166 (uP_UARTB_TX) were removed since they are part of the default boot operation of the DM3730 processor and may toggle at boot time.
- GPIO_60 (GPMC_nBE0_CLE) was removed since it connects to the Package on-Package (PoP) NAND flash memory.

[1] http://support.logicpd.com/downloads/1474/

- The GPIO signals in Table 2.1 are all available on the DM3730 processor. Additional GPIO signals may be available through the TPS65950 Power Management IC (PMIC); please see Appendix A for more information.

Be sure to consider the following items when selecting a GPIO for your embedded system:

- Verify available GPIOs based on the specific SOM-LV schematic and system baseboard used in the final design.
- This list is based on the standard DM3730 SOM-LV configuration (SOMDM3730-10-2782IFCR-A) and does not take into account signals that may become available when certain components are not populated, such as Bluetooth and Wi-Fi.
- Verify the voltage levels of each GPIO signal are compatible with the receiving signal.
- Verify availability for reset configuration and internal pull-ups/pull-downs using "Table 13-84: CONTROL_PADCONF_CAPABILITIES" in the Texas Instruments (TI) *AM/DM37x Multimedia Device Technical Reference Manual (TRM)*.[2]
- Verify the GPIO you select is used in only one location in the pin mux of the DM3730 processor; some GPIO signals can be found in multiple locations of the pin mux. These signals include but are not limited to: GPIO_120, GPIO_121, GPIO_122, GPIO_124, GPIO_125, GPIO_126, GPIO_130, and GPIO_131.

Table 2.1: DM3730/AM3703 SOM-LV Filtered GPIOs

J1/J2 Connection	U4 Connection	SOM-LV Signal	uP Signal	Notes
J1.15	U4.W21	nSUSPEND	McBSP1_CLKX/McBSP3_CLKX/GPIO_162	
J1.17	U4.K26	nSTANDBY	McBSP1_FSX/McSPI4_CS0/McBSP_FSX/GPIO_161	
J1.115	U4.D25	uP_nIRQC	CAM_STROBE/GPIO_126	
J1.117	U4.B23	uP_nIRQB	CAM_WEN/CAM_SHUTTER/GPIO_167	
J1.119	U4.C23	uP_nIRQA	CAM_FLD/CAM_GLOBAL_RESET/GPIO_98	
J1.136	U4.H18	uP_UARTB_CTS	UART3_CTS_RCTX/GPIO_163	
J1.138	U4.H19	uP_UARTB_RTS	UART3_RTS_SD/GPIO_164	
J1.139	U4.U3	uP_nBE1	GPMC_nBE1/GPIO_61	
J1.142	U4.B26	uP_GPIO_3	CAM_XCLKB/GPIO_111	
J1.154	U4.U21	uP_UARTA_DSR	McBSP1_DR/McSPI4_SOMI/McBSP3_DR/GPIO_159	
J1.162	U4.W8	uP_UARTA_CTS	UART1_CTS/SSI1_RDY_TX/HSUSB3_TLL_CLK/GPIO_150	
J1.164	U4.AA9	uP_UARTA_RTS	UART1_RTS/SSI1_FLAG_TX/GPIO_149	
J1.165	U4.D26	LCD_HSYNC	DSS_HSYNC/GPIO_67	
J1.167	U4.D27	LCD_VSYNC	DSS_VSYNC/GPIO_68	
J1.171	U4.D28	LCD_DCLK	DSS_PCLK/GPIO_66	
J1.175	U4.E27	LCD_MDISP	DSS_ACBIAS/GPIO_69	
J1.185	U4.AD27	LCD_D11	DSS_D11/SDI_DAT1P/GPIO_81	
J1.187	U4.AB28	LCD_D12	DSS_D12/SDI_DAT2N/GPIO_82	
J1.191	U4.AB27	LCD_D13	DSS_D13/SDI_DAT2P/GPIO_83	
J1.193	U4.AA28	LCD_D14	DSS_D14/SDI_DAT3N/GPIO_84	
J1.195	U4.AA27	LCD_D15	DSS_D15/SDI_DAT3P/GPIO_85	
J1.197	U4.AH24	LCD_D5	DSS_D5/UART3_TX_IRTX/DY2/GPIO_75	
J1.199	U4.E26	LCD_D6	DSS_D6/UART1_TX/GPIO_76	
J1.201	U4.F28	LCD_D7	DSS_D7/UART1_RX/GPIO_77	
J1.203	U4.F27	LCD_D8	DSS_D8/GPIO_78	

[2] http://www.ti.com/product/dm3730#technicaldocuments

J1/J2 Connection	U4 Connection	SOM-LV Signal	uP Signal	Notes
J1.205	U4.G26	LCD_D9	DSS_D9/GPIO_79	
J1.207	U4.AD28	LCD_D10	DSS_D10/SDI_DAT1N/GPIO_80	
J1.211	U4.AG22	LCD_D0	DSS_D0/UART1_CTS/DX0/GPIO_70	
J1.213	U4.AH22	LCD_D1	DSS_D1/UART1_RTS/DY0/GPIO_71	
J1.215	U4.AG23	LCD_D2	DSS_D2/DX1/GPIO_72	
J1.217	U4.AH23	LCD_D3	DSS_D3/DY1/GPIO_73	
J1.219	U4.AG24	LCD_D4	DSS_D4/UART3_RX_IRRX/DX2/GPIO_74	
J1.220	U4.AG4	uP_SPI_CS1	MMC2_DAT2/McSPI3_CS1/GPIO_134	
J1.222	U4.AF4	uP_SPI_CS0	MMC2_DAT3/McSPI3_CS0/GPIO_135	
J1.224	U4.AH5	uP_SPI_SOMI	MMC2_DAT0/McSPI3_SOMI/GPIO_132	
J1.226	U4.AG5	uP_SPI_SIMO	MMC2_CMD/McSPI3_SIMO/GPIO_131	
J2.10	U4.AE22	uP_CLKOUT2_26Mhz	SYS_CLKOUT2/GPIO_186	
J2.126	U4.Y21	SIM0_nDETECT	McBSP1_CLKR/McSPI4_CLK/SIM_CD/GPIO_156	
J2.127	U4.A24	CSI_HSYNC	CAM_HS/SSI2_DAT_TX/GPIO_94	
J2.128	U4.P26	SIM0_CLK	SIM_CLK/GPIO_127	1, 2
J2.131	U4.A23	CSI_VSYNC	CAM_VS/SSI2_FLAG_TX/GPIO_95	
J2.132	U4.P27	SIM0_IO/TX	SIM_IO/GPIO_126	1, 2
J2.133	U4.AG17	CSI_D0	CAM_D0/CSI2_DX2/GPIO_99	3
J2.135	U4.AH17	CSI_D1	CAM_D1/CSI2_DY2/GPIO_100	3
J2.136	U4.R25	SIM0_nRESET	MMC1_DAT7/SIM_RST/GPIO_129	1, 2
J2.137	U4.B24	CSI_D2	CAM_D2/SSI2_RDY_TX/GPIO_101	
J2.139	U4.C24	CSI_D3	CAM_D3/SSI2_DAT_RX/GPIO_102	
J2.141	U4.D24	CSI_D4	CAM_D4/SSI2_FLAG_RX/GPIO_103	
J2.143	U4.A25	CSI_D5	CAM_D5/SSI2_RDY_RX/GPIO_104	
J2.145	U4.K28	CSI_D6	CAM_D6/GPIO_105	3
J2.147	U4.L28	CSI_D7	CAM_D7/GPIO_106	3
J2.151	U4.K27	CSI_D8	CAM_D8/GPIO_107	3
J2.153	U4.L27	CSI_D9	CAM_D9/GPIO_108	3
J2.155	U4.B25	CSI_D10	CAM_D10/SSI2_WAKE/GPIO_109	
J2.167	U4.C25	CSI_MCLK	CAM_XCLKA/GPIO_96	
J2.171	U4.C27	CSI_PCLK	CAM_PCLK_GPIO_97	
J2.174	U4.AC28	LCD_D23	DSS_D23/SDI_CLKN/DSS_D5/GPIO_93	
J2.176	U4.AC27	LCD_D22	DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92	
J2.178	U4.J26	LCD_D21	DSS_D21/SDI_STP/McSPI3_CS0/DSS_D3/GPIO_91	
J2.180	U4.E28	LCD_D20	DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_D/GPIO_90	
J2.181	U4.AH18	CSI1_DY1	CSI2_DY1/GPIO_115	3
J2.182	U4.H25	LCD_D19	DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D/GPIO_89	
J2.183	U4.AG18	CSI1_DX1	CSI2_DX1/GPIO_114	3
J2.184	U4.H26	LCD_D18	DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88	
J2.185	U4.AH19	CSI1_DY0	CSI2_DY0/GPIO_113	3
J2.186	U4.H27	LCD_D17	DSS_D17/GPIO_87	
J2.187	U4.AG19	CSI1_DX0	CSI2_DX0/GPIO_112	3
J2.188	U4.G25	LCD_D16	DSS_D16/GPIO_86	

TABLE NOTES:

1. Due to buffer strength, an external serial resistor must be connected to the BGA balls where GPIO_120 through GPIO_129 are muxed with MMC signals; the resistor value is

dependent on the implementation in the final system design. More information about this requirement can be found in "Chapter 25.2: General-Purpose Interface Environment" in the *AM/DM37x Multimedia Device TRM*.

2. GPIO_120 through GPIO_127 and GPIO_129 require special registers to be set up in the DM3730 that control PBIAS settings. Please refer to "Chapter 13.4.5: Extended-Drain I/O Pin and PBIAS Cells" in the *AM/DM37x Multimedia Device TRM* for more information.

3. GPIO_99, GPIO_100, GPIO_105 through GPIO_108, and GPIO_112 through GPIO_115 can only be used as GPI (input only) and require that VAUX4 be enabled. See Logic PD's *AN 488 DM3730/AM3703 SOM-LV Power Management*[3] for information on how to enable the VAUX4 power supply.

2.2 DM3730/AM3703 Torpedo SOM GPIO Selection

Table 2.2 shows a list of available GPIO signals after being filtered using the following criteria:

- The *DM3730/AM3703 Torpedo Schematic*[4] (PN 1017879A) was used in creating this document. In the unlikely event that an I/O is changed on a future revision of the schematic, that change will need to be evaluated to determine its impact, if any, on Table 2.2.
- Signals were removed from the list if they touch more than two nodes within the schematic net list. All recommended signals connect directly between the DM3730 processor (U4) and one of the Torpedo SOM connectors (J1 or J2).
- GPIO_179 (MCSPI2_SIMO) and GPIO_180 (MCSPI2_SOMI) were removed since they are designated as output from LogicLoader; however, they can be used for testing purposes as demonstrated in this document.
- GPIO_151 (uP_UARTA_RX) and GPIO_148 (uP_UARTA_TX) were removed since they are used for the debug serial port from LogicLoader.
- GPIO_165 (uP_UARTB_RX) and GPIO_166 (uP_UARTB_TX) were removed since they are part of the default boot operation of the DM3730 processor and may toggle at boot time.
- GPIO_60 (GPMC_nBE0_CLE) was removed since it connects to the Package-on-Package (PoP) NAND flash memory.
- The GPIO signals in Table 2.2 are all available on the DM3730 processor. Additional GPIO signals may be available through the TPS65950 Power Management IC (PMIC); please see Appendix A for more information.

Be sure to consider the following items when selecting a GPIO for your embedded system:

- Verify available GPIOs based on the specific SOM schematic and system baseboard used in the final design.
- This list is based on the standard DM3730 Torpedo SOM configuration (SOMDM3730-20-2780AGCR-A) and does not take into account signals that may become available when certain resistor packs are populated.
- Verify the voltage levels of each GPIO signal are compatible with the receiving signal.
- Verify availability for reset configuration and internal pull-ups/pull-downs using "Table 13-84: CONTROL_PADCONF_CAPABILITIES" in the Texas Instruments (TI) *AM/DM37x Multimedia Device Technical Reference Manual (TRM)*.[5]

[3] http://support.logicpd.com/downloads/1444/
[4] http://support.logicpd.com/downloads/1468/
[5] http://www.ti.com/product/dm3730#technicaldocuments

Table 2.2: DM3730/AM3703 Torpedo SOM Filtered GPIOs

J1/J2 Connection	U4 Connection	Torpedo SOM Signal	uP Signal	Notes
J1.7	U4.L3	uP_A9	GPMC_A9/SYS_nDMAREQ2/GPIO_42	1
J1.11	U4.H3	uP_nCS1	GPMC_nCS1/GPIO_52	7
J1.13	U4.M3	uP_A8	GPMC_A8/GPIO_41	1
J1.21	U4.U3	uP_nBE1	GPMC_nBE1/GPIO_61	
J1.28	U4.P8	uP_nCS6	GPMC_nCS6/SYS_nDMAREQ3/McBSP4_DX/GPT11_PWM_EVT/GPIO_57	8
J1.29	U4.H2	uP_D8	GPMC_D8/GPIO_44	1, 2
J1.31	U4.K2	uP_D9	GPMC_D9/GPIO_45	1, 2
J1.32	U4.R8	uP_nCS5	GPMC_nCS5/SYS_nDMAREQ2/McBSP4_DR/GPT10_PWM_EVT/GPIO_56	
J1.34	U4.T8	uP_nCS4	GPMC_nCS4/SYS_nDMAREQ1/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55	
J1.36	U4.U8	uP_nCS3	GPMC_nCS3/SYS_nDMAREQ0/GPIO_54	
J1.38	U4.K3	uP_A10	GPMC_A10/SYS_nDMAREQ3/GPIO_43	1
J1.40	U4.V8	uP_nCS2	GPMC_nCS2/GPIO_53	
J1.41	U4.R2	uP_D12	GPMC_D12/GPIO_48	1, 2
J1.42	U4.K4	uP_A4	GPMC_A4/GPIO_37	1
J1.43	U4.P1	uP_D10	GPMC_D10/GPIO_46	1, 2
J1.44	U4.L4	uP_A3	GPMC_A3/GPIO_36	1
J1.45	U4.R1	uP_D11	GPMC_D11/GPIO_47	1, 2
J1.46	U4.M4	uP_A2	GPMC_A2/GPIO_35	1
J1.47	U4.T2	uP_D13	GPMC_D13/GPIO_49	1, 2
J1.48	U4.N4	uP_A1	GPMC_A1/GPIO_34	1
J1.50	U4.N3	uP_A7	GPMC_A7/GPIO_40	1
J1.51	U4.V3	MCSPI2_CS1	McSPI2_CS1/GPT8_PWM_EVT/HSUSB2_TLL_DATA3/USUSB2_DATA3/MM2_TXEN_N/GPIO_182	
J1.52	U4.R3	uP_A6	GPMC_A6/GPIO_39	1
J1.54	U4.T3	uP_A5	GPMC_A5/GPIO_38	1
J1.58	U4.Y4	MCSPI2_CS0	McSPI2_CS0/GPT11_PWM_EVT/HSUSB2_TLL_DATA6/HSUSB2_DATA6/GPIO_181	
J1.59	U4.W1	uP_D14	GPMC_D14/GPIO_50	1, 2
J1.60	U4.AA4	MCSPI1_SOMI	McSPI1_SOMI/MMC2_DAT6/GPIO_173	
J1.62	U4.AD1	MCBSP4_DR	McBSP4_DR/SSI1_FLAG_RX/HSUSB3_TLL_DATA0/MM3_RXRCV/GPIO_153	
J1.63	U4.Y1	uP_D15	GPMC_D15/GPIO_51	1, 2
J1.64	U4.AB3	MCSPI1_CLK	McSPI1_CLK/MMC2_DAT4GPIO_171	
J1.66	U4.AB4	MCSPI1_SIMO	McSPI1_SIMO/MMC2_DAT5/GPIO_172	
J1.67	U4.AA3	MCSPI2_CLK	McSPI2_CLK/HSUSB2_TLL_DATA7/HSUSB2_DATA7/GPIO_178	
J1.68	U4.W8	uP_UARTA_CTS	UART1_CTS/SSI1_RDY_TX/HSUSB3_TLL_CLK/GPIO_150	
J1.69	U4.AC3	MCSPI1_CS1	McSPI1_CS1/ADPLLV2D_DITHERING_EN2/MMC3_CMD/GPIO_175	
J1.71	U4.AC2	MCSPI1_CS0	McSPI1_CS0/MMC2_DAT7/GPIO_174	
J1.73	U4.AC1	LCD_PANEL_PWR	McBSP4_FSX/SSI1_WAKE/HSUSB3_TLL_DATA3/MM3_TXEN_n/GPIO_155	
J1.74	U4.AA9	uP_UARTA_RTS	UART1_RTS/SSI1_FLAG_TX/GPIO_149	
J1.75	U4.AD2	LCD_BACKLIGHT_PWR	McBSP4_DX/SSI1_RDY_RX//HSUSB3_TLL_DATA2/MM3_TXDAT/GPIO_154	

J1/J2 Connection	U4 Connection	Torpedo SOM Signal	uP Signal	Notes
J1.84	U4.AH5	SD2_DATA0	MMC2_DAT0/McSPI3_SOMI/GPIO_132	
J1.91	U4.AF4	SD2_DATA3	MMC2_DAT3/McSPI3_CS0/GPIO_135	
J1.93	U4.AG4	SD2_DATA2	MMC2_DAT2/McSPI3_CS1/GPIO_134	
J1.95	U4.AH4	SD2_DATA1	MMC2_DAT1/GPIO_133	
J1.97	U4.AG5	SD2_CMD	MMC2_CMD/McSPI3_SIMO/GPIO_131	
J1.98	U4.N8	uP_IODIR	GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58	
J2.12	U4.D26	LCD_HSYNC	DSS_HSYNC/GPIO_67	
J2.14	U4.D27	LCD_VSYNC	DSS_VSYNC/GPIO_68	
J2.16	U4.E27	LCD_MDISP	DSS_ACBIAS/GPIO_69	
J2.18	U4.E26	LCD_D6	DSS_D6/UART1_TX/GPIO_76	
J2.22	U4.G26	LCD_D9	DSS_D9/UART3_TX_IRTX/GPIO_79	
J2.24	U4.F27	LCD_D8	DSS_D8/UART3_RX_IRRX/GPIO_78	
J2.26	U4.F28	LCD_D7	DSS_D7/UART1_RX/GPIO_77	
J2.29	U4.A25	CSI_D5	CAM_D5/SSI2_RDY_RX/GPIO_104	
J2.31	U4.B24	CSI_D2	CAM_D2/SSI2_RDY_TX/GPIO_101	
J2.33	U4.C24	CSI_D3	CAM_D3/SSI2_DAT_RX/GPIO_102	
J2.35	U4.D24	CSI_D4	CAM_D4/SSI2_FLAG_RX/GPIO_103	
J2.42	U4.M27	SD1_CMD	MMC1_CMD/MS_BS/GPIO_121	3, 4, 5
J2.44	U4.N25	SD1_DATA2	MMC1_DAT2/MS_DAT2/GPIO_124	3, 4, 5
J2.45	U4.K26	MCSPI4_CS0	McBSP1_FSX/McSPI4_CS0/McBSP_FSX/GPIO_161	
J2.46	U4.N26	SD1_DATA1	MMC1_DAT1/MS_DAT1/GPIO_123	3, 4, 5
J2.48	U4.N27	SD1_DATA0	MMC1_DAT0/MS_DAT0/GPIO_122	3, 4, 5
J2.50	U4.P28	SD1_DATA3	MMC1_DAT3/MS_DAT3/GPIO_125	3, 4, 5
J2.54	U4.P26	uP_GPIO_127	SIM_CLK/GPIO_127	3, 5
J2.56	U4.R27	uP_GPIO_128	SIM_PWRCTRL/GPIO_128	3
J2.58	U4.R25	uP_GPIO_129	/SIM_RST/GPIO_129	3, 5
J2.66	U4.AA28	LCD_D14	DSS_D14/SDI_DAT3N/GPIO_84	
J2.68	U4.AB27	LCD_D13	DSS_D13/SDI_DAT2P/GPIO_83	
J2.70	U4.AB28	LCD_D12	DSS_D12/SDI_DAT2N/GPIO_82	
J2.72	U4.AA25	uP_UARTC_TX	UART2_TX/MCBSP3_CLKX/GPT11_PWM_EVT/GPIO_146	
J2.74	U4.AB25	uP_UARTC_RTS	UART2_RTS/MCBSP3_DR/GPT10_PWM_EVT/GPIO_145	
J2.76	U4.AB26	uP_UARTC_CTS	UART2_CTS/MCBSP3_DX/GPT9_PWM_EVT/GPIO_144	
J2.78	U4.AA27	LCD_D15	DSS_D15/SDI_DAT3P/GPIO_85	
J2.79	U4.E28	LCD_D2	LCD_D20/SDI_DEN/McSPI3_SOMI/DSS_D2/GPIO_90	
J2.81	U4.J26	LCD_D3	DSS_D21/SDI_STP/McSPI3_CS0/DSS_D3/GPIO_91	
J2.82	U4.AD28	LCD_D10	DSS_D10/SDI_DAT1N/GPIO_80	
J2.83	U4.H25	LCD_D1	DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89	
J2.84	U4.AD27	LCD_D11	DSS_D11/SDI_DAT1P/GPIO_81	
J2.85	U4.AG17	CSI_D0	CAM_D0/CSI2_DX2/GPIO_99	6
J2.86	U4.AD25	uP_UARTC_RX	UART2_RX/MCBSP3_FSX/GPT8_PWM_EVT/GPIO_147	
J2.87	U4.AH17	CSI_D1	CAM_D1/CSI2_DY2/GPIO_100	6
J2.94	U4.AC27	LCD_D4	DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92	
J2.96	U4.AC28	LCD_D5	DSS_D23/SDI_CLKN/DSS_D5/GPIO_93	
J2.98	U4.H25	LCD_D0	DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88	

TABLE NOTES:

1. These signals also have a possible connection to the top PoP BGA footprint. Caution must be used when considering these signals as alternative GPIO function.
2. These signals are not available when using PoP memories with 16-bit NAND memory.
3. Due to buffer strength, an external serial resistor must be connected to the BGA balls where GPIO_120 through GPIO_129 are muxed with MMC signals; the resistor value is dependent on the implementation in the final system design. More information about this requirement can be found in "Chapter 25.2: General-Purpose Interface Environment" of the *AM/DM37x Multimedia Device TRM*.
4. VMMC1 must be enabled to use GPIO_120 through GPIO_125. Note that VMMC1 can be enabled for 1.8V or 3.0V operation.
5. GPIO_120 through GPIO_127 and GPIO_129 require special registers to be set up in the DM3730 that control PBIAS settings. Please refer to "Chapter 13.4.5: Extended-Drain I/O Pin and PBIAS Cells" in the *AM/DM37x Multimedia Device TRM* for more information.
6. GPIO_99 and GPIO_100 can only be used as GPI (input only) and require that VAUX4 be enabled. See Logic PD's *AN 489 DM3730/AM3703 Torpedo SOM Power Management*[6] for information on how to enable the VAUX4 power supply.
7. Used for Ethernet chip select on the DM3730 Torpedo SOM Development Kit. Can be used as GPIO if Ethernet is not enabled in software.
8. Used for USB host chip select on the DM3730 Torpedo SOM Development Kit. Can be used as GPIO if USB Host is not enabled in software.

2.3 DM3730/AM3703 Torpedo + Wireless SOM GPIO Selection

Table 2.3 shows a list of available GPIO signals after being filtered using the following criteria:

- The *DM3730 Torpedo + Wireless SOM Schematic*[7] (PN 1020613A) was used in creating this document. In the unlikely event that an I/O is changed on a future revision of the schematic, that change will need to be evaluated to determine its impact, if any, on Table 2.3.
- Signals were removed from the list if they touch more than two nodes within the schematic net list. All recommended signals connect directly between the DM3730 processor (U4) and one of the Torpedo + Wireless SOM connectors (J1 or J2).
- GPIO_179 (MCSPI2_SIMO) and GPIO_180 (MCSPI2_SOMI) were removed since they are designated as output from LogicLoader; however, they can be used for testing purposes as demonstrated in this document.
- GPIO_151 (uP_UARTA_RX) and GPIO_148 (uP_UARTA_TX) were removed since they are used for the debug serial port from LogicLoader.
- GPIO_165 (uP_UARTB_RX) and GPIO_166 (uP_UARTB_TX) were removed since they are part of the default boot operation of the DM3730 processor and may toggle at boot time.
- GPIO_60 (GPMC_nBE0_CLE) was removed since it connects to the Package-on-Package (PoP) NAND flash memory.
- The GPIO signals in Table 2.3 are all available on the DM3730 processor. Additional GPIO signals may be available through the TPS65950 power management IC (PMIC); please see Appendix A for more information.

[6] http://support.logicpd.com/downloads/1446/
[7] http://support.logicpd.com/downloads/1531/

Be sure to consider the following items when selecting a GPIO for your embedded system:

- Verify available GPIOs based on the specific SOM schematic and system baseboard used in the final design.
- This list is based on the standard DM3730 Torpedo + Wireless SOM configuration (SOMDM3730-30-2780AKCR-2) and does not take into account signals that may become available when certain resistor packs are populated.
- Verify the voltage levels of each GPIO signal are compatible with the receiving signal.
- Verify availability for reset configuration and internal pull-ups/pull-downs using "Table 13-84: CONTROL_PADCONF_CAPABILITIES" in the Texas Instruments (TI) *AM/DM37x Multimedia Device Technical Reference Manual (TRM)*.[8]

Table 2.3: DM3730/AM3703 Torpedo + Wireless SOM Filtered GPIOs

J1/J2 Connection	U4 Connection	Torpedo + Wireless SOM Signal	uP Signal	Notes
J1.7	U4.L3	uP_A9	GPMC_A9/SYS_nDMAREQ2/GPIO_42	1
J1.11	U4.H3	uP_nCS1	GPMC_nCS1/GPIO_52	
J1.13	U4.M3	uP_A8	GPMC_A8/GPIO_41	1
J1.21	U4.U3	uP_nBE1	GPMC_nBE1/GPIO_61	
J1.28	U4.P8	uP_nCS6	GPMC_nCS6/SYS_nDMAREQ3/McBSP4_DX/GPT11_PWM_EVT/GPIO_57	
J1.29	U4.H2	uP_D8	GPMC_D8/GPIO_44	1, 2
J1.31	U4.K2	uP_D9	GPMC_D9/GPIO_45	1, 2
J1.32	U4.R8	uP_nCS5	GPMC_nCS5/SYS_nDMAREQ2/McBSP4_DR/GPT10_PWM_EVT/GPIO_56	
J1.34	U4.T8	uP_nCS4	GPMC_nCS4/SYS_nDMAREQ1/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55	
J1.36	U4.U8	uP_nCS3	GPMC_nCS3/SYS_nDMAREQ0/GPIO_54	
J1.38	U4.K3	uP_A10	GPMC_A10/SYS_nDMAREQ3/GPIO_43	1
J1.40	U4.V8	uP_nCS2	GPMC_nCS2/GPIO_53	
J1.41	U4.R2	uP_D12	GPMC_D12/GPIO_48	1, 2
J1.42	U4.K4	uP_A4	GPMC_A4/GPIO_37	1
J1.43	U4.P1	uP_D10	GPMC_D10/GPIO_46	1, 2
J1.44	U4.L4	uP_A3	GPMC_A3/GPIO_36	1
J1.45	U4.R1	uP_D11	GPMC_D11/GPIO_47	1, 2
J1.46	U4.M4	uP_A2	GPMC_A2/GPIO_35	1
J1.47	U4.T2	uP_D13	GPMC_D13/GPIO_49	1, 2
J1.48	U4.N4	uP_A1	GPMC_A1/GPIO_34	1
J1.50	U4.N3	uP_A7	GPMC_A7/GPIO_40	1
J1.51	U4.V3	MCSPI2_CS1	McSPI2_CS1/GPT8_PWM_EVT/HSUSB2_TLL_DATA3/USUSB2_DATA3/MM2_TXEN_N/GPIO_182	
J1.52	U4.R3	uP_A6	GPMC_A6/GPIO_39	1
J1.54	U4.T3	uP_A5	GPMC_A5/GPIO_38	1
J1.58	U4.Y4	MCSPI2_CS0	McSPI2_CS0/GPT11_PWM_EVT/HSUSB2_TLL_DATA6/HSUSB2_DATA6/GPIO_181	
J1.59	U4.W1	uP_D14	GPMC_D14/GPIO_50	1, 2
J1.60	U4.AA4	MCSPI1_SOMI	McSPI1_SOMI/MMC2_DAT6/GPIO_173	
J1.62	U4.AD1	MCBSP4_DR	McBSP4_DR/SSI1_FLAG_RX/HSUSB3_TLL_DATA0/MM3_RXRCV/GPIO_153	

[8] http://www.ti.com/product/dm3730#technicaldocuments

J1/J2 Connection	U4 Connection	Torpedo + Wireless SOM Signal	uP Signal	Notes
J1.63	U4.Y1	uP_D15	GPMC_D15/GPIO_51	1, 2
J1.64	U4.AB3	MCSPI1_CLK	McSPI1_CLK/MMC2_DAT4GPIO_171	
J1.66	U4.AB4	MCSPI1_SIMO	McSPI1_SIMO/MMC2_DAT5/GPIO_172	
J1.67	U4.AA3	MCSPI2_CLK	McSPI2_CLK/HSUSB2_TLL_DATA7/HSUSB2_DATA7/GPIO_178	
J1.68	U4.W8	uP_UARTA_CTS	UART1_CTS/SSI1_RDY_TX/HSUSB3_TLL_CLK/GPIO_150	
J1.69	U4.AC3	MCSPI1_CS1	McSPI1_CS1/ADPLLV2D_DITHERING_EN2/MMC3_CMD/GPIO_175	
J1.70	U4.Y8	MCSPI2_CS0	McSPI2_CS0/GPT11_PWM_EVT/HSUSB2_TLL_DATA6/HSUSB2_DATA6/GPIO_181	
J1.71	U4.AC2	MCSPI1_CS0	McSPI1_CS0/MMC2_DAT7/GPIO_174	
J1.72	U4.AA8	uP_UARTA_TX	UART1_TX/SSI1_DAT_TX/GPIO_148	
J1.73	U4.AC1	LCD_PANEL_PWR	McBSP4_FSX/SSI1_WAKE/HSUSB3_TLL_DATA3/MM3_TXEN_n/GPIO_155	
J1.74	U4.AA9	uP_UARTA_RTS	UART1_RTS/SSI1_FLAG_TX/GPIO_149	
J1.75	U4.AD2	LCD_BACKLIGHT_PWR	McBSP4_DX/SSI1_RDY_RX//HSUSB3_TLL_DATA2/MM3_TXDAT/GPIO_154	
J1.84	U4.AH5	SD2_DATA0	MMC2_DAT0/McSPI3_SOMI/GPIO_132	
J1.91	U4.AF4	SD2_DATA3	MMC2_DAT3/McSPI3_CS0/GPIO_135	
J1.93	U4.AG4	SD2_DATA2	MMC2_DAT2/McSPI3_CS1/GPIO_134	
J1.95	U4.AH4	SD2_DATA1	MMC2_DAT1/GPIO_133	
J1.97	U4.AG5	SD2_CMD	MMC2_CMD/McSPI3_SIMO/GPIO_131	
J1.98	U4.N8	uP_IODIR	GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58	
J2.12	U4.D26	LCD_HSYNC	DSS_HSYNC/GPIO_67	
J2.14	U4.D27	LCD_VSYNC	DSS_VSYNC/GPIO_68	
J2.16	U4.E27	LCD_MDISP	DSS_ACBIAS/GPIO_69	
J2.18	U4.E26	LCD_D6	DSS_D6/UART1_TX/GPIO_76	
J2.22	U4.G26	LCD_D9	DSS_D9/UART3_TX_IRTX/GPIO_79	
J2.24	U4.F27	LCD_D8	DSS_D8/UART3_RX_IRRX/GPIO_78	
J2.26	U4.F28	LCD_D7	DSS_D7/UART1_RX/GPIO_77	
J2.29	U4.A25	CSI_D5	CAM_D5/SSI2_RDY_RX/GPIO_104	
J2.31	U4.B24	CSI_D2	CAM_D2/SSI2_RDY_TX/GPIO_101	
J2.33	U4.C24	CSI_D3	CAM_D3/SSI2_DAT_RX/GPIO_102	
J2.35	U4.D24	CSI_D4	CAM_D4/SSI2_FLAG_RX/GPIO_103	
J2.37	U4.H18	uP_UARTB_CTS	UART3_CTS_RCTX/GPIO_163	
J2.39	U4.H19	uP_UARTB_RTS	UART3_RTS_SD/GPIO_164	
J2.42	U4.M27	SD1_CMD	MMC1_CMD/MS_BS/GPIO_121	3, 4, 5
J2.44	U4.N25	SD1_DATA2	MMC1_DAT2/MS_DAT2/GPIO_124	3, 4, 5
J2.45	U4.K26	MCSPI4_CS0	McBSP1_FSX/McSPI4_CS0/McBSP_FSX/GPIO_161	
J2.46	U4.N26	SD1_DATA1	MMC1_DAT1/MS_DAT1/GPIO_123	3, 4, 5
J2.48	U4.N27	SD1_DATA0	MMC1_DAT0/MS_DAT0/GPIO_122	3, 4, 5
J2.50	U4.P28	SD1_DATA3	MMC1_DAT3/MS_DAT3/GPIO_125	3, 4, 5
J2.52	U4.C23	CSI_FLD	CAM_FLD/CAM_GLOBAL_RESET/GPIO_98	
J2.54	U4.P26	uP_GPIO_127	SIM_CLK/GPIO_127	
J2.56	U4.R27	uP_GPIO_128	SIM_PWRCTRL/GPIO_128	
J2.58	U4.R25	uP_GPIO_129	SIM_RST/GPIO_129	
J2.66	U4.AA28	LCD_D14	DSS_D14/SDI_DAT3N/GPIO_84	

J1/J2 Connection	U4 Connection	Torpedo + Wireless SOM Signal	uP Signal	Notes
J2.68	U4.AB27	LCD_D13	DSS_D13/SDI_DAT2P/GPIO_83	
J2.70	U4.AB28	LCD_D12	DSS_D12/SDI_DAT2N/GPIO_82	
J2.78	U4.AA27	LCD_D15	DSS_D15/SDI_DAT3P/GPIO_85	
J2.83	U4.H25	LCD_D1	DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89	
J2.84	U4.AD27	LCD_D11	DSS_D11/SDI_DAT1P/GPIO_81	
J2.85	U4.AG17	CSI_D0	CAM_D0/CSI2_DX2/GPIO_99	6
J2.87	U4.AH17	CSI_D1	CAM_D1/CSI2_DY2/GPIO_100	6
J2.98	U4.H26	LCD_D0	DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88	

TABLE NOTES:

1. These signals also have a possible connection to the top PoP BGA footprint. Caution must be used when considering these signals as alternative GPIO function.
2. These signals are not available when using PoP memories with 16-bit NAND memory.
3. Due to buffer strength, an external serial resistor must be connected to the BGA balls where GPIO_120 through GPIO_129 are muxed with MMC signals; the resistor value is dependent on the implementation in the final system design. More information about this requirement can be found in "Chapter 25.2: General-Purpose Interface Environment" in the *AM/DM37x Multimedia Device TRM*.
4. VMMC1 must be enabled to use GPIO_120 through GPIO_125. Note that VMMC1 can be enabled for 1.8V or 3.0V operation.
5. GPIO_120 through GPIO_129 require special registers to be set up in the DM3730 that control PBIAS settings. Please refer to "Chapter 13.4.5: Extended-Drain I/O Pin and PBIAS Cells" in the *AM/DM37x Multimedia Device TRM* for more information.
6. GPIO_99, GPIO_100, and GPIO_112 through GPIO_115 can only be used as GPI (input only) and require that VAUX4 be enabled. See Logic PD's *AN 528 DM3730/AM3703 Torpedo + Wireless SOM Power Management*[9] for information on how to enable the VAUX4 power supply.

[9] http://support.logicpd.com/downloads/1480/

3 Configure GPIO Examples

This section will describe how to program the DM3730/AM3703 GPIO_111 signal on the DM3730/AM3703 SOM using LogicLoader, Windows CE, Linux, and Android. Each example will show how to configure GPIO_111 as an output or an input. For accessing GPIO_111 on the DM3730 Development Kits, use the connections noted below.

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- GPIO_111 access is through J17.36 on the breakout board.
- Ground reference in the examples below is J17.1 on the breakout board.
- 1.8V reference in the examples below is J18.68 (VIO_1V8) on the breakout board.

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- GPIO_111 access is through J6.20 on the baseboard.
- Ground reference in the examples below is J6.25 on the baseboard.
- 1.8V reference in the examples below is J30.22 on the baseboard.

NOTE: The Torpedo Launcher 3 Baseboard requires R197 to be populated with a zero ohm resistor to connect CAM_XCLKB to J6.20. R198 must be removed since the Torpedo Launcher 3 Baseboard comes with CAM_FLD as the default signal driving J6.20. R197 and R198 can be seen on revision F or later of the *Torpedo Launcher 3 Baseboard Schematics*, available on the DM3730 Torpedo Development Kit downloads page.[10]

3.1 Configure GPIO Signals using LogicLoader

It is possible to set up and configure GPIOs on both the DM3730/AM3703 processor and TPS65950 PMIC by using scripting functionality provided in LogicLoader. Examples of how to use processor GPIO functionality are provided in this section; there is an example in Appendix B on how to access TPS65950 GPIO signals using LogicLoader.

In this example of accessing a GPIO signal on the DM3730/AM3703 processor, signal GPIO_111 will be driven high and low. According to Logic PD's *DM3730/AM3703 SOM-LV Schematic* and *High-Density Breakout Board Schematic*,[11] GPIO_111 is tied to the DM3730/AM3703 processor CAM_XCLKB/GPIO_111 signal and is routed to pin J17.36 on the breakout board. If you wish to monitor the output from the breakout board, attach a digital voltmeter, oscilloscope probe, or logic analyzer to J17.36.

First, we need to determine which of the pin mux registers within the DM3730/AM3703 processor correspond to the CAM_XCLKB signal; this information can be found in "Chapter 13: System Control Module" of TI's *AM/DM37x Multimedia Device TRM*. Locate the CAM_XCLKB signal in Table 13-4: "Core Control Module Pad Configuration Register Fields." On the row with CAM_XCLKB, notice the Mode 4 column corresponds with GPIO_111; in other words, we want to change the MUXMODE to 4 to enable the GPIO function. Also notice that the CAM_XCLKB pad configuration can be found in the CONTROL_PADCONF_CAM_D11[31:16] register at address 0x4800_212C; this means that CAM_XCLKB control is in the upper half of that register.

1. At the losh> prompt in LogicLoader, enter the following command.

```
losh> x /w 0x4800212c        # Read contents of CONTROL_PADCONF_CAM_D11
0x4800212c  010f011c  ....
```

[10] http://support.logicpd.com/auth/downloads/DM3730-AM3703-Torpedo/
[11] http://support.logicpd.com/downloads/1443/

2. In the *AM/DM37x Multimedia Device TRM*, "Table 13-82: CONTROL_PADCONF_X" indicates we want to set MUXMODE to 0x4; the rest of the bits can remain the same.

```
losh> temp = $@                          # Set temp equal to value
                                         # seen in previous command
losh> temp = $temp & 0x0000ffff          # Clear upper 16 bit
losh> temp = $temp | 0x00040000          # Set upper 16 bits
                                         # for MUXMODE 4
losh> w /w 0x4800212c $temp              # Set the MUXMODE of
                                         # CAM_XCLKB for GPIO_111
writing: (8) *4800212c = 0004011c
```

Next, we'll look at "Chapter 25: General-Purpose Interface Overview" in the *AM/DM37x Multimedia Device TRM* to configure GPIO_111. The DM3730/AM3703 processor has six banks of GPIOs; each bank contains thirty-two GPIOs. GPIO_111 can be found in bank GPIO4 as bit number 15 (see Table 25-5: "GPIO Channel Description" in the *AM/DM37x Multimedia Device TRM*).

3.1.1 GPIO Output

Building on the steps in the section above, it is now possible to configure the GPIO as an output. GPIOs are inputs by default; if you need the GPIO to be an output, it is best to configure the appropriate output level before changing the signal direction.

1. Write to GPIO4 GPIO_SETDATAOUT to set the signal high.

```
losh> w /w 0x49054094 0x00008000         # Write the SETDATAOUT
                                         # with bit 15 set, GPIO_111 high
writing: (8) *49058094 = 00008000
```

2. Next, we need to set the GPIO direction with GPIO4 GPIO_OE.

```
losh> x /w 0x49054034                    # Read the data direction bits
0x49058034  ffffffff ....
losh> temp = $@                          # Set temp equal to value
                                         # seen in previous command
losh> temp = $temp & 0xffff7fff          # Clear just the bit
                                         # associated to GPIO_111
losh> w /w 0x49054034 $temp              # Write the modified value
                                         # of GPIO_OE with bit 15,
                                         # GPIO_111 set as output
writing: (8) *49054034 = 0ffff7fff
```

At this point, the GPIO signal will be high on the measuring instrumentation.

3. To send it low, write to GPIO4 GPIO_CLEARDATAOUT.

```
losh> w /w 0x49054090 0x00008000         # Write the CLEARDATAOUT
                                         # with bit 15 set, GPIO_111
                                         # low
writing: (8) *49054090 = 00008000
```


3.1.2 GPIO Input

To read the value of GPIO_111, reset the board, tie the pin ground reference stated at the beginning of Section 0, and perform the steps below.

1. At the losh> prompt in LogicLoader, enter the command below.

```
losh> x /w 0x4800212c                    # Read contents of
                                         # CONTROL_PADCONF_CAM_D11
0x4800212c  010f011c  ....
```

2. In the *AM/DM37x Multimedia Device TRM*, "Table 13-82: CONTROL_PADCONF_X" indicates we want to set MUXMODE to 0x4 and set INPUTENABLE to 0x1; the rest of the bits can remain the same.

```
losh> temp = $@                          # Set temp equal to value
                                         # seen in previous command
losh> temp = $temp & 0x0000ffff          # Clear upper 16 bit
losh> temp = $temp | 0x01040000          # Set upper 16 bits
                                         # for MUXMODE 4, enable input
losh> w /w 0x4800212c $temp              # Set the MUXMODE of CAM_XCLKB
                                         # for GPIO_111 and enable input
writing: (8) *4800212c = 0104011c
```

3. Tie the pin to 1.8V reference.

```
losh> x /w 0x49054038                    #Read the values on GPIO bank 4
0x49054038  00008000                           ....
```

4. Tie the pin to ground.

```
losh> x /w 0x49054038                    #Read the values on GPIO bank 4
0x49054038  00000000                           ....
```

3.2 Configure GPIO Signals in Windows CE

IMPORTANT NOTE: Windows CE software is not supported for use on the DM3730/AM3703 Torpedo + Wireless SOM.

This section describes how to access GPIO signals on the DM3730/AM3703 processor using Logic PD's DM37x Windows Embedded CE 6.0 BSP version 3.0.0 or later. Logic PD provides an application programming interface (API) in the BSP. The API header information can be found in the following directory:

.\WINCE600\PLATFORM\COMMON\SRC\SOC\OMAP35XX_TPS659XX_TI_V1\inc\gpio.h

As previously stated, GPIO_133 and uP_GPIO_1 signals on the DM3730/AM3703 SOM-LV are not recommended for use in a production system. However, they can be used for testing purposes. For additional information on how uP_GPIO_1 is used within the DM37x Windows Embedded CE 6.0 BSP, refer to the code in the following BSP routine:

src\oal\oallib\debug.c OEMWriteDebugLED()

3.2.1 GPIO_Win32 Sample Application

Download the Visual Studio 2005 (VS2005) Win32 GPIO Sample Application[12] (hereafter GPIO_Win32) from Logic PD's website. Using this application you can drive GPIO_133 (gpio133) on the DM3730/AM3703 SOM. After the download has completed, extract the ZIP file and locate the *gpio_win32_readme.txt* file. Please read this file for specific system requirements and instructions on how to use the sample application before continuing through this application note.

3.2.2 Modify Sample Application for GPIO_111

The following sections will describe how to change the GPIO_Win32 sample application to toggle the DM3730/AM3703 GPIO_111 signal instead of GPIO_133.

To verify the GPIO_111 signal is truly toggling, measure the voltage on the appropriate pin for your development kit:

- J17.36 on the DM3730 SOM-LV Development Kit breakout board
- J6.20 on the DM3730 Torpedo Development Kit baseboard

NOTE: If a different GPIO signal is desired, please refer to Section 2 to select a GPIO signal. If you are using the DM3730 SOM-LV Development Kit, please refer to Appendix A to determine which breakout board pin must be probed for testing.

3.2.2.1 Build Modified GPIO_Win32 Sample Application

Before modifying the GPIO_Win32 sample application, the DM3730/AM3703 processor must be configured for pin muxing.

1. Make sure you have selected the correct OS design solution for your kit.

   If you are using the DM3730/AM3703 SOM-LV, the BSP already sets up GPIO_111 and you can now skip to Step 4 below.

2. Locate the *platform.c* file in the *102xxxxx_LogicPD _WinCE6_BSP_x-x-x.zip* file at *platform\LOGIC_ARM_A8\src\oal\oallib\platform.c*.

3. In the *platform.c* file, add the following line **before** the #if 0 //Leave as Default State section.

```
OUTREG16(&pConfig->CONTROL_PADCONF_CAM_XCLKB, (INPUT_DISABLE |
PULL_INACTIVE | MUX_MODE_4)); /*CAM_XCLKB*/
```

   This line can be found near line #648.

4. Perform a build by selecting Build > Advance Build Commands > Build Current BSP and Subprojects.

5. Next, change line 35 in the *GPIO_Win32.cpp* file of the GPIO_Win32 sample application to the following:

```
#define GPIO_LED                                111 //SOM-LV uP_GPIO_3
```

[12] http://support.logicpd.com/downloads/1285/

An example of this is shown in Figure 3.1 below.

```
#ifdef BSP_TORPEDO
#define GPIO_DEVICE_NAME        L"TWL1:"
#define GPIO_LED                17 //Torpedo PMIC GPIO 17 - J31.15
#else
#define GPIO_DEVICE_NAME        L"GIO1:"
//#define GPIO_LED              133 //SOM-LV uP_GPIO_0
#define GPIO_LED                111 //SOM-LV uP_GPIO_3

#endif
```

Figure 3.1: Change to Line 35 in GPIO_Win32.cpp File

6. After line 35 has been changed, select Build > Build Solution in your GPIO_Win32 sample application to build in the changes.
7. Copy your newly modified GPIO_Win32 sample application from the build directory.

   NOTE: The location of the build directory can be seen in the VS2005 output window as shown in Figure 3.2 below. Your application will exist in the same location as the *BuildLog.htm* file. The location of the *BuildLog.htm* file is seen in the VS2005 output window as the third line from the bottom.

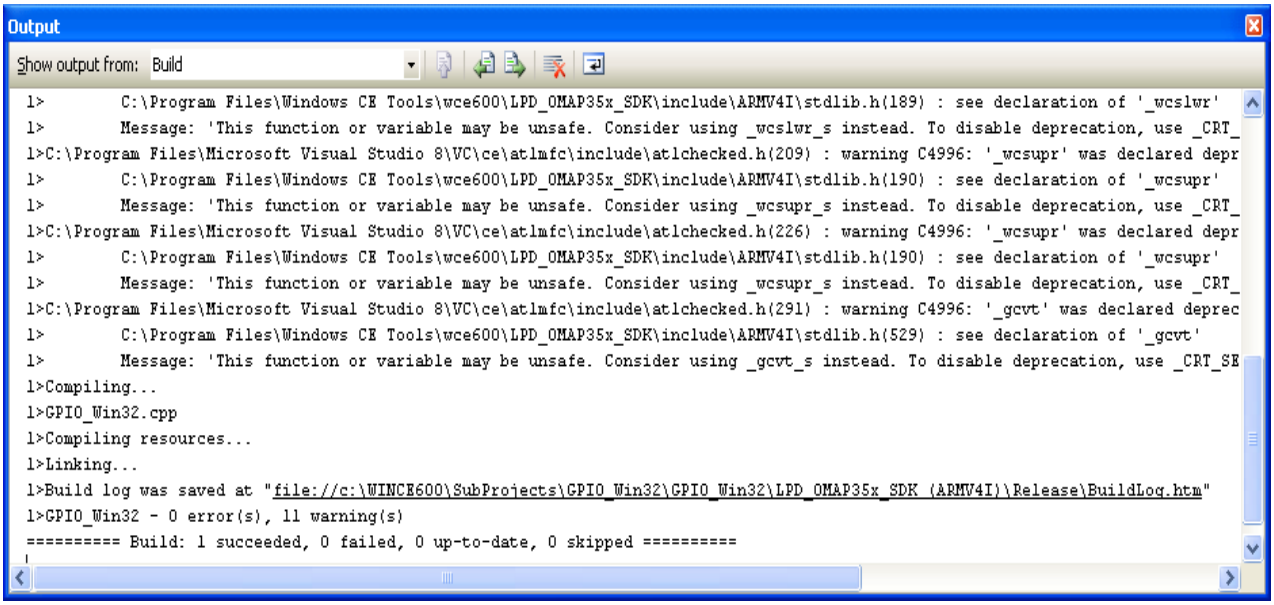

Figure 3.2: VS2005 Output Window

Figure 3.3 shows these files in the GPIO_Win32 sample application build directory.

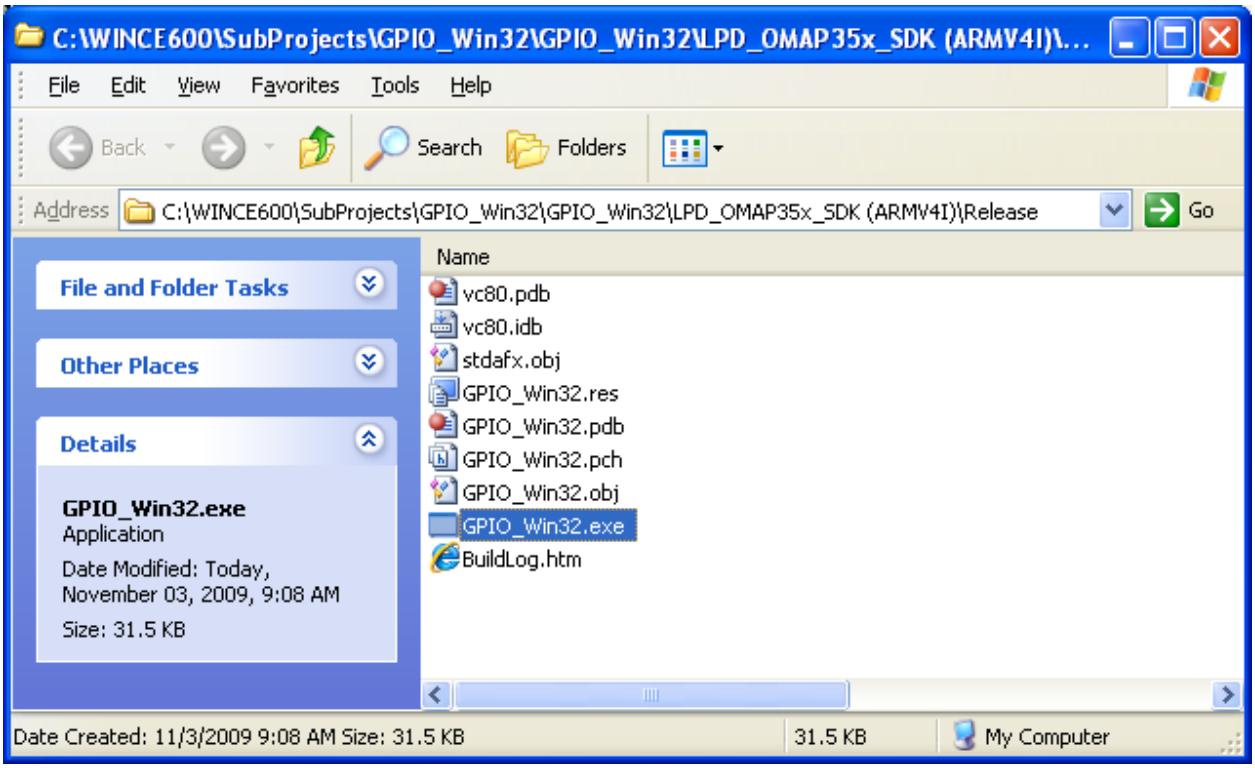

Figure 3.3: GPIO_Win32 Application Build Directory

8. Paste the copied GPIO_Win32 sample application on to an SD card.

3.2.2.2 Run Modified GPIO_Win32 Sample Application from SD Card

1. Insert the SD card containing the modified GPIO_Win32 sample application into your DM3730 Development Kit and power it on.
2. After Windows CE launches, select Start > Programs > Windows Explorer > SD_Card > GPIO_Win32.exe to run the application.

Figure 3.4 shows the window prior to running the GPIO_Win32 application.

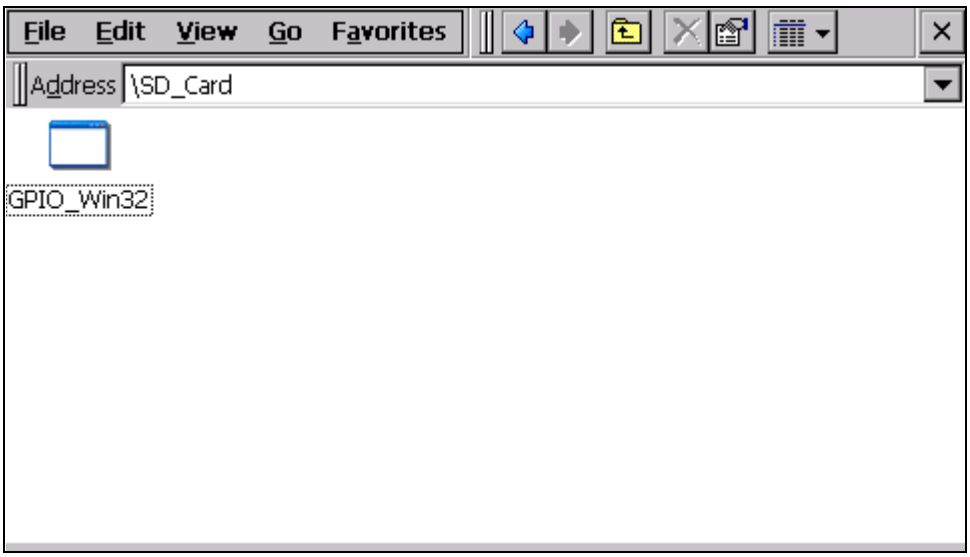

Figure 3.4: Windows Explore SD_Card Files

3. After running the GPIO_Win32 sample application, your LCD will display a red box with two buttons below the box, similar to that in Figure 3.5 below. This is considered the OFF state. By selecting the ON button on the touchscreen, the box will turn green.

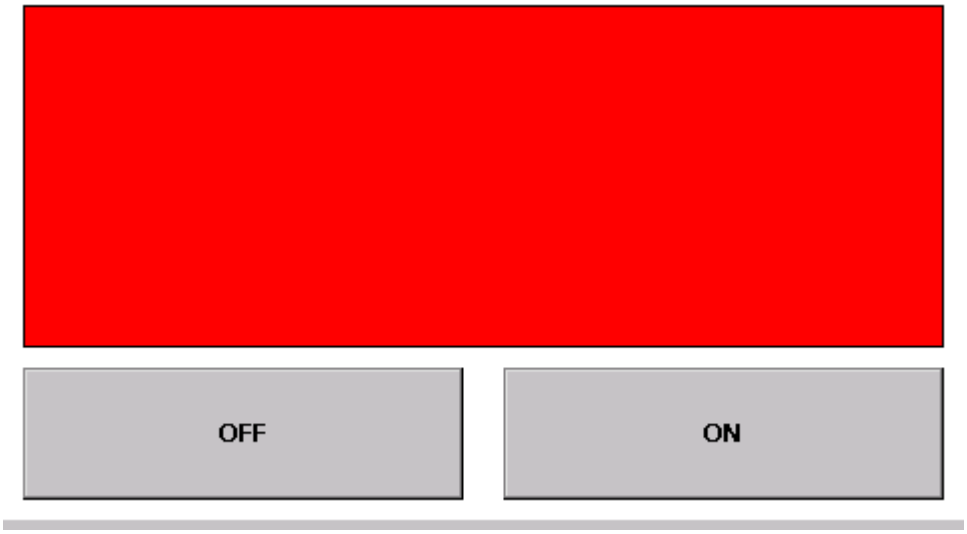

Figure 3.5: GPIO_Win32 Application Initial Screen Shot (LED OFF State)

NOTE: This sample application was originally written to drive GPIO_133 (LED D3), so an illuminated LED D3 signifies ON. However, if you are monitoring the GPIO_111 signal, you will notice a low signal for ON and a high signal for OFF. This is because the LED does not come on until the signal is driven low.

3.2.3 Use GPIO_111 as Input

The information above described how to drive GPIO_133 and GPIO_111. For a reference on how to use the API calls for accessing GPIOs as inputs, see GPIOGetIrq() routing in the

pwrkey.c source code found in Logic PD's DM37x Windows Embedded CE 6.0 BSP: (*PLATFORM\LOGIC_ARM_A8\SRC\DRIVERS\PWRKEY*).

To use GPIO_111 as an input, add the following line (that includes the *input_enable* parameter) to the *platform.c* file.

```
OUTREG16(&pConfig->CONTROL_PADCONF_CAM_XCLKB, (INPUT_ENABLE |
PULL_INACTIVE | MUX_MODE_4)); /*CAM_XCLKB*/
```

3.3 Configure GPIO Signals in Linux

This section describes how to access GPIO signals on the DM3730/AM3703 processor using Logic PD's DM37x Linux BSP version 1.0 or later. We will be using GPIO_111 in this example.

1. Locate the pin in the OMAP mux files by searching for the string `gpio_111` in the debug data provided by the kernel, then `grep` for the pin.

```
DM-37x# grep gpio_111 /debug/omap_mux/*

/debug/omap_mux/cam_xclkb:signals: cam_xclkb | NA | NA | NA | gpio_111
| NA | NA | safe_mode
```

   From this output, we find that */debug/omap_mux/cam_xclkb* is the file associated with the GPIO_111 pin.

2. Verify what mode the pin is in.

```
DM-37x# cat /debug/omap_mux/cam_xclkb

name: cam_xclkb.safe_mode (0x4800212e/0x0fe = 0x010f), b b26, t NA
mode: OMAP_PIN_INPUT_PULLDOWN | OMAP_MUX_MODE7
signals: cam_xclkb | NA | NA | NA | gpio_111 | NA | NA | safe_mode
```

3. Since the pin is in MODE7 (safe_mode), change it to MODE4 and then set GPIO_111 as an output. After making these changes, verify the pin is in the new mode.

```
DM-37x# echo 0x4 > /debug/omap_mux/cam_xclkb

DM-37x# cat /debug/omap_mux/cam_xclkb

name: cam_xclkb.gpio_111 (0x4800212e/0x0fe = 0x0004), b b26, t NA

mode: OMAP_PIN_OUTPUT | OMAP_MUX_MODE4

signals: cam_xclkb | NA | NA | NA | gpio_111 | NA | NA | safe_mode
```

4. Now we can use the *gpiolib* interface to manipulate the pin.

```
DM-37x# echo 111 > /sys/class/gpio/export
```


3.3.1 GPIO Output

Note that the steps above created a */sys/class/gpio/gpio111* directory and populated it with files to allow us to manipulate the pin.

1. Now we can set it as an output.

```
DM-37x# echo out > /sys/class/gpio/gpio111/direction
```

2. We can set it high.

```
DM-37x# echo 1 > /sys/class/gpio/gpio111/value
```

3. And we can set it low.

```
DM-37x# echo 0 > /sys/class/gpio/gpio111/value
```

3.3.2 GPIO Input

The GPIO_111 pin can be configured as an input in the GPIO controller. This requires changing the pin mux value that was previously set. "Chapter 13.4.4: Pad Functional Multiplexing and Configuration" in the *AM/DM37x Multimedia Device TRM* provides details on how to set up the pin as an input with pull-up.

1. First, set the following bits: bit 8 (INPUTENABLE), bit 4 (PULLTYPESELECT) and bit 3 (PULLUDENABLE). Then set bits 2 through 0 representing MODE4 (GPIO). This will change the pin to OMAP_PIN_INPUT_PULLUP | OMAP_MUX_MODE4.

```
DM-37x# echo 0x11c > /debug/omap_mux/cam_xclkb

DM-37x# cat /debug/omap_mux/cam_xclkb

name: cam_xclkb.gpio_111 (0x4800212e/0x0fe = 0x011c), b b26, t NA
mode: OMAP_PIN_INPUT_PULLUP | OMAP_MUX_MODE4
signals: cam_xclkb | NA | NA | NA | gpio_111 | NA | NA | safe_mode
```

2. Next, reverse the direction.

```
DM-37x# echo in > /sys/class/gpio/gpio111/direction
```

3. Check its value.

```
DM-37x# cat /sys/class/gpio/gpio111/value

1
```

Since the pin mux is set up with a pull-up, the value will be 1.

4. Ground the pin (J17.36 on the breakout board) and check the value again.

```
DM-37x# cat /sys/class/gpio/gpio111/value
```



```
0
```

5. Finally, free the pin.

```
DM-37x# echo 111 > /sys/class/gpio/unexport
```

Note that */sys/class/gpio/gpio111* is no longer there.

3.4 Configure GPIO Signals in Android

For information about how to configure GPIO signals in Android, please see the document below that is appropriate for your system:

- *AN 494 DM37x Android Froyo 2.2 GPIO Demo*[13]
- *AN 531 DM3730/AM3703 Android Gingerbread 2.3.4 GPIO Demo*[14]

4 Summary

This application note provided assistance with using GPIO signals on the DM3730/AM3703 SOMs. If you have any questions concerning this or any other Logic PD documentation, please contact Logic PD.[15]

[13] http://support.logicpd.com/downloads/1459/
[14] http://support.logicpd.com/downloads/1535/
[15] http://support.logicpd.com/support/askaquestion.php

Appendix A: Configure TPS65950 PMIC Signal as GPIO

Configuring GPIOs on the TPS65950 is a bit more complex than configuring the DM3730/AM3703 processor GPIOs. The TPS65950 requires access through the I2C and then access to the GPIO control registers within the TPS65950. The example below that shows how to enable and drive LCD_DON high can easily be modified to access any other GPIO or register within the TPS65950.

The following script programs the TPS65950 GPIO.1 to output high or low. This signal connects to pin J1.153 on the DM3730/AM3703 SOM-LV, signal ICT_JTAG_TMS (LCD_DON). LCD_DON is connected to J18.52 on the breakout board. **NOTE:** The TPS65950 GPIO.1 signal does not go external of the DM3730/AM3703 Torpedo SOM or DM3730/AM3703 Torpedo + Wireless SOM.

```
#TPS95650 is attached to I2C1
#I2C1 base address is 0x48070000
#Bitrate is 2.6 MHz
#High speed mode
#Procedure for setting LCD_DON to high

#Set GPIO_ON(bit 2), clear GPIO1CD2(bit1) in GPIO_CTRL,
#register 0xAA, address_group 0x49, data 0x4
losh> w /b 0x004900AA 0x04 /dev/pm0

#Set GPIO1OUT to HIGH in SETGPIODATAOUT1,
#register 0xA4, address_group 0x49, data 0x2
losh> w /b 0x004900A4 0x02 /dev/pm0

#Set GPIO1DIR to HIGH in GPIODATADIR1,
#register 0x9B, address_group 0x49, data 0x2
losh> w /b 0x0049009b 0x02 /dev/pm0
```

To change the script so it sets LCD_DON low, change the write-to SETGPIODATAOUT1 to CLEARGPIODATAOUT1 like this:

```
#Set GPIO1OUT to HIGH in CLEARGPIODATAOUT1,
#register 0xA1, address_group 0x49, data 0x2
losh> w /b 0x004900a1 0x02 /dev/pm0
```

If you need to read a TPS65950 GPIO as an input within LogicLoader, or use TPS65950 GPIOs within Windows CE or Linux, contact Logic PD and we can work with you to create a suitable script.

Appendix B: Enabling VPLL2

LogicLoader I2C Commands

The following commands in LogicLoader will enable VPLL2 to output 1.8V, making accessible GPIOs that are powered by VPLL2.

```
losh> x /b 0x004b008E 1 /dev/pm0      # read VPLL2_DEV_GRP silicon
register 0x8E of the PMIC chip device ID 0x4b (address_group) Should
return 0x0

losh> x /b 0x004b0091 1 /dev/pm0      # read VPLL2_DEDICATED silicon
register 0x91 of the PMIC chip device ID 0x4b (address_group) Should
return 0x3

losh> w /b 0x004b0091 0x5 /dev/pm0    # write 0x5 (data) to
VPLL2_DEDICATED silicon register 0x91 of the PMIC chip device ID 0x4b
(address_group) Set VPLL2 voltage to 1.8V

losh> w /b 0x004b008E 0x2e /dev/pm0   # write 0x2e (data) to
VPLL2_DEV_GRP silicon register 0x8E of the PMIC chip device ID 0x4b
(address_group) Enable VPLL2
```

Linux I2C Commands

The following commands can be run from the Linux prompt to enable VPLL2 at 1.8V.

```
DM-37x# i2cset -f -y 1 0x4b 0x91 0x5
DM-37x# i2cget -f -y 1 0x4b 0x91
0x05
DM-37x# i2cset -f -y 1 0x4b 0x8e 0x2e
DM-37x# i2cget -f -y 1 0x4b 0x8e
0x2e
```