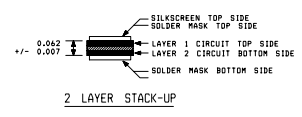
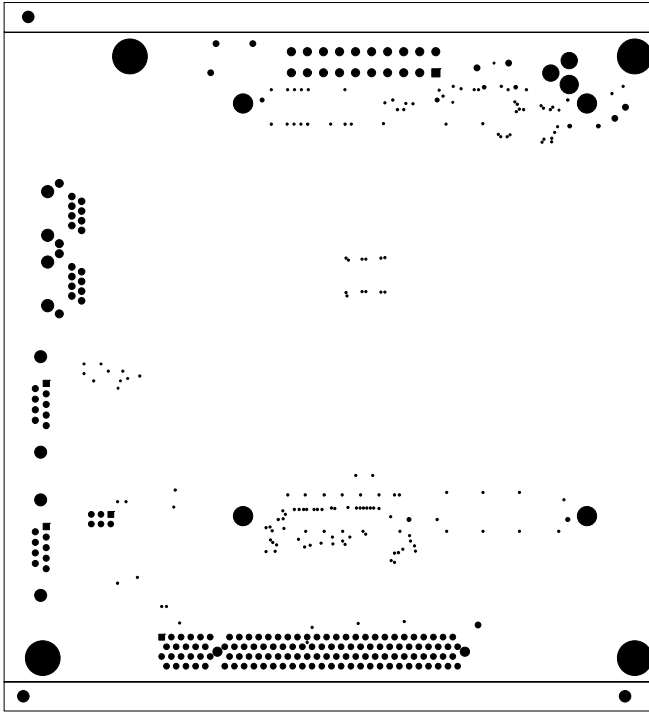


- NOTE:
- MATERIAL SELECTION:  
2 LAYER, EPOXY GLASS, NEMA GRADE FR-4, 0.062 +/- 0.007 THICK.  
0.5 OZ. MINIMUM COPPER CLADDING WITH SMOBC.
  - FINISH ON ALL SOLDERABLE SURFACES TO BE:  
X ENTEK SELECTLESS NICKEL (IMMERSION GOLD) - (GOLD BODY).  
□ DSP - ENTEK PLUS 106A.  
□ WHITE TIN.
  - SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR - BLUE. USE LIQUID PHOTOIMAGABLE RESIST.
  - SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND TESTPOINT LANDS ARE TO BE FREE OF INK.
  - MANUFACTURER'S IDENTIFICATION: ADD TO SILKSCREEN TOP SIDE.
  - ELECTRICAL BARE BOARD TEST REQUIRED.
  - DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
  - BOARD TO BE SCORED AT DESIGNATED LINE, SCORING TO BE 30 DEG. AND A MINIMUM OF 0.015 INCHES BOARD MATERIAL IN CHANNEL.
  - THE PRINTED CIRCUIT BOARDS MANUFACTURED TO THIS DRAWING MUST BE ROHS COMPLIANT. LAMINATE AND PREPREG SHALL BE POLYCLAD 370HR. ALTERNATIVE MATERIAL MUST BE APPROVED BY LOGIC/MDC PRIOR TO USE.



DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
△	0.010	+/- 0.003	10	PLATED
x	0.012	+/- 0.003	152	PLATED
◇	0.020	+/- 0.003	4	PLATED
■	0.028	+/- 0.003	4	NON-PLATED
○	0.035	+/- 0.003	32	PLATED
∞	0.040	+/- 0.003	150	PLATED
●	0.043	+/- 0.003	18	PLATED
⊗	0.043	+/- 0.003	4	NON-PLATED
+	0.055	+/- 0.003	20	PLATED
+	0.064		4	
□	0.096	+/- 0.003	2	PLATED
○	0.098	+/- 0.003	4	PLATED
⊖	0.120	+/- 0.003	2	PLATED
⊖	0.125	+/- 0.003	4	PLATED
■	0.125	+/- 0.003	4	NON-PLATED
⊖	0.128	+/- 0.003	4	NON-PLATED
⊖	0.140	+/- 0.003	1	PLATED
TOTAL			419	

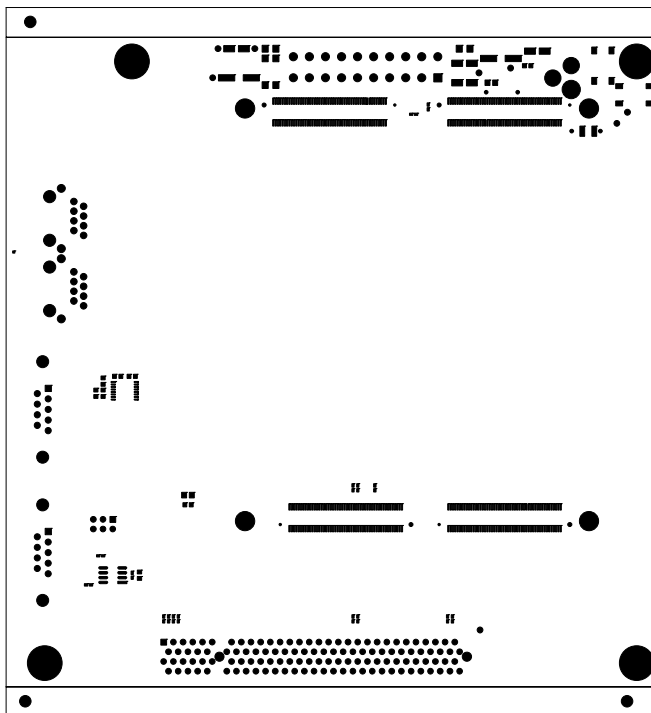
DRILL



ASIC PRODUCT DEVELOPMENT  
100457 REV. A  
03-23-04

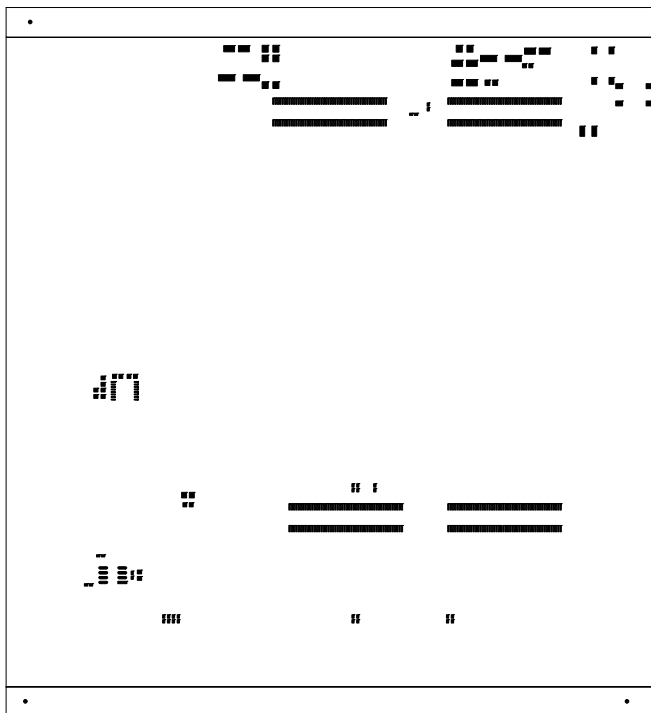
HOLDER MARK BOTTOM SIDE





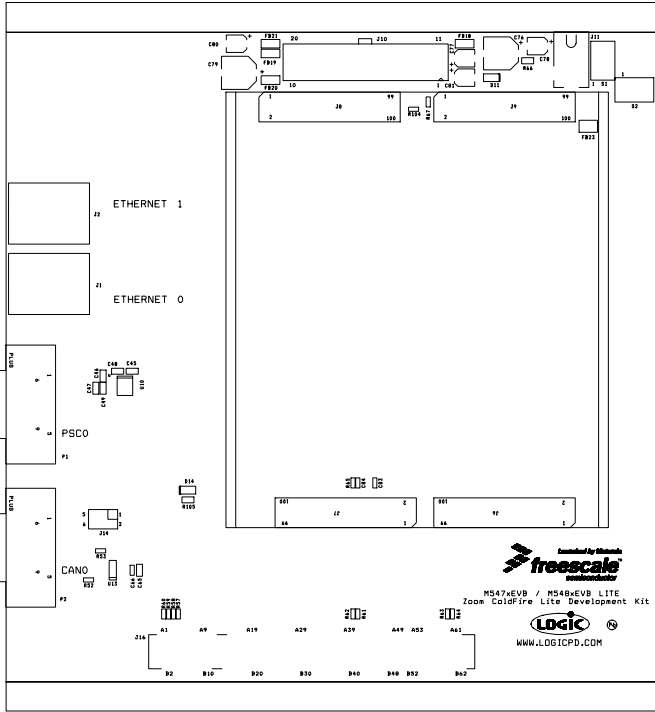
ASIC PRODUCT DEVELOPMENT  
000001 REV. A  
03-23-06

SOLDER MASK TOP SIDE



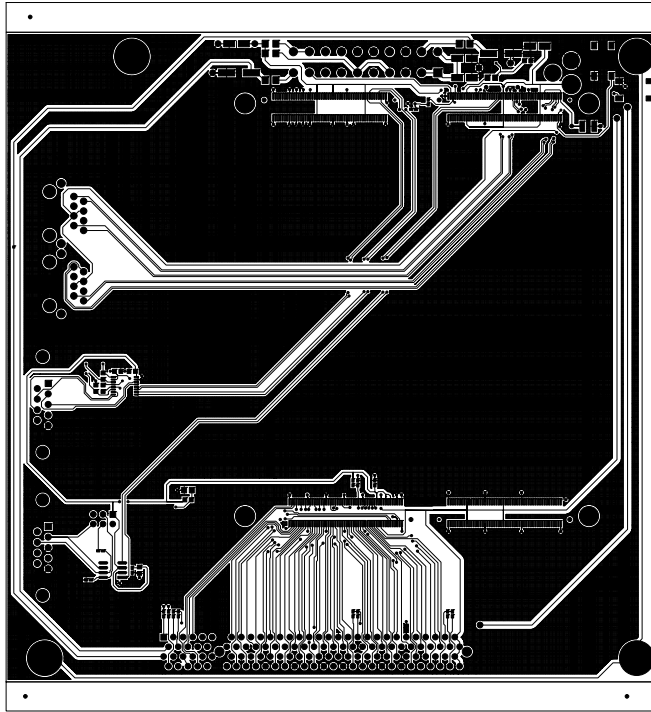
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03-23-04

SOLDERPART TOP SIDE



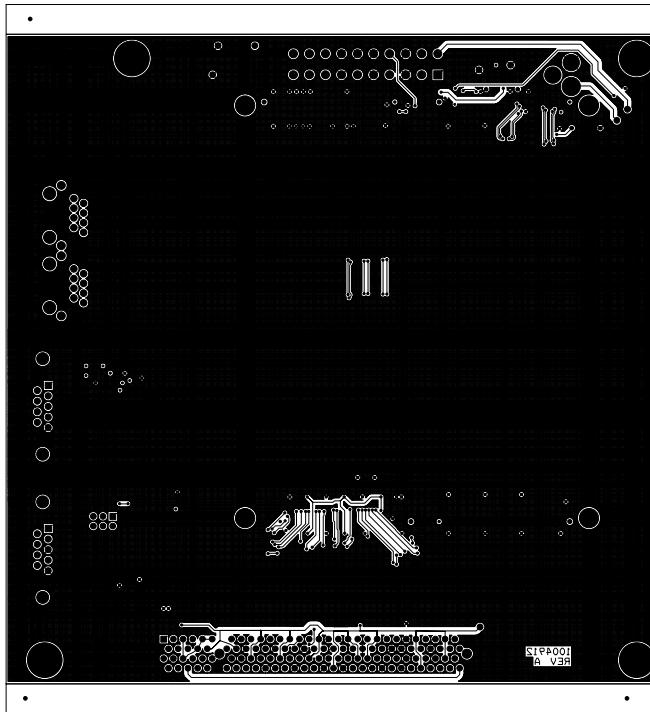
LOGIC PRODUCT DEVELOPMENT  
 10044171 REV. A  
 03-23-06

SILKSCREEN TOP SIDE



ASIC PRODUCT DEVELOPMENT  
004612 REV. A  
03-23-06

LAYER 1 CIRCUIT TOP SIDE



ASIC PRODUCT DEVELOPMENT  
000001 REV A  
03-23-06

LAYER 2 CIRCUIT BOTTOM SIDE