

PROJECT:	SDK-DRG -10
PART NUMBER:	1001660
ASSEMBLY NAME:	MCF53xx SDK
SCHEMATICS:	ECR, KTL

01 - TITLE PAGE

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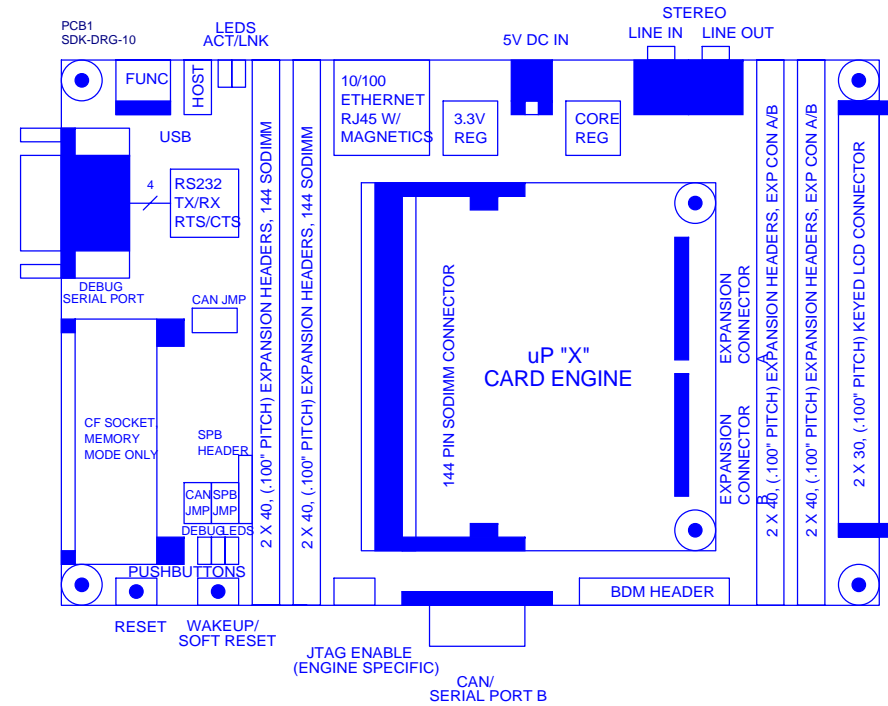
COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES

LAYOUT NOTE:
NOTES IN RED TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDELINES

NET NAMES
NET NAMES IN GREEN TEXT ARE NETS THAT ARE NOT DIRECTLY CONNECTED WITH A VISIBLE WIRE ON SINGLE SCHEMATIC PAGE, BUT USE THIS CONVENTION TO MAKE THE SCHEMATIC EASIER TO READ

NET NOTE
NET NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC NET, IT IS NOT A NET NAME MERELY TEXT AND HAS NO AFFECT ON THE DRC.



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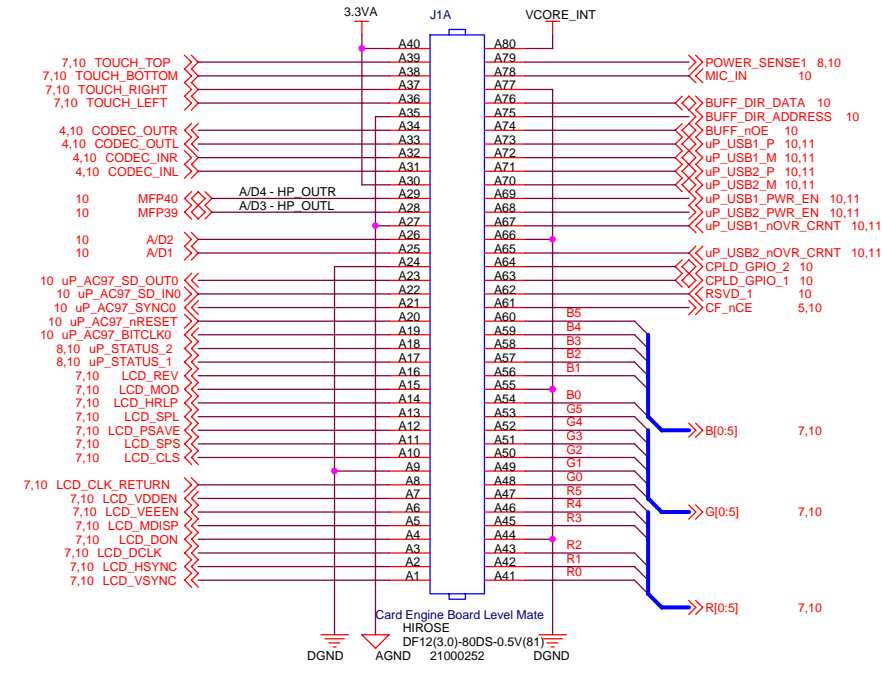
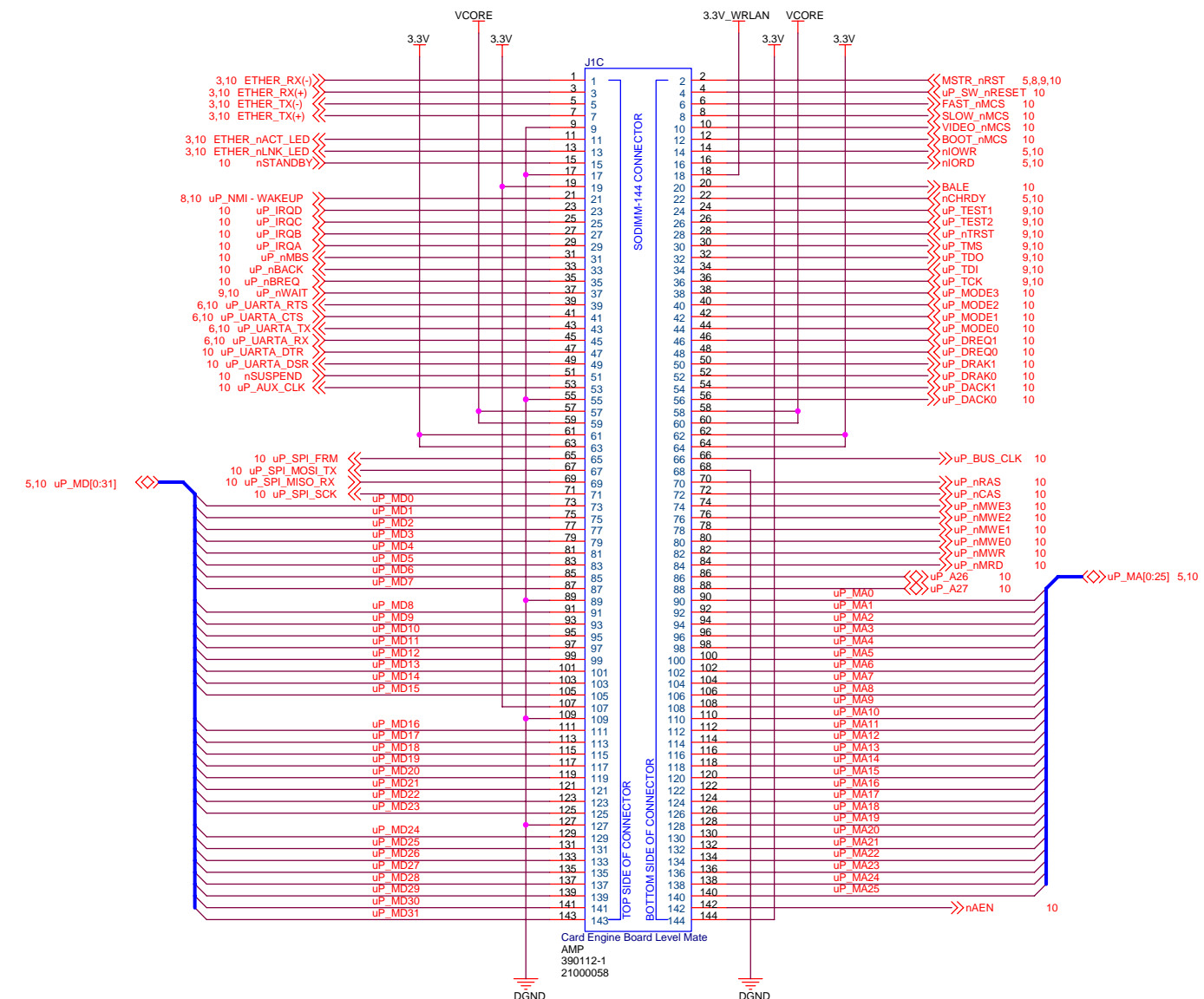
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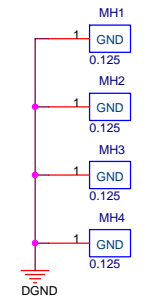
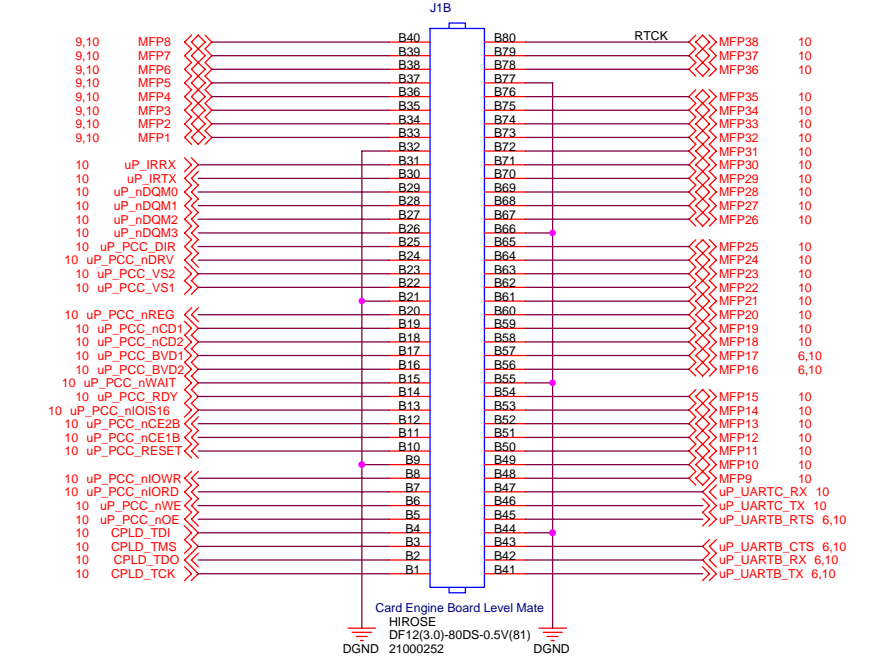
	LOGIC PRODUCT DEVELOPMENT		411 WASHINGTON AVE. N MINNEAPOLIS, MN 55401 PHONE: (612) 672-9495 FAX: (612) 672-9489
	Title Zoom SDK Application Board		
Size C	Number 1001660	Rev 7	
Design Create Date = Monday, July 01, 2002		Project SDK-DRG - 10	Sheet 1 Of 12

02 - EXPANSION BUS

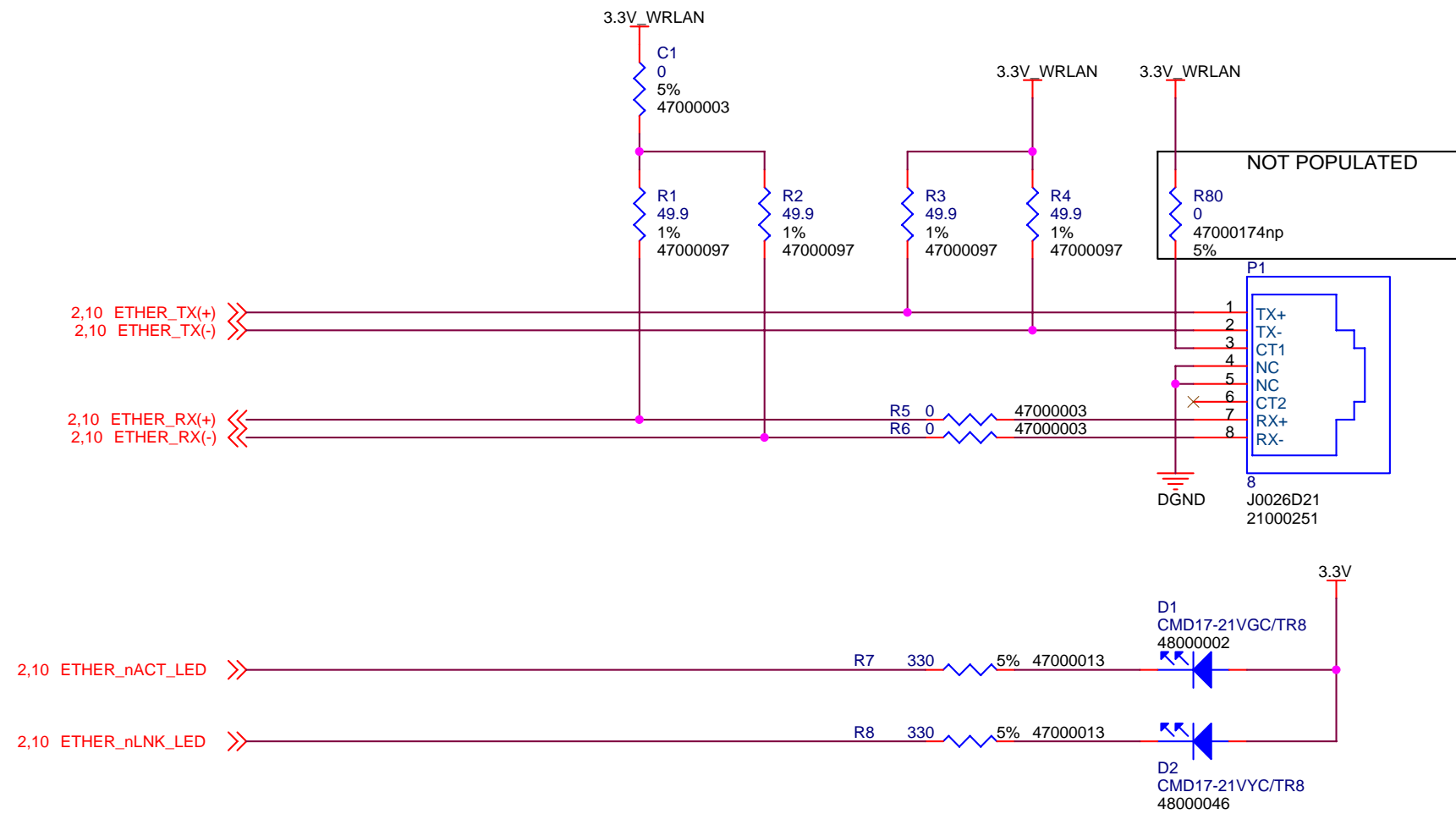
NOTE:
NOT ALL CARD ENGINES WILL HAVE ALL THESE SIGNALS, PLEASE SEE SPECIFIC CARD ENGINE HARDWARE SPEC FOR DETAILED PINOUT AND SIGNAL INFORMATION.



NOTE:
REFER TO THE PROCESSOR CARD ENGINE PINOUT PAGES (7, 10) FOR LCD DATA SIGNALS. THE DATA SIGNALS ARE SETUP FOR AN 18 BIT TFT INTERFACE. FOR SUPPORT OF OTHER DISPLAY TYPES, REFER TO THE LCD PINOUT TABLE IN THE CARD ENGINE HARDWARE SPECIFICATION MANUAL.




03 - ENGINE ETHERNET



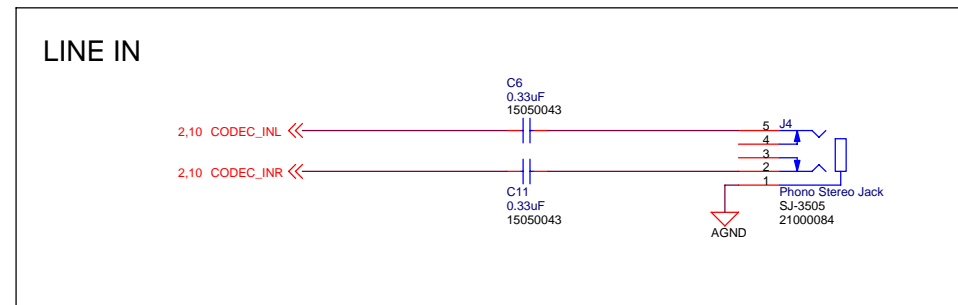
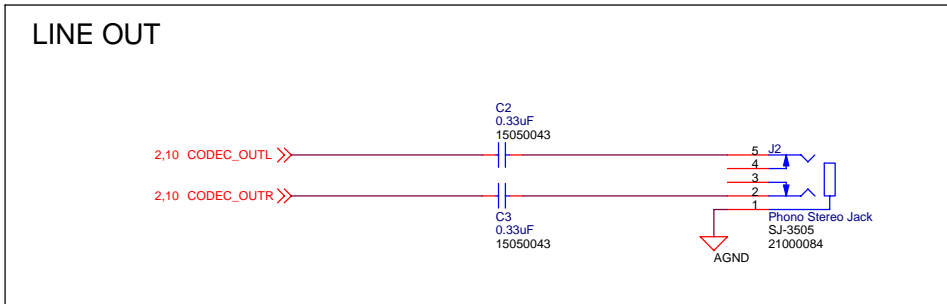
REVISIONS 4->5

1. CHANGED VALUES OF R1, R2, R5, R6, C1

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04 - AUDIO



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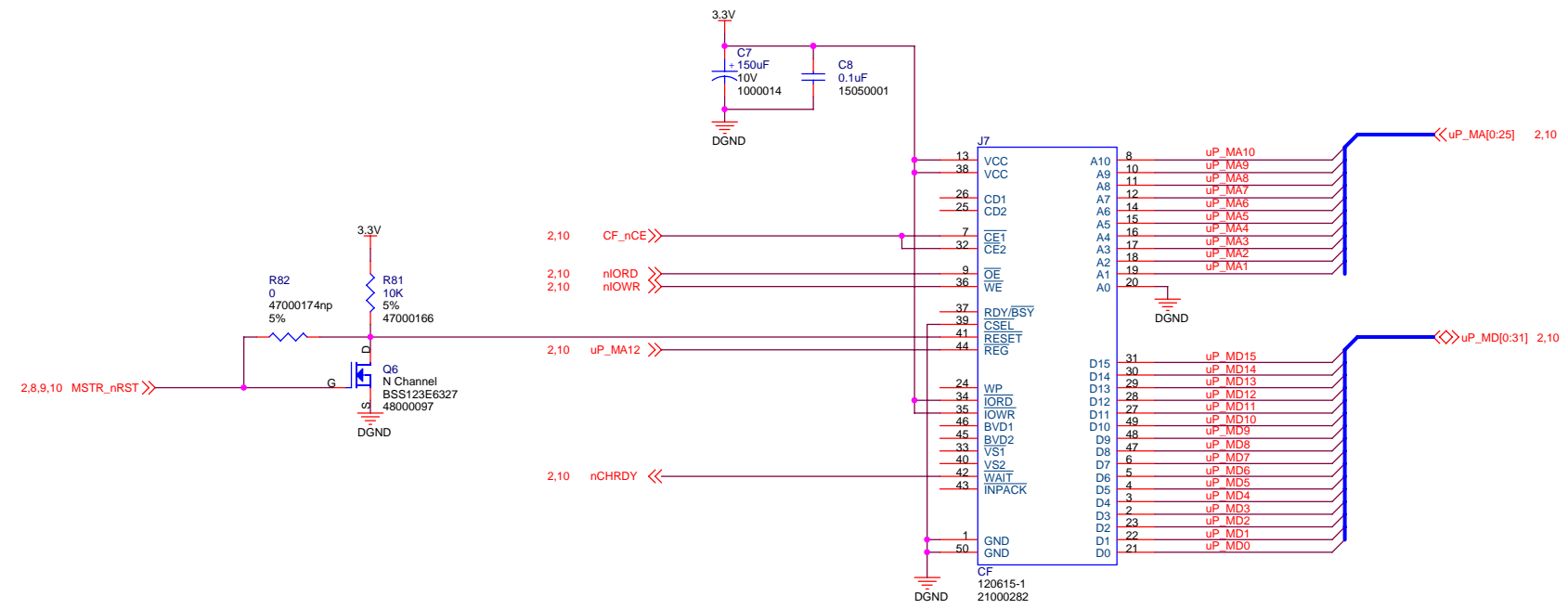


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COMPACT FLASH
SOCKET MEMORY
MODE ONLY



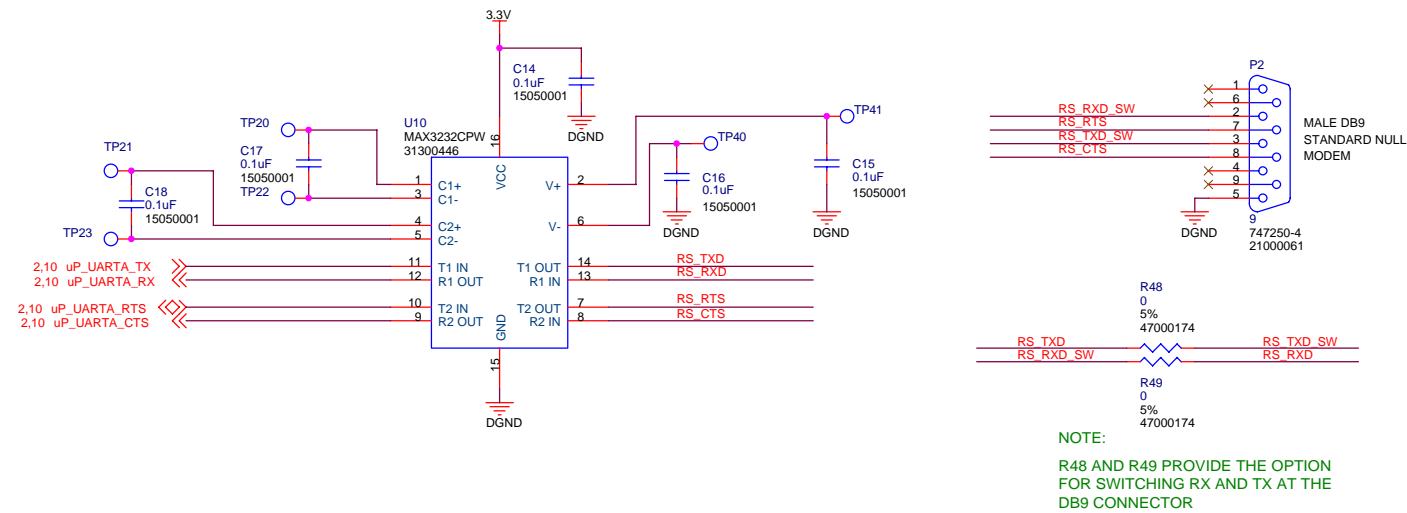
REVISIONS 2->3:

- 1. CHANGED C7 TO 1000014 (WAS 15150011)

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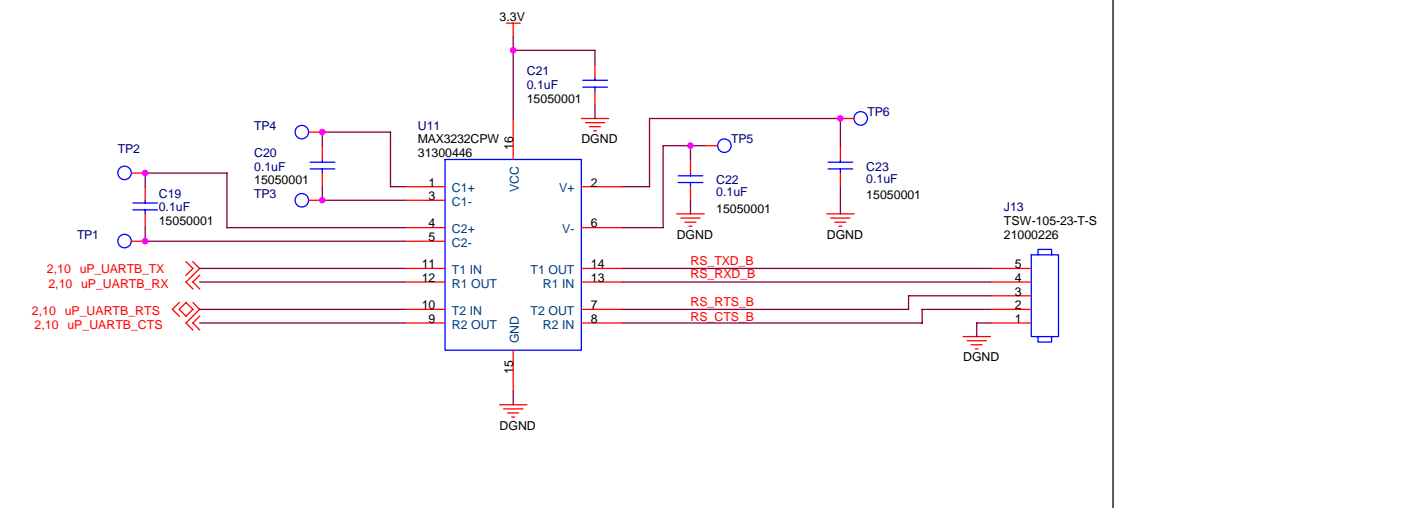
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UART A

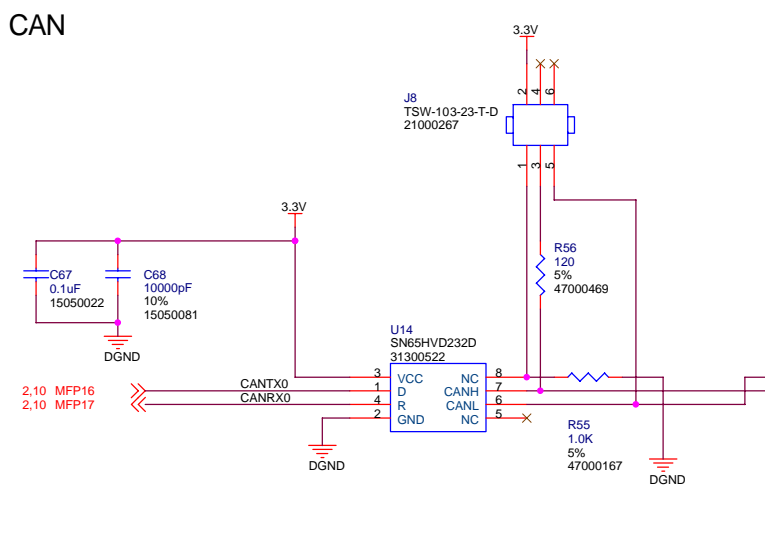


06 - RS232, CAN

UART B

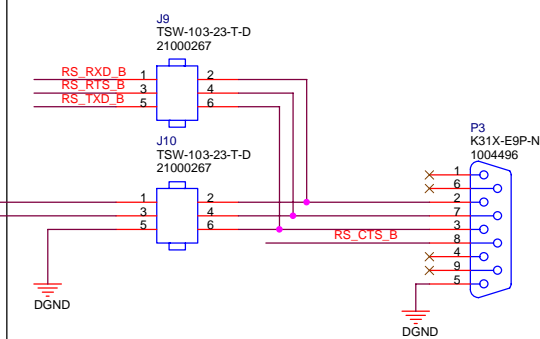


CAN



CAN/UARTB DB9 SELECTION

PLACE 3 JUMPERS ON J9 PINS 1-2, 3-4, 5-6 TO SELECT UARTB. OR PLACE 3 JUMPERS ON J10 PINS 1-2, 3-4, 5-6 TO SELECT CAN. DO NOT PUT JUMPERS ON U9 AND J10 SIMULTANEOUSLY.

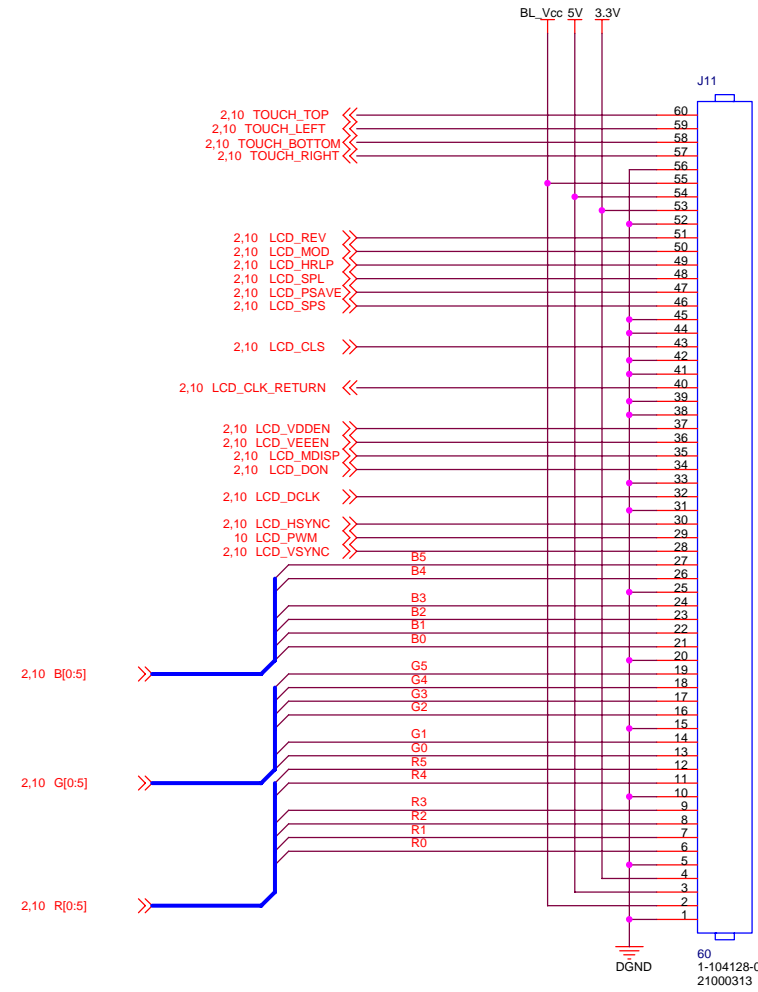


REVISIONS 5->6:
1. Changed P3 part number

REVISIONS 6->7:
1. Added ground to pin 5 of P3

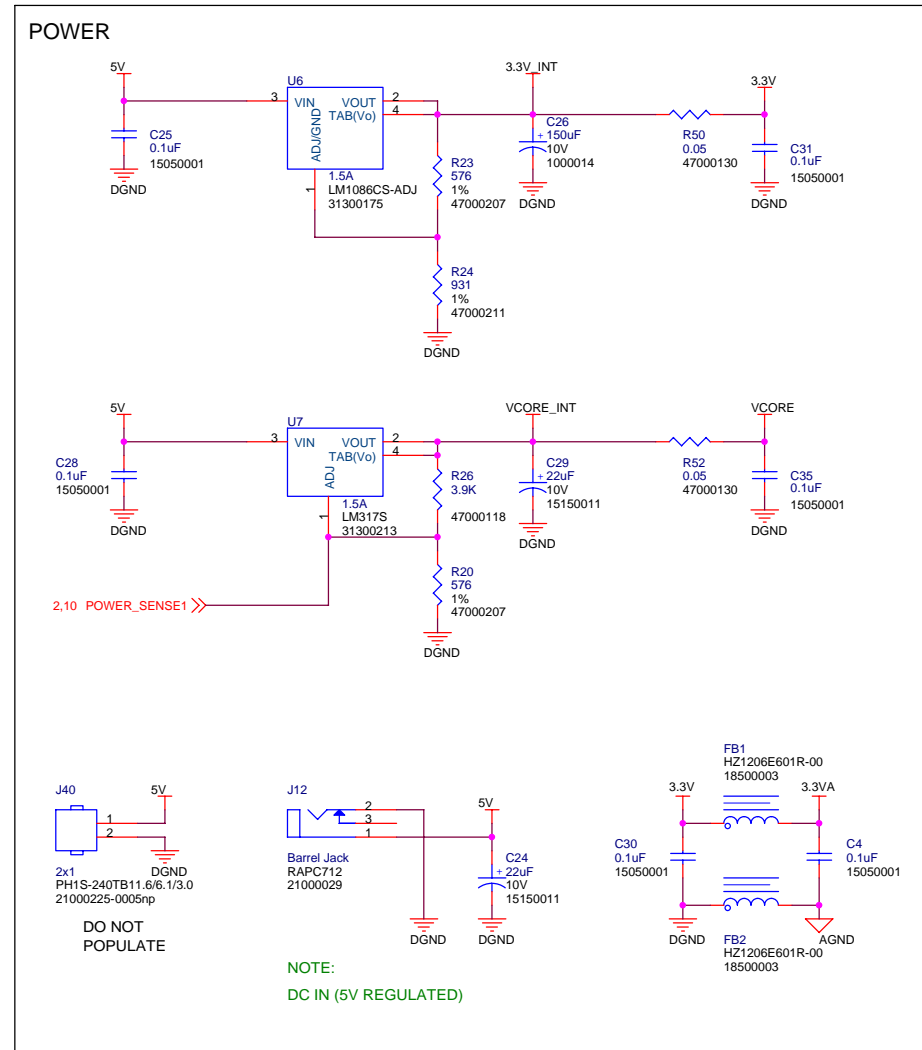
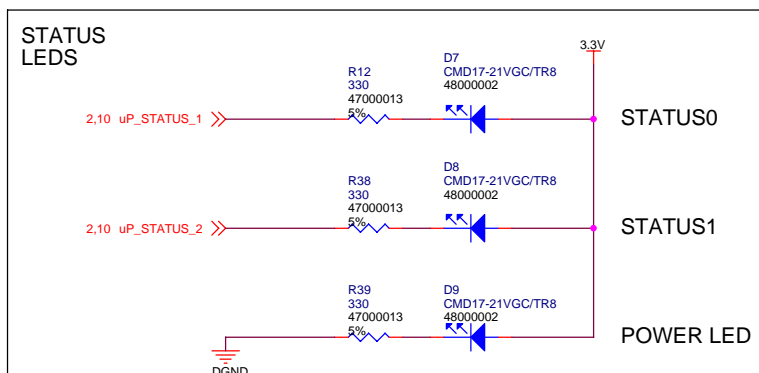
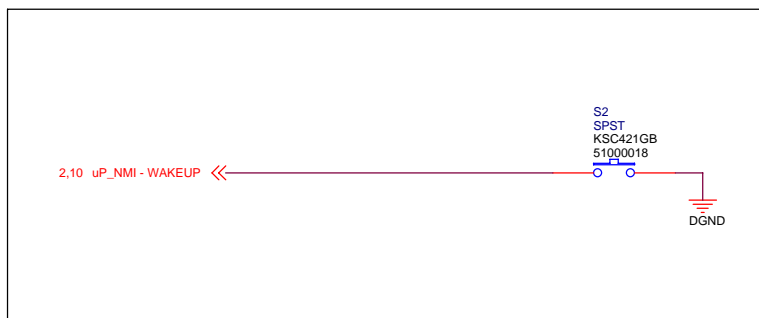
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NOTE:
THE NET BL_Vcc IS CONNECTED
TO A 2PIN HEADER J40 ON PAGE
8.



NOTE:
THIS CONNECTOR IS ACTUALLY A 30X2 DUAL ROW .100" PITCH, .025" SQ POST MALE
HEADER. IT IS REPRESENTED SYMBOLICALLY AS A SINGLE ROW CONNECTOR TO
ILLUSTRATE HOW THE SIGNALS WILL ROUTE THROUGH THE RIBBON CABLE.

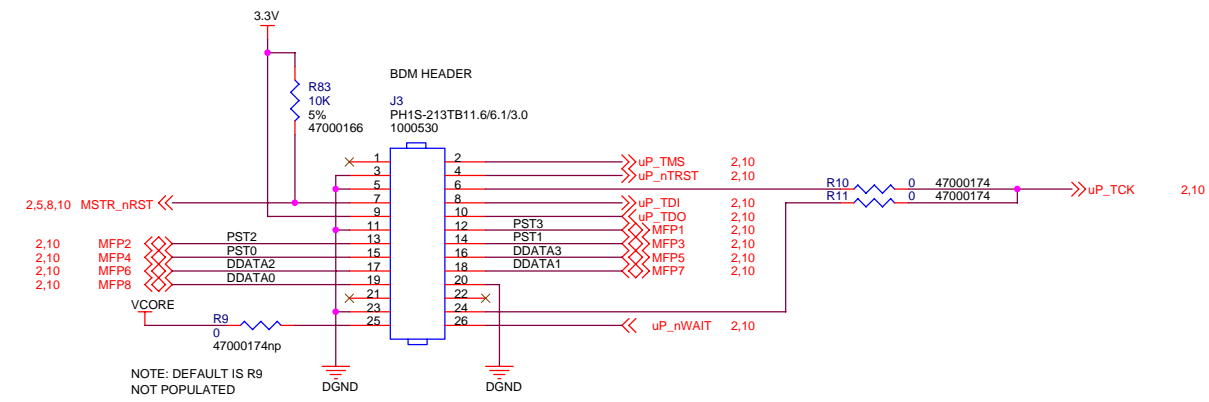
NOTE:
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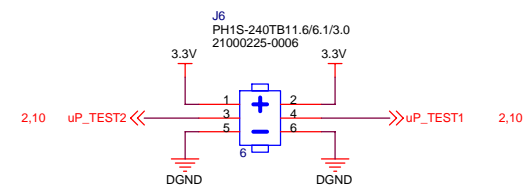
- REVISIONS 2->3:
1. CHANGED C26 TO 1000014 (WAS 15150011)
2. CHANGED S1 & S2 TO 51000018

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IMPORTANT NOTE: ONLY 3.3V BDM debugging cables can be used with MCF53xx processors.



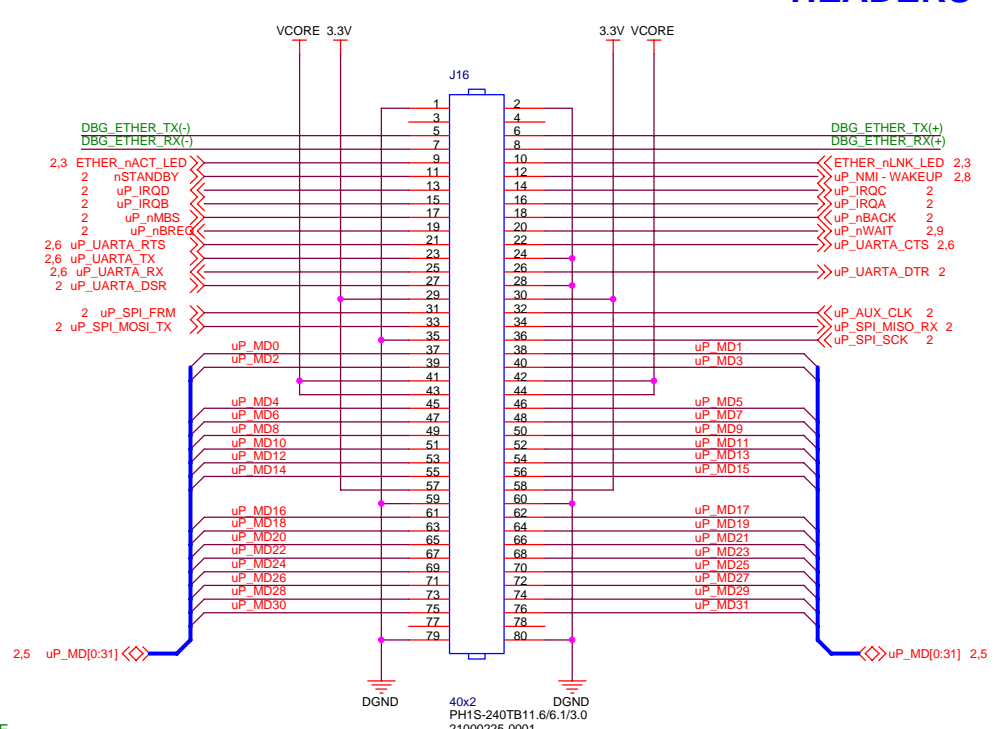
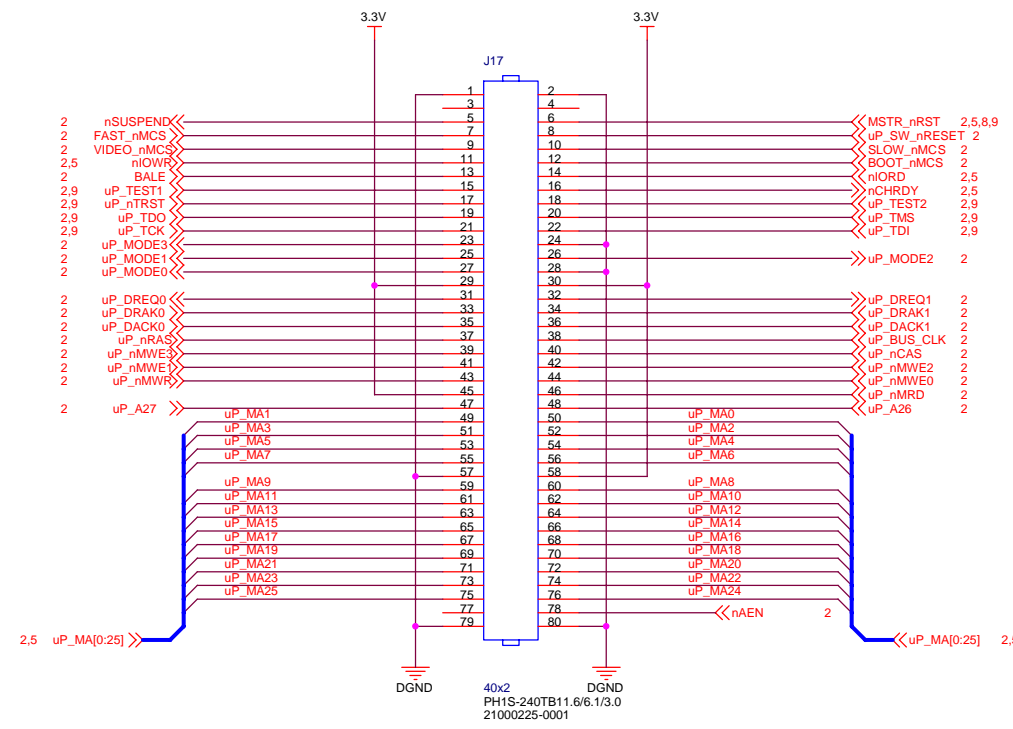
REVISIONS 3->4:

- TIED J3 PIN 7 TO MSTR_nRST

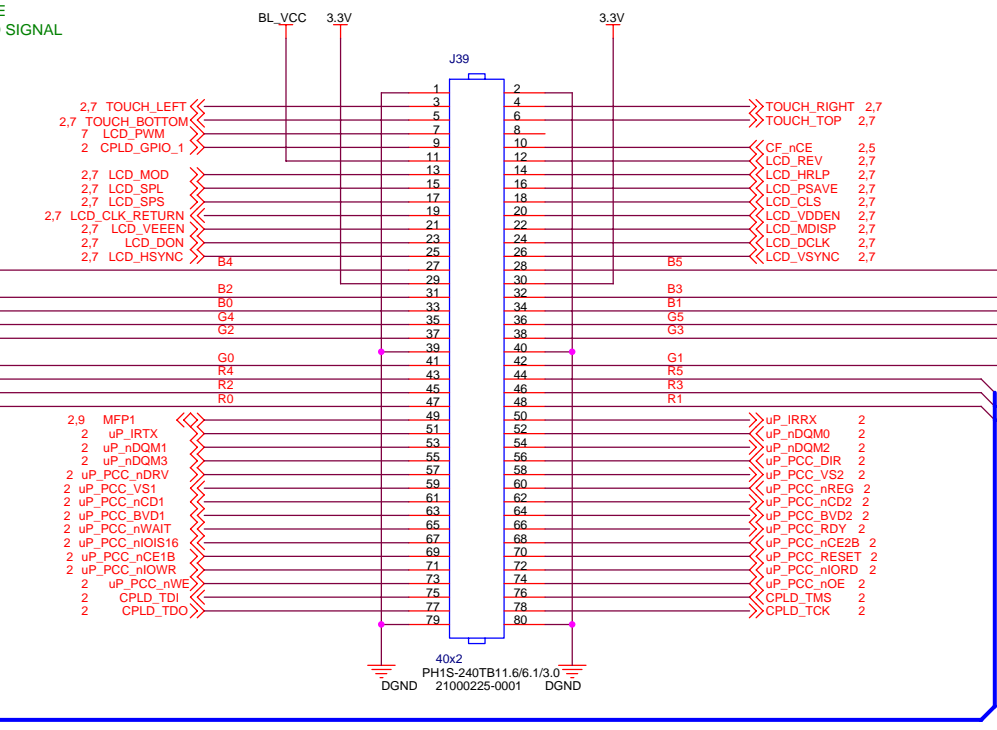
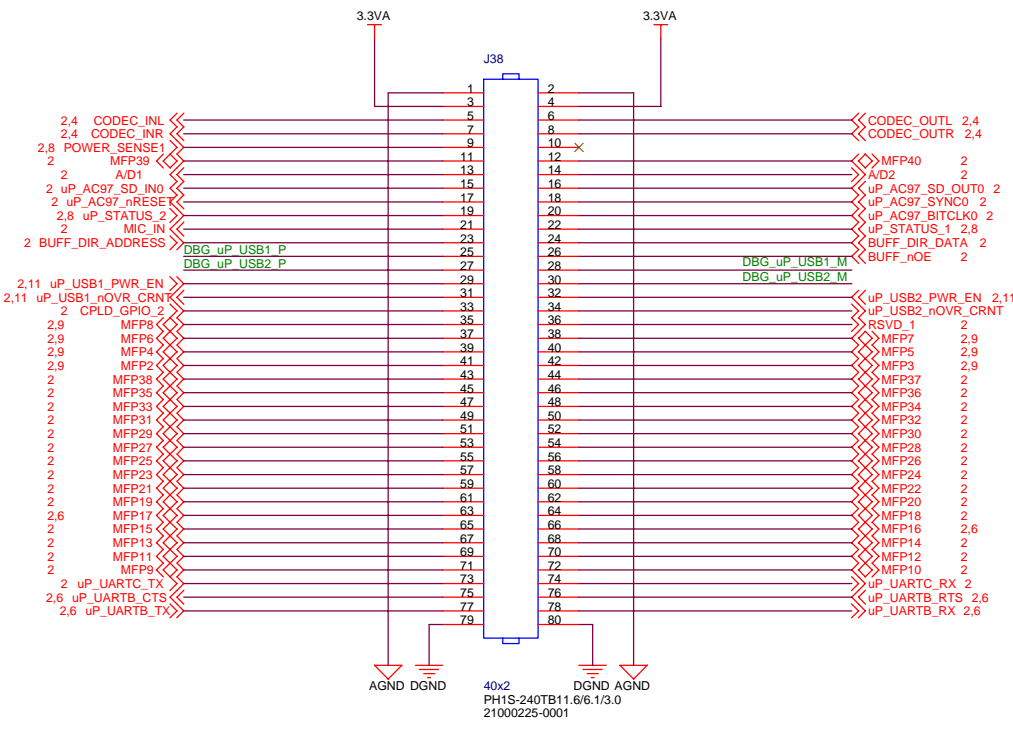
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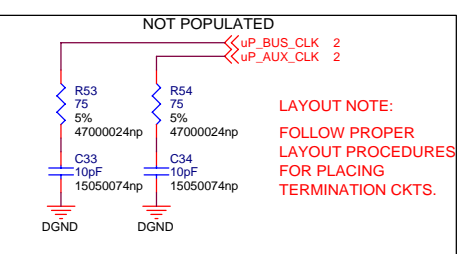
10 - EXPANSION/DEBUG HEADERS



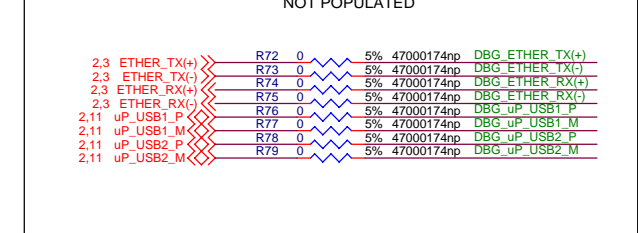
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TERMINATIONS



DIFF PAIRS TO DEBUG HEADERS



NOTE:
THE SDK SHIPS STANDARD WITH THESE RESISTORS NOT POPULATED TO MAKE THE CONNECTION TO THE EXPANSION HEADERS, POPULATE R72 - R79.

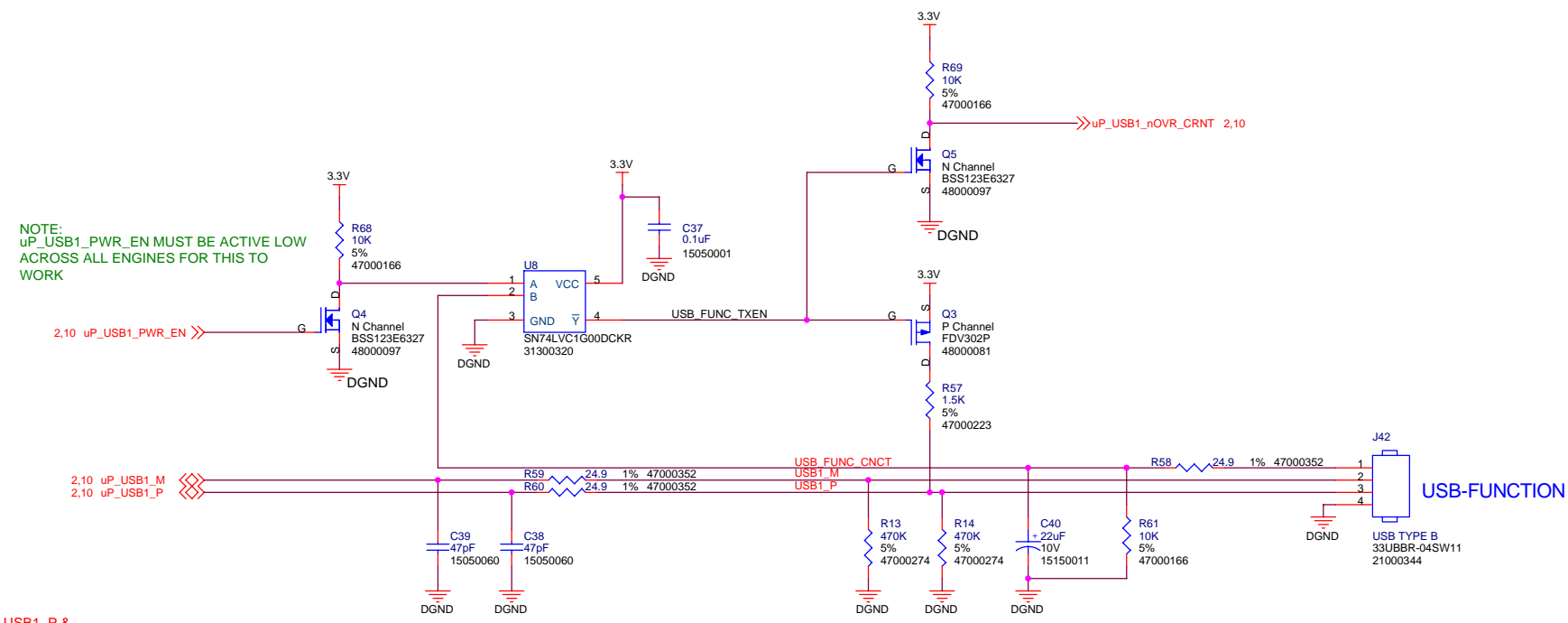
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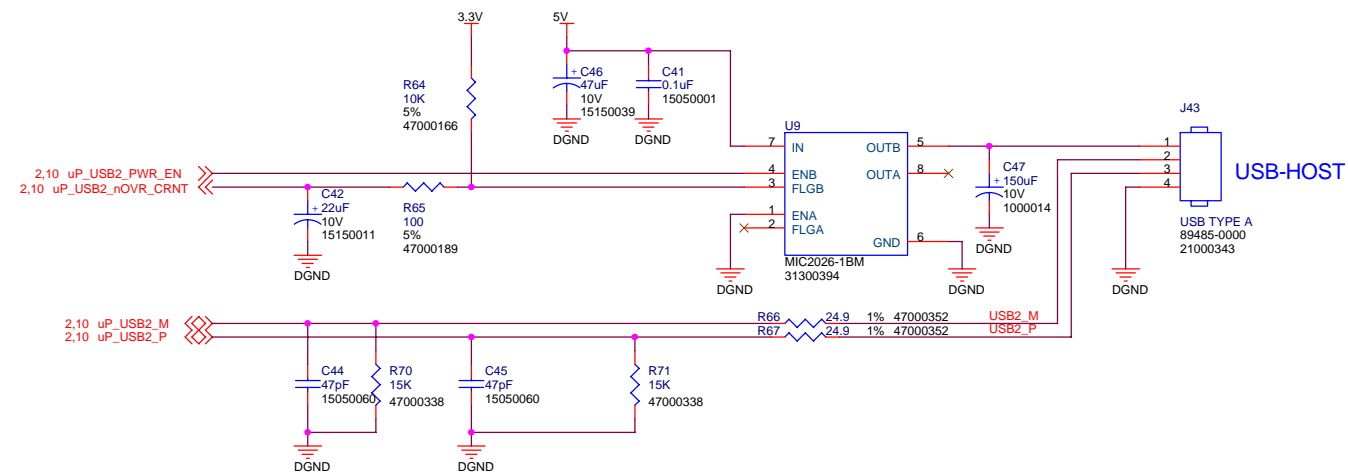
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11 - USB HOST, FUNCTION



LAYOUT NOTE:
THE USB DIFFERENTIAL PAIRS USB1_M, USB1_P &
USB2_M, USB2_P NEED TO BE ROUTED SUCH
THAT THEY HAVE A DIFFERENTIAL IMPEDENCE OF
90 OHMS.



REVISIONS 2->3:

1. ADDED R13 AND R14.


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12 - ECO LIST

Revision Control			
ECO Number	Rev	Description of Change	Date
	1	PRELIMINARY SCHEMATICS	03/24/05
	2	Design review corrections completed	04/14/05
	3	Added MFG/Logic part numbers to all parts	05/26/05
C02020	4	Tied MSTR_nRST to J3 pin 7	11/10/05
C02085	5	Updated ethernet circuit.	12/1/05
C02258	6	Updated P3 part number	01/25/06
C02316	7	Added P3 pin 5 to GND	02/10/06

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