01 - TITLE PAGE

PROJECT:	MCF5373-10 CARD ENGINE
PART NUMBER:	1002736
ASSEMBLY NAME:	MCF5373-10 CARD ENGINE
SCHEMATICS:	KTL

TABLE OF CONTENTS

COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES

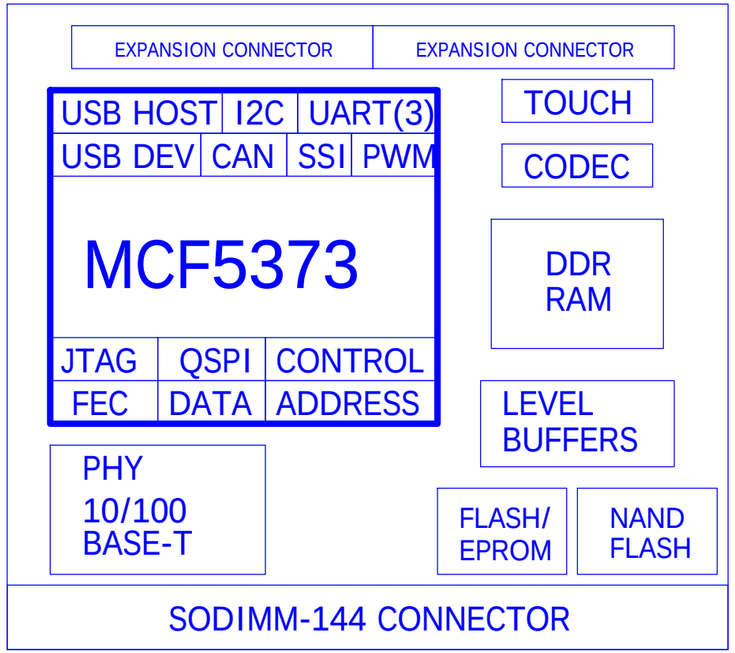
LAYOUT NOTE:
NOTES IN RED TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDLINES

NET NAMES

NET NAMES IN GREEN TEXT ARE NETS THAT ARE NOT DIRECTLY CONNECTED WITH A VISIBLE WIRE ON SINGLE SCHEMATIC PAGE, BUT USE THIS CONVENTION TO MAKE THE SCHEMATIC EASIER TO READ

NET NOTE

NET NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC NET, IT IS NOT A NET NAME MERELY TEXT AND HAS NO AFFECT ON THE DRC.



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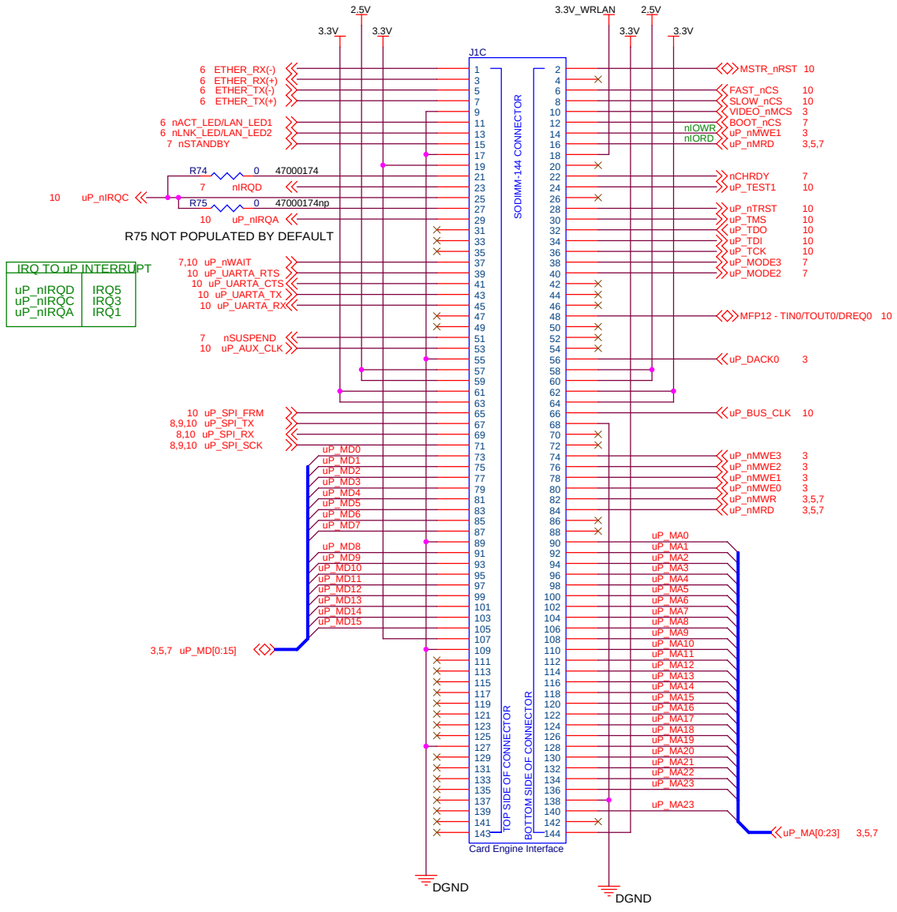
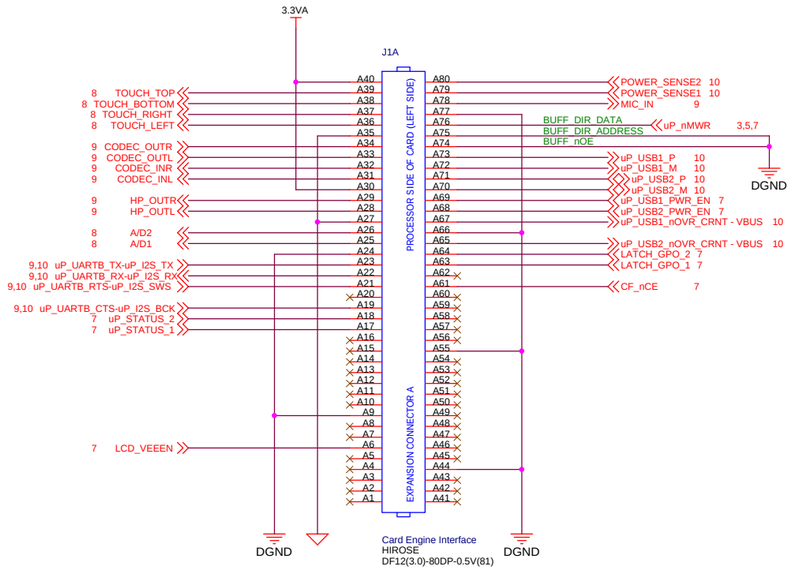
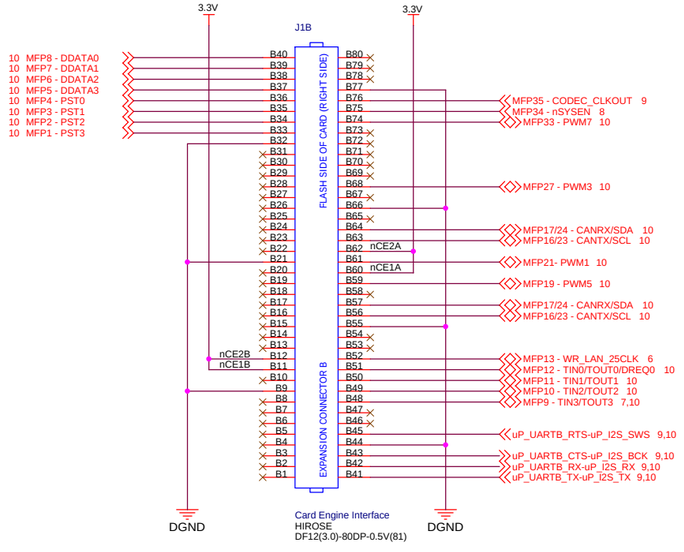
02 - EXPANSION BUS







NOTE: UARTB AND AUDIO INTERFACE
CANNOT BE USED SIMULTANEOUSLY

Schematic Modify Date = Tuesday, March 20, 2007
Design Create Date = Friday, October 18, 2002

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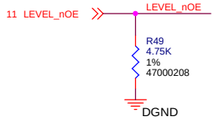
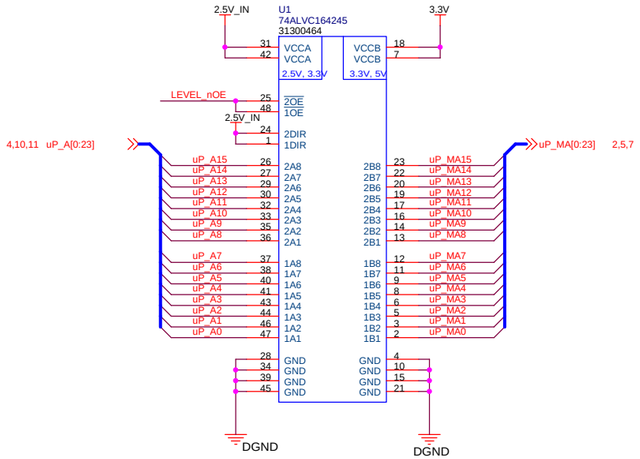
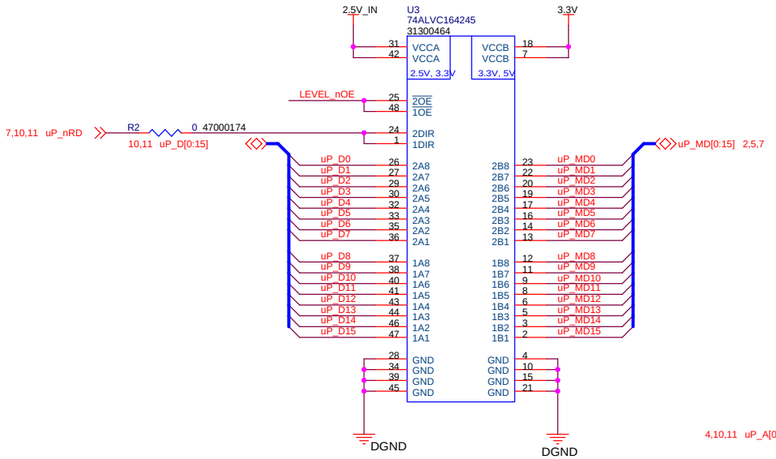
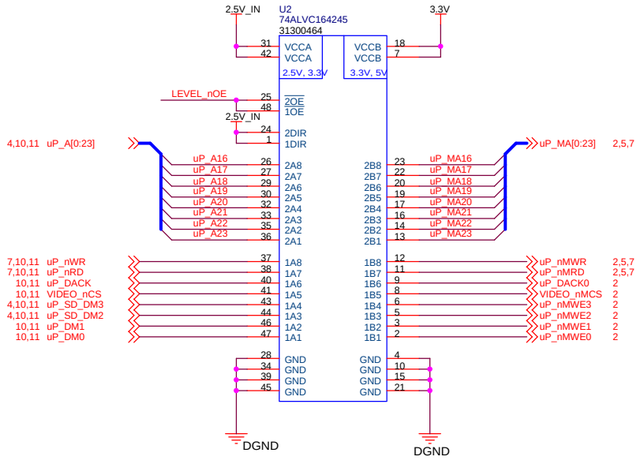
03 - BUFFERS

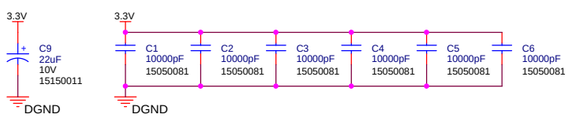


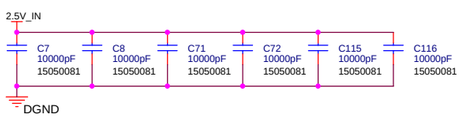






NOTE: 2 CAPACITORS NEAR POWER PINS PER BUFFER, AND THE BULK CAPACITOR SHOULD BE PLACED ON THE BOARD IN THE GENERAL AREA OF THE BUFFERS.





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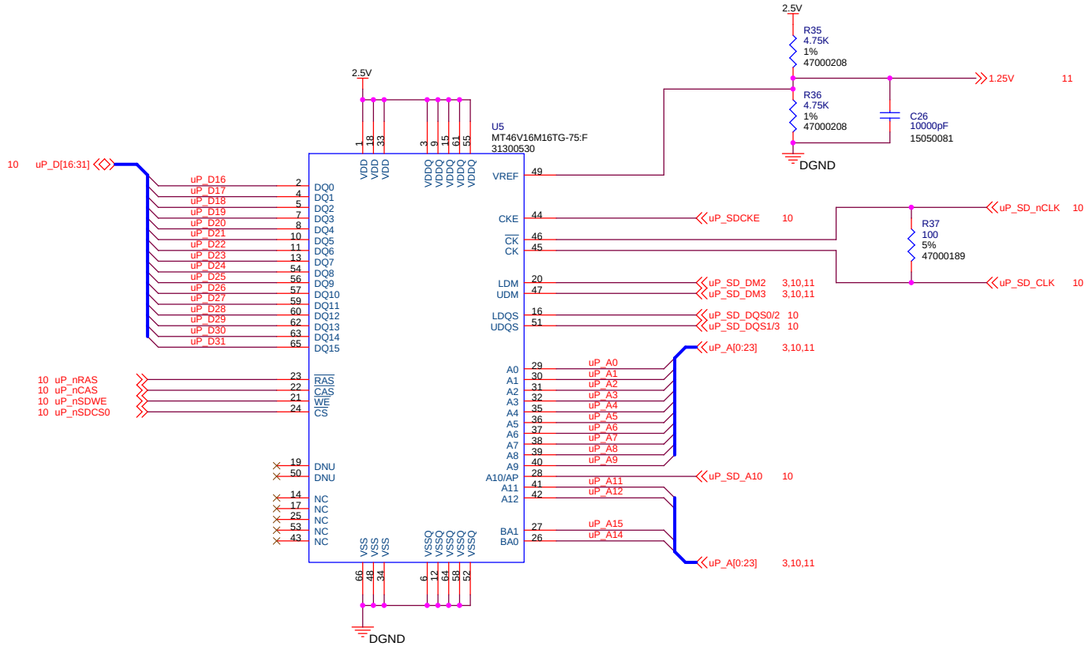
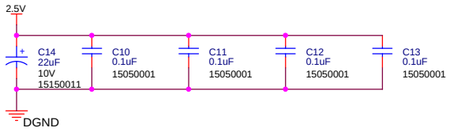
04 - DDR RAM

ENGINE DENSITY	CONFIG	PART #
16 MByte		MT46V8M16TG-75
32 MByte	STANDARD	MT46V16M16TG-75:F
64 Mbyte		MT46V32M16P-75





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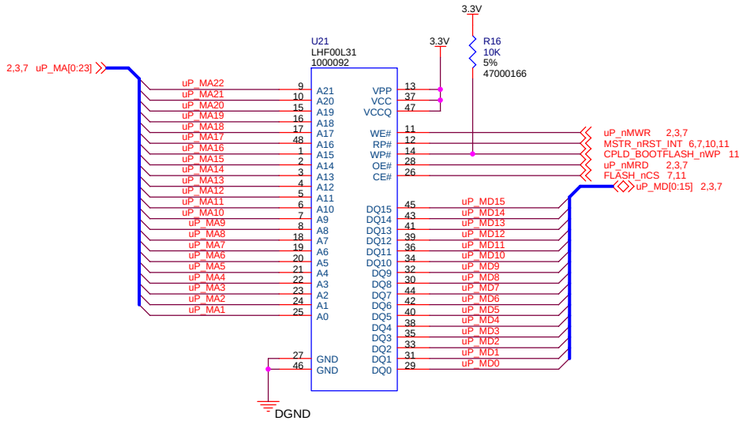
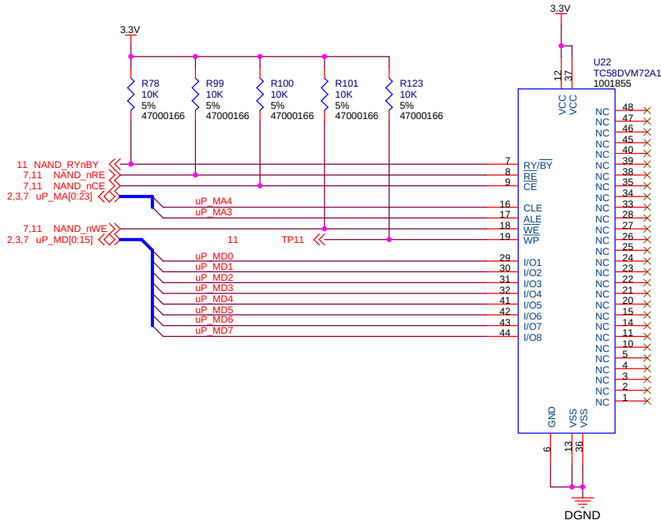
05 - FLASH

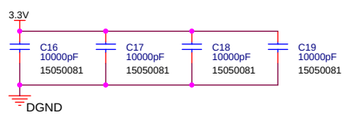


NOR DENSITY	CONFIG	PART #
1 MByte		TE28F800C3BA90
2 MByte	STANDARD	LHF00L31 TE28F160C3BD70
4 MByte		TE28F320C3BC70



NAND DENSITY	CONFIG	PART #
16 MByte	STANDARD	NAND128W3A0AN6 TC58DVM72A1FT00
32 MByte		NAND256W3A0AN6 TC58DVM82A1FT00
64 MByte		NAND512W3A0AN6 TC58DVM92A1FT00

NOTE: PLACE TWO .01uF DECOUPLING CAPS
PER CHIP NEAR THE FLASH ON THE PCB.



REVISION 3 -> A

1) REMOVED 8MB FLASH OPTION.

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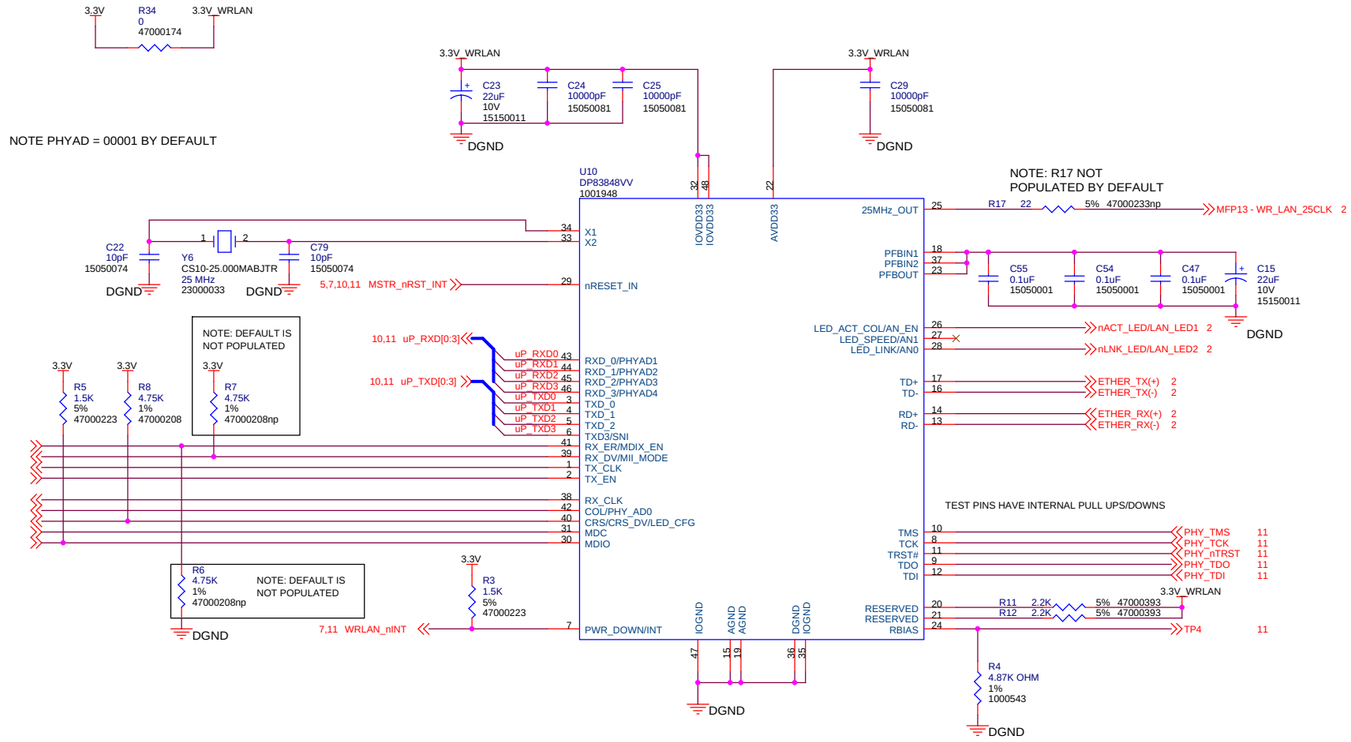
06 - WIRED LAN



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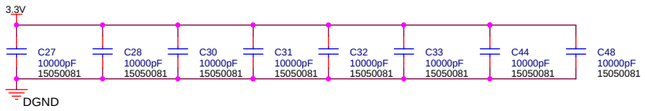
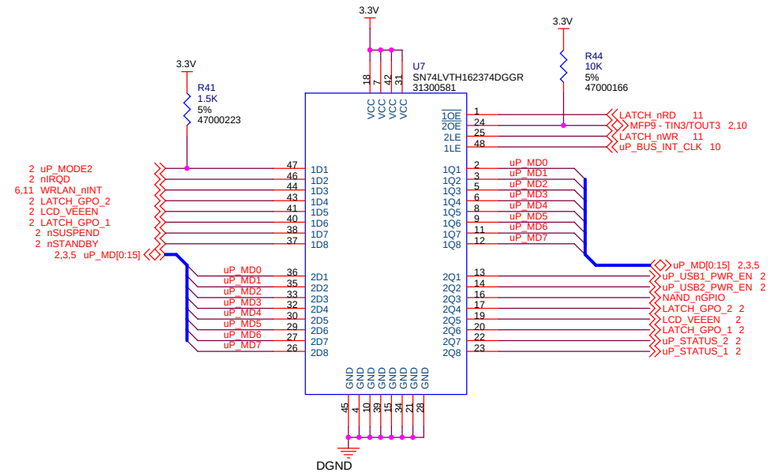
07 - LOGIC

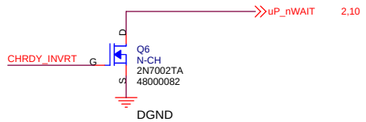
NOTE: PLACE ONE .01uF DECOUPLING CAPS
PER CHIP NEAR THE FLASH ON THE PCB.



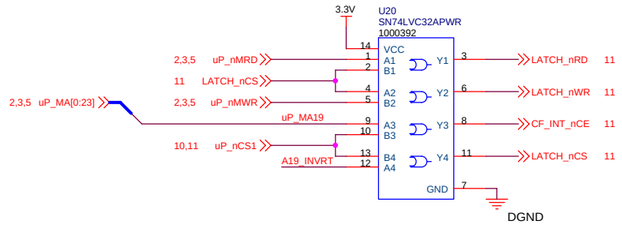
LATCH U7 IS USED AS A MEMORY MAPPED INPUT/OUTPUT REGISTER BASED ON READS AND WRITES TO AREA 1 + OFFSET. THE PHYSICAL ADDRESS IS nCS1 + 0X00080000 (nCS1 LOW AND A19 HIGH)



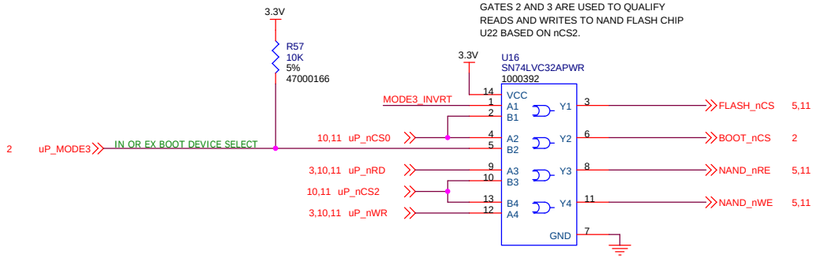
THIS MOSFET ALLOWS FOR COMPACT FLASH CARDS THAT HAVE PUSH/PULL OUTPUTS ON THE nCHRDY PINS TO MAINTAIN OPEN DRAIN ASSERTION OF THE nWAIT SIGNAL.



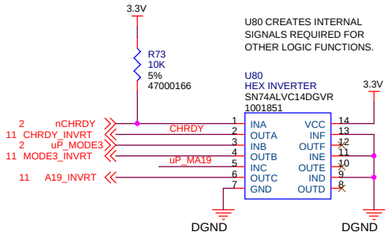
U20 QUALIFIES READS AND WRITES TO LATCH U7 AND THE CF CARD USING nCS1 AND A19.



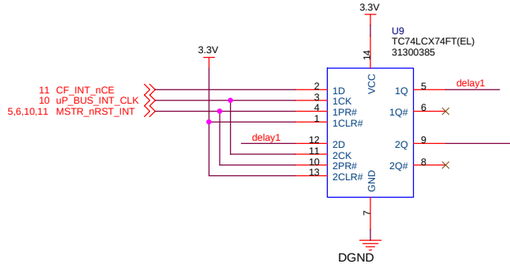
U16 GATES 1 AND 2 ROUTE nCS0 TO ONBOARD OR OFFBOARD BOOT DEVICE. GATES 2 AND 3 ARE USED TO QUALIFY READS AND WRITES TO NAND FLASH CHIP U22 BASED ON nCS2.



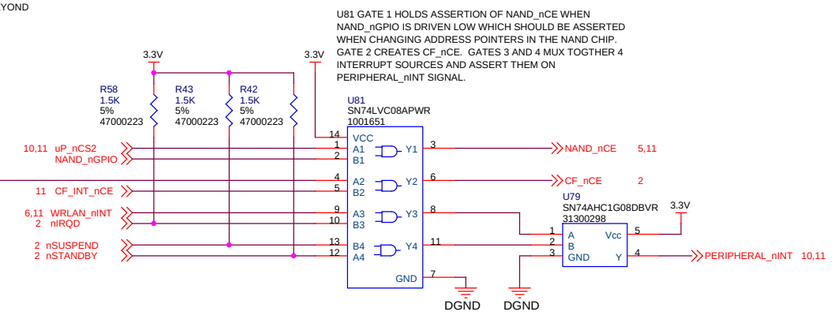
U80 CREATES INTERNAL SIGNALS REQUIRED FOR OTHER LOGIC FUNCTIONS.



U9 DELAYS RISING EDGE OF CF_nCE BY 2 CLOCKS TO MEET CF TIMING. ADDRESS HOLD TIME MUST BE EXTENDED FOR nCS1 FLEX BUS AREA IN SOFTWARE BY 2 CLOCKS BEYOND nCS1 DEASSERTION TO PREVENT BUS CONFLICTS.



U81 GATE 1 HOLDS ASSERTION OF NAND_nCE WHEN NAND_nGPIO IS DRIVEN LOW WHICH SHOULD BE ASSERTED WHEN CHANGING ADDRESS POINTERS IN THE NAND CHIP. GATE 2 CREATES CF_nCE. GATES 3 AND 4 MUX TOGTHER 4 INTERRUPT SOURCES AND ASSERT THEM ON PERIPHERAL_nINT SIGNAL.



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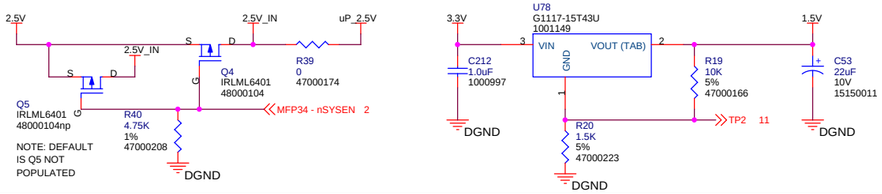
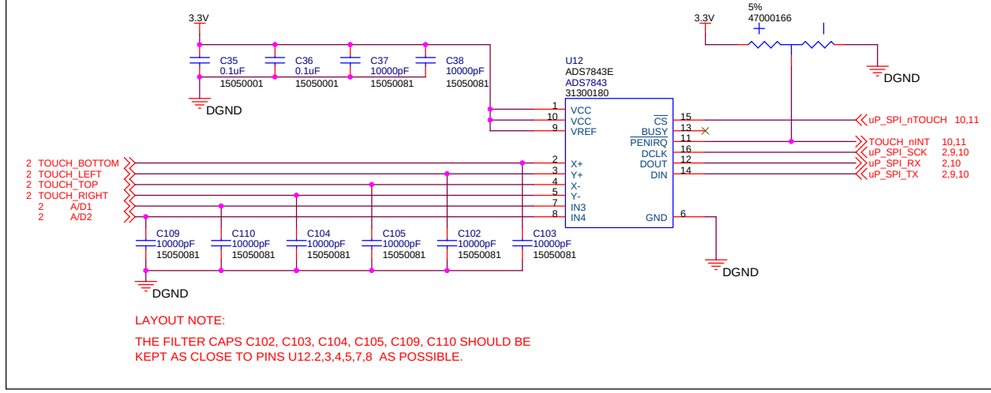
Vin = 3.3V
Vout = 1.5V
Iout < 1A



TOUCH

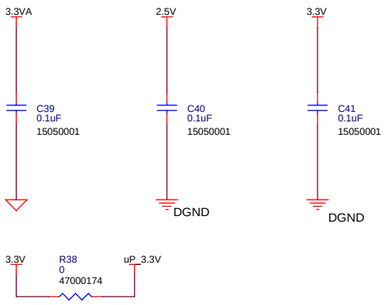
NOTE: JP2 IS + SIDE POPULATED WHEN U12 IS PRESENT, OTHERWISE JP2 IS - SIDE POPULATED



LAYOUT NOTE:

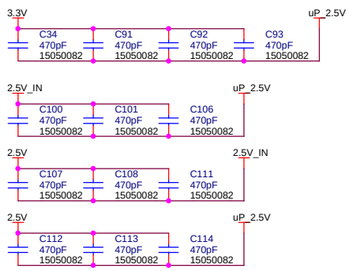
THE FILTER CAPS C102, C103, C104, C105, C109, C110 SHOULD BE KEPT AS CLOSE TO PINS U12.2,3,4,5,7,8 AS POSSIBLE.

POWER



LAYOUT NOTE:

THESE CAPACITORS ARE USED FOR DECOUPLING ACROSS POWER PLANES ON THE CARD ENGINE AND ARE STRATEGICALLY PLACED TO MINIMIZE EMISSIONS.



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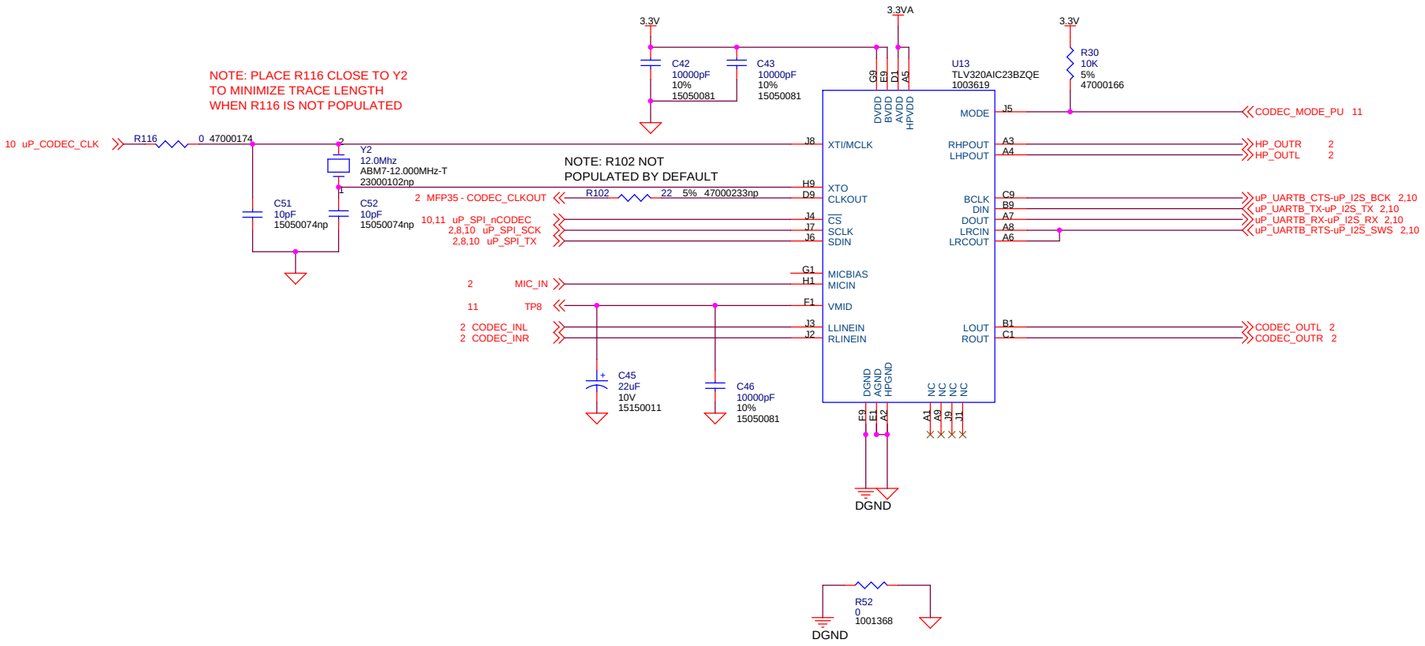
09 - CODEC

NOTE: UARTB AND AUDIO INTERFACE
CANNOT BE USED SIMULTANEOUSLY



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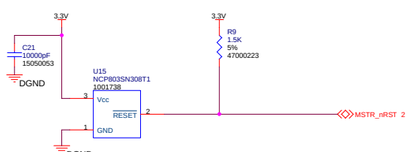
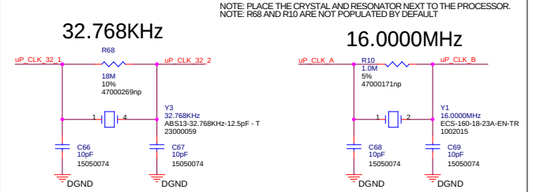
10 - PROCESSOR

RESET CIRCUIT



CLOCKS

NOTE: PLACE THE CRYSTAL AND RESONATOR NEXT TO THE PROCESSOR.
NOTE: R68 AND R10 ARE NOT POPULATED BY DEFAULT



POWER SENSE

NOTE: PLACE NEAR PINS 79 AND 80 OF EXPANSION CONNECTOR A

PROBABLY STILL WANT TO LEVEL SHIFT nCS4, nCS5 BEFORE GOING OFF BOARD

NOTE: UARTB AND AUDIO INTERFACE CANNOT BE USED SIMULTANEOUSLY

NOTE: DEFAULT IS R59 NOT POPULATED

NOTE: DEFAULT IS R65 NOT POPULATED

REVISION 2 -> 3

1) CPU U14 PIN OUT CHANGED FOR BALLS H1, H11, J4, AND J11

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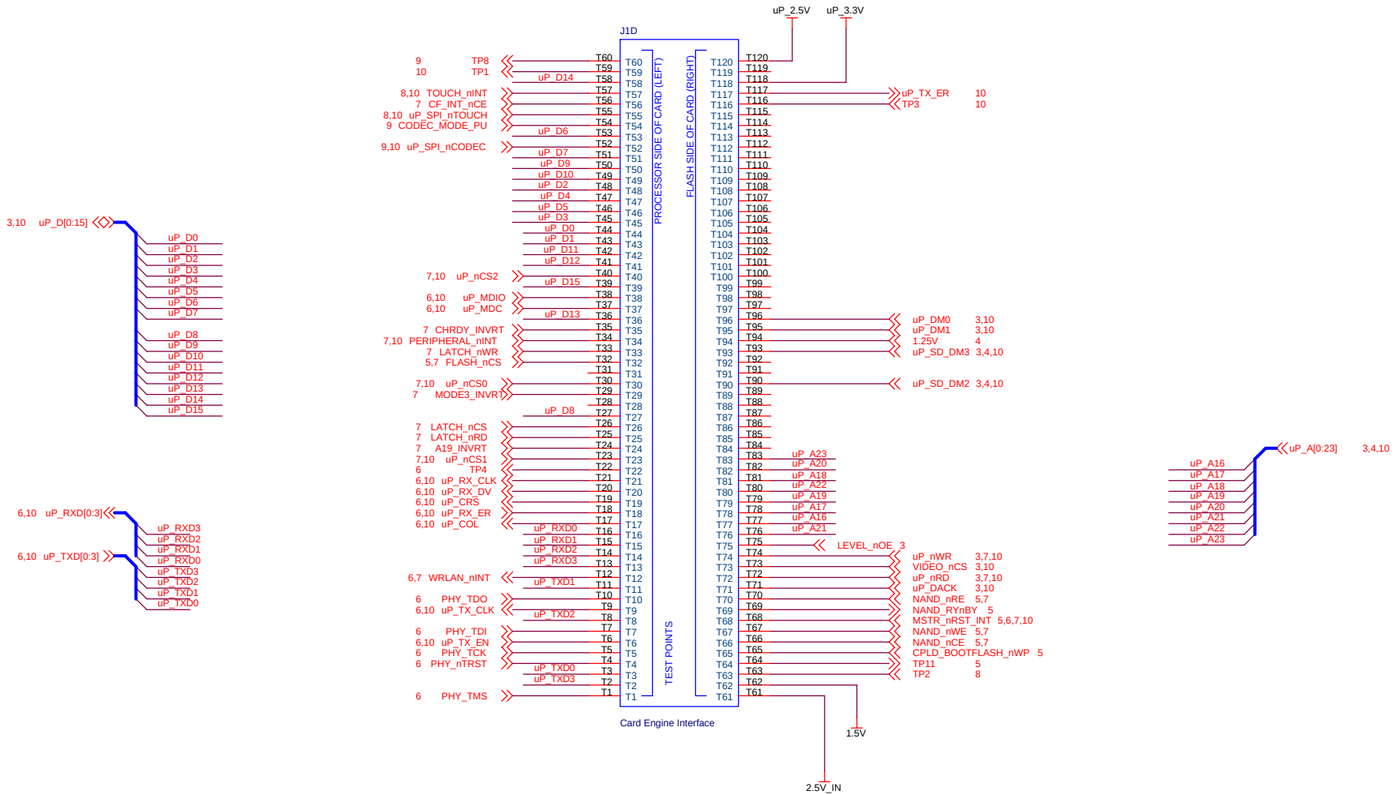
11 - TEST POINTS

NOTE: THIS SYMBOL REPRESENTS THE 60 TEST POINTS LOCATED ON THE RIGHT AND LEFT EDGES OF THE CARD ENGINE.



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12 - ECO LIST

Revision Control			
ECO Number	Rev	Description of Change	Date
	1	Preliminary Schematics	
C02126	2	Changes from DVT on Dragonfire board	12/12/2005
C02954	3	Beta build. CPU pin out change only.	09/26/2006
C03532	A	Production. Removed 8MB Flash option.	03/20/2007

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