LH79520 to LH79524 Card Engine Migration

Application Note 435

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Abstract

This Application Note is for developers who are presently using the LH79520 Card Engine with the intention of migrating to the LH79524 Card Engine. The goal of this document is to provide a guide for baseboard design so that the transition from the LH79520 to the LH79524 may be as smooth as possible

Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	MR	Initial release	RGL	03/04/10

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1 Introduction

The NXP LH79520 and LH79524 processors are very similar. The main difference between the two is that the LH79524 has more peripheral options than the LH79520: the LH79520 processor peripherals are a subset of the LH79524 peripheral set. Logic has created Card Engines for both of these processors with the intent to allow them to be interchangeable from a customer-specific baseboard development standpoint

2 Differences between LH79520 and LH79524 Card Engines

2.1 Memory

The LH79524 provides additional memory density configuration options.

2.1.1 DRAM

The LH79520 and LH79524 offer DRAM densities of 16, 32, or 64 MB. The default configuration for the LH79520 is 32 MB. The default configuration for the LH79524 is 64 MB.

2.1.2 SRAM

The LH79520 contains 32 kB of on-chip SRAM. The LH79524 contains 16 kB of on-chip SRAM.

2.1.3 Programmable Memory Interface

The LH79524 provides a 24-bit external address bus and a 32-bit external data bus for SDRAM and SRAM/Flash/ROM interfaces. An on-chip Boot ROM controller allows booting from 8-, 16-, or 32-bit devices.

2.1.4 NAND Flash

The LH79524 processor supports direct connection to NAND flash chips. An internal boot ROM allows the Card Engine to boot directly from a discrete NAND device. The default configuration for the LH79524 is 64 MB of NAND flash. However, the NAND device footprint is scalable from 32, 64, 128 MB, and higher depending on NAND chip availability.

2.2 USB

The LH79520 does not support an onboard USB Host controller. The LH79524 Card Engine is configured with one available USB device interface. The USB client supports full-speed (12 Mbits/sec) operation, and both suspend and resume signaling. Please refer to the LH79524 Universal Microcontroller User's Guide for information on how to properly use this feature.

2.3 Analog to Digital Converter (ADC)

The LH79520 microcontroller does not contain an internal ADC. The LH79524 microcontroller contains an internal ADC which provides a total of 8 analog inputs available from the J1A expansion connector. Note: The touch interface is multiplexed with four ADC signals on the Card Engine.

2.4 Vectored Interrupt Controller

The LH79524 contains a Vectored Interrupt Controller which provides 16 standard and 16 vectored IRQ interrupts. Each interrupt is configurable as IRQ or FIQ.

2.5 I2C

The LH79524 Card Engine has added an I^2C Module.

2.6 Codecs

The LH79524 processor contains integrated codec support features (I^2S).

2.7 Direct Memory Access (DMA)

The LH79520 processor has two external DMA channels. The LH79524 processor has one external DMA channel muxed with the UART0 CTS and RTS signals. If CTS and RTS functionality on UART0 are not required, the external DMA channel is available to the user. If necessary, please contact Logic for assistance gaining support for the device.

2.8 General Purpose I/O (GPIO)

The LH79520 contains up to 64 GPIO signals. The LH79524 increases the number of GPIO signals to 108 pins on 14 ports. The following tables list the pin differences between the LH79520 and LH79524 Card Engines.

Table 3.1: Connector J1C Pin Differences

Card Engine	Pin #	Signal Name	I/O	Description
LH79520	J1C.10	VIDEO_nMCS	O	Chip select for area 1 of LH79520 memory (active low).
LH79524	J1C.10	VIDEO_nCS	O	This signal is tied to the CPLD, it is disabled internally.
LH79520	J1C.18	3.3V_WRLAN	I	This pin outputs power for use with external Wired Lan circuitry. Please refer to Logic Product Development SDK and IDK kits for reference designs for Wired Lan connector implementations. Typically this power output would be used to supply power to the Wired Lan Activity and Link LEDs.
LH79524	J1C.18	2.5V	O	Power Supply (2.5V). To maintain scalability between multiple Logic Product Development Card Engines, This signal should be used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
LH79520	J1C.21	uP_NMI	I	The NMI (non-maskable interrupt – highest priority) and IRQ[3:0] signals generate a request to the CPU for service (interrupt service routine). The NMI signal is active low. The uP_NMI has a 10k pull up located on the Card Engine.
LH79524	J1C.21		NC	No internal connection (not implemented on the LH79524)
LH79520	J1C.23		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
LH79524	J1C.23	CPLD_nIRQD	I	Active Low. Dedicated hardware interrupt on LH79524. This interrupt is readable and maskable in the CPLD. See the IO controller specification for detailed information on accessing CPLD interrupts. This signal is pulled up to 3.3V through a 10K resistor.
LH79520	J1C.39		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
LH79524	J1C.39	uP_UARTA_RTS (UP_UARTA_RTS – DREQ)	O	The LH79524 UART0 RTS signal. Tied to 3.3V through a 10K resistor.

Card Engine	Pin #	Signal Name	I/O	Description
LH79520	J1C.41		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
LH79524	J1C.41	uP_UARTA_CTS (uP_UARTA_CTS – nDACK)	I	The LH79524 UART0 CTS signal. Tied to 3.3V through a 10K resistor.
LH79520	J1C.48		NC	No internal connection.
LH79524	J1C.48	DREQ0 (uP_UARTA_RTS – DREQ)	I/O	DMA request 0 signal. This signal is multiplexed with UARTA _RTS signal. This signal has a 10K pull up to 3.3V. This signal is only externally connected when R114 is populated. R114 is not populated by default.
LH79520	J1C.54	uP_DACK1	O	This handshake signal is output by the CPU to acknowledge DMA requests.
LH79524	J1C.54		NC	No internal connection (not implemented on the LH79524)
LH79520	J1C.56		NC	No internal connection.
LH79524	J1C.56	nDACK0 (uP_UARTA_CTS – nDACK)	I/O	DMA acknowledge 0 signal. This signal is multiplexed with UARTA_CTS. This signal has a 10K pull up to 3.3V. This signal is only externally connected when R115 is populated. R115 is not populated by default.
LH79520	J1C.65	uP_SPI_FRM	O	Serial Frame Output.
LH79524	J1C.65		NC	No internal connection (not implemented on the LH79524)
LH79520	J1C.67	uP_SPI_MOSI_TX	O	This output transmits SPI data.
LH79524	J1C.67		NC	No internal connection (not implemented on the LH79524)
LH79520	J1C.69	uP_SPI_MISO_RX	I	This input receives SPI data. This signal has a 10k pull up located on the Card Engine.
LH79524	J1C.69		NC	No internal connection (not implemented on the LH79524)
LH79520	J1C.71	uP_SPI_SCK	O	SPI transmit/receive data is shifted/sampled on the rising or falling edge of this clock.
LH79524	J1C.71		NC	No internal connection (not implemented on the LH79524)
LH79520	J1C.74		NC	No internal connection.
LH79524	J1C.74	uP_nWE3	O	Active low. Byte lane enable for data bus bits 24->31.
LH79520	J1C.128	uP_MA19	I/O	Buffered Address Bus bit 19.
LH79524	J1C.128		O	This signal is tied to ground through a 10K resistor.
LH79520	J1C.130	uP_MA20	I/O	Buffered Address Bus bit 20.
LH79524	J1C.130	uP_A19	O	Address Bus bit 19.
LH79520	J1C.132	uP_MA21	I/O	Buffered Address Bus bit 21.
LH79524	J1C.132	uP_A20	O	Address Bus bit 20.
LH79520	J1C.134	uP_MA22	I/O	Buffered Address Bus bit 22.
LH79524	J1C.134	uP_A21	O	Address Bus bit 21.
LH79520	J1C.136	uP_MA23	I/O	Buffered Address Bus bit 23.
LH79524	J1C.136	uP_A22	O	Address Bus bit 22.
LH79520	J1C.138	uP_MA24	I/O	Buffered Address Bus bit 24.
LH79524	J1C.138		O	This signal is tied to ground through a 10K resistor.

Card Engine	Pin #	Signal Name	I/O	Description
LH79520	J1C.140	uP_MA25	I/O	Buffered Address Bus bit 25.
LH79524	J1C.140	uP_A23	O	Address Bus bit 23.

Table 3.2: Connector J1A Pin Differences

Card Engine	Pin #	Signal Name	I/O	Description
LH79520	J1A.6		NC	No internal connection.
LH79524	J1A.6	LCD_VEEEN - MOD	O	Active high. This signal is the enable for the LCD panel Vee.
LH79520	J1A.8	LCD_CLK_RETURN	I	High Resolution clock input. This signal has a 10k pull down located on the Card Engine.
LH79524	J1A.8		NC	No internal connection (not implemented on the LH79524)
LH79520	J1A.12	G0	O	High Resolution Rev (AC bias) Signal.
LH79524	J1A.12	LCD_PSAVE	O	LCDPS Signal Output (Power Save)–This signal is only used with a HR-TFT interface.
LH79520	J1A.15		NC	No internal connection.
LH79524	J1A.15	LCD_VEEEN - MOD	O	LCDMOD is only used with a HR-TFT interface
LH79520	J1A.16	B0	O	High Resolution Power Save Signal.
LH79524	J1A.16	LCD_REV – DON	O	LCDREV Signal Output (Grey Scale Voltage Reverse) – This signal is only used with the HR-TFT interface.
LH79520	J1A.19		NC	No internal connection.
LH79524	J1A.19	uP_I2S_BCK	O	Clock output from the onboard I2S interface. If no CODEC is populated, an external CODEC or other device could use this signal.
LH79520	J1A.21		NC	No internal connection.
LH79524	J1A.21	uP_I2S_SWS	O	This signal is the I2S sync output to an I2S compliant audio CODEC. The CODEC Frequency is set on the CODEC, while the default frequency for the sync is set up on the processor.
LH79520	J1A.22		NC	No internal connection.
LH79524	J1A.22	uP_I2S_RX – UARTC_RX	I	This signal is the I2S output from the CODEC to the processor.
LH79520	J1A.23		NC	No internal connection.
LH79524	J1A.23	uP_I2S_TX – UARTC_TX	O	This signal is the I2S output from the processor to the I2S compliant CODEC.
LH79520	J1A.64		NC	No internal connection.
LH79524	J1A.64	CPLD_GPIO_2	I/O	This signal is a general purpose I/O (GPIO). It is controlled by a memory-mapped address in the CPLD. See the LH79524 IO Controller Specification for further details.
LH79520	J1A.67		NC	No internal connection.
LH79524	J1A.67	uP_USB1_nOVR_CRNT - VBUS	I	Active HIGH. This is a detect signal used to determine whether or not the USB interface is currently in use. This signal is pulled down to GND through a 365K resistor. See SDK baseboard schematics for proper USB interfacing.
LH79520	J1A.69		NC	No internal connection.
LH79524	J1A.69	uP_USB1_PWR_EN	O	Active high. Enables power supply for USB. See SDK baseboard schematics for proper USB interfacing.

Card Engine	Pin #	Signal Name	I/O	Description
LH79520	J1A.72		NC	No internal connection.
LH79524	J1A.72	uP_USB1_M	I/O	USB data I/O minus. Route as a differential pair with uP_USB1_P.
LH79520	J1A.73		NC	No internal connection.
LH79524	J1A.73	uP_USB1_P	I/O	USB data I/O plus. Route as a differential pair with uP_USB1_M.
LH79520	J1A.74	BUFF_nOE	O	Controls the outputs of the buffers present on the Card Engine, the states are active or tri-state.
LH79524	J1A.74		NC	No internal connection (not implemented on the LH79524)
LH79520	J1A.78		NC	No internal connection.
LH79524	J1A.78	MIC_IN	I	This signal is the microphone input to the I2S compliant audio CODEC. Please see the Texas Instruments #TLV320AIC23GQE Stereo Audio CODEC Technical Datasheet for more details.

Table 3.3: Connector J1B Pin Differences

Card Engine	Pin #	Signal Name	I/O	Description
LH79520	J1B.46		NC	No internal connection.
LH79524	J1B.46	uP_I2S_TX - UARTC_TX	O	UARTC transmit output signal on the LH79524.
LH79520	J1B.47		NC	No internal connection.
LH79524	J1B.47	uP_I2S_RX - UARTC_RX	I	UARTC receive input signal on the LH79524.
LH79520	J1B.48	MFP9 - CLKIN/UARTCLK	I	External Clock Input (if CLKINSEL = high at reset) This signal has a 10k pull up located on the Card Engine.
LH79524	J1B.48		NC	No internal connection (not implemented on the LH79524)
LH79520	J1B.49	MFP10 - CLKINSEL	I	External Clock Select. This signal has a 10k pull down located on the Card Engine. The processor also has an internal pull down. The card engine derives its clock from the 14.7456 crystal onboard when this signal is LOW.
LH79524	J1B.49		NC	No internal connection (not implemented on the LH79524)
LH79520	J1B.50		NC	No internal connection.
LH79524	J1B.50	MFP11 – uP_PA3/CTCAP0B/CTCMP0B	I/O	GPIO pin, Port A bit 3 I/O
LH79520	J1B.56		NC	No internal connection.
LH79524	J1B.56	MFP16 – uP_PJ4/AD3	I	Digital or Analog GPIO, Port J bit 4, A/D bit 3
LH79520	J1B.57		NC	No internal connection.
LH79524	J1B.57	MFP17 – uP_PJ2/AD4	I	Digital or Analog GPIO, Port J bit 2, A/D bit 4
LH79520	J1B.58		NC	No internal connection.
LH79524	J1B.58	MFP18 - uP_PA5/CTCAP1A/CTCMP1B	I/O	GPIO pin, Port A bit 5 I/O
LH79520	J1B.59		NC	No internal connection.
LH79524	J1B.59	MFP19 – uP_PA4/CTCAP1A/CTCMP1A	I/O	GPIO pin, Port A bit 4 I/O

Card Engine	Pin #	Signal Name	I/O	Description
LH79520	J1B.62	MFP22 - PWM1/DEOT1	O	PWM Output
LH79524	J1B.62		NC	No internal connection (not implemented on the LH79524)
LH79520	J1B.63	MFP23 – CPLD_GPI_3	O	This signal is a general-purpose input. This signal has a 10K pull up.
LH79524	J1B.63	MFP23 - uP_PA7/CTCAP2B/CTCMP2B/SCL	I/O	GPIO pin, Port A bit 7 I/O
LH79520	J1B.64		NC	No internal connection.
LH79524	J1B.64	MFP24 - uP_PA6/CTCAP2A/CTCMP2A/SDA	I/O	GPIO pin, Port A bit 6 I/O
LH79520	J1B.67	MFP26 - uP_PH7	I	Port H bit 7
LH79524	J1B.67		NC	No internal connection (not implemented on the LH79524)
LH79520	J1B.68	MFP27 - uP_MCS2	O	Chip select for area 2 of LH79520 memory
LH79524	J1B.68		NC	No internal connection (not implemented on the LH79524)
LH79520	J1B.69	MFP28 – nTSTA	O	Reserved for production test.
LH79524	J1B.69		NC	No internal connection (not implemented on the LH79524)
LH79520	J1B.71	MFP30 - uP_nSDWE	O	SDRAM Write Enable.
LH79524	J1B.71		NC	No internal connection (not implemented on the LH79524)
LH79520	J1B.72	MFP31 - uP_nMCS3	O	Chip select for area 3 of LH79520 memory.
LH79524	J1B.72	MFP31 - uP_nSDCS1	O	Active low. This signal is the processor's Synchronous Memory Chip Select 1.

3 Summary

The NXP LH79520 and LH79524 processors are very similar with exception to the number of peripherals. Logic utilized their similarities to make the LH79520 and LH79524 Card Engine products, which can be used almost interchangeably depending on the user's application. However, due to the larger number of peripherals on the LH79524 processor, the LH79524 Card Engine has additional peripheral features which are not available on the LH79520 Card Engine.

