Communicating to the CODEC via I2S

Application Note 194

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Abstract

This document is applicable to the LH79520-10 card engine. The following procedure needs to be followed in order to communicate to the on-board CODEC via the CPLD I2S peripheral. See the Texas Instruments TLV320DAC23 data sheet for the complete command set and registers.

REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	James Wicks	Release	HR	01/02/2004

1 Introduction

This document applies the LH79520-10 card engine's audio interface. It gives an overview of the software steps that must be taken in order to use the audio output interface on the card engine.

The audio output interface on the LH7952-10 card engine is driven by a TI TLV320DAC23 (audio DAC) that has an I2S digital audio interface to receive audio-out data from the system. The TLV320DAC23 takes the data on its I2S interface and coverts it to the analog equivalent on the audio output interface.

The Sharp LH79520 processor does not have a native I2S peripheral. To provide for an I2S communication scheme, an I2S peripheral was incorporated into the LH79520-10's on-board CPLD.

2 Communicating to the CODEC via I2S

1. Setup processor DMA:
   a. Configure the processor DMA for audio to use the external request signal, and for a 32-bit source to 32-bit destination transfer, with the source address incrementing and the destination address fixed.
   b. Set up the audio buffer for 32-bit words, where each word is one stereo sample, with bits 31 down to 16 for the left channel, and bits 15 down to 0 for the right channel.
   c. Point the source address to the audio buffer and the destination address to 0x5440 0000 (the I2S memory mapped data register on the card engine CPLD). Since it is configured for a 32-bit destination, and the IO Controller is on a 16-bit wide memory space, the DMA controller will automatically perform two writes: one to addresses 0x54400000 (left channel audio data register) and one to address 0x54400002 (right channel audio data register).

2. Configure the CODEC:
   a. The CODEC needs to be configured over the SPI interface (See Logic's Application Note 187: CODEC configuration via SPI, referenced in Section 3.3.1 of the LH79520-10 IO Controller Specification.)

3. Play audio buffer:
   a. When the IO Controller receives the bit-clock from the CODEC (after it has been configured), the IO Controller will generate a DMA request every sample period.
   b. In response to the DMA requests, the processor will write out the DMA buffer to the audio interface per the DMA configuration given the processor in step 1.