CODEC Configuration via SPI

Application Note 187

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Abstract

Follow the procedure below to configure certain Card Engine's CODEC device via the CPLD SPI peripheral. This application note is applicable for the LH79520-10 and SH7750R-10 Card Engines.

REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
1	James Wicks	First draft	JAW	11/25/2003
A	Hans Rempel	Release Edit	HR	01/02/2004

1 Introduction

The following procedure needs to be followed in order to configure the CODEC via the CPLD SPI peripheral. For CODEC configuration details, please see Texas Instruments TLV320DAC23 data manual for the complete command set and registers.

2 Configure the Codec via SPI

1. Write applicable 8-bit SPI data into the SPI DATA register.

2. Write 0x11 to the SPI CONTROL register. (see bit definition below.)
   bit (0) = 1, CODEC selected
   bit (1) = 0, touch not selected
   bit (2) = 0, write
   bit (3) = x, RD ONLY BIT
   bit (4) = 1, load 8-bit SPI data into internal shift register and load count
   bit (5) = x, RD ONLY BIT

3. Read SPI CONTROL register until bit (5) goes high (indicates registers loaded).

4. Write 0x01 to SPI CONTROL register. (writing this command starts SPI TX.)
   bit (0) = 1, CODEC selected
   bit (1) = 0, touch not selected
   bit (2) = 0, write
   bit (3) = x, RD ONLY BIT
   bit (4) = 0, don't load shift register and count
   bit (5) = x, RD ONLY BIT

5. Read SPI CONTROL register until bit (3) goes high (indicates transmit done).

6. Repeat steps 1 – 5 one time. (this creates the necessary 16-bit transmit.)

7. Write 0x00 to the SPI CONTROL register.
   bit (0) = 0, CODEC not selected
   bit (1) = 0, touch not selected
   bit (2) = 0, write
   bit (3) = x, RD ONLY BIT
   bit (4) = 0, don't load shift register and count
   bit (5) = x, RD ONLY BIT