# LH79520-10: Setting and Configuring the Audio Interface

Application Note 176

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## Abstract

This document explains why the CODEC's power down control register's power, clock, and oscillator bits on the LH79520-10 must always be enabled (set to 0).



**REVISION HISTORY**

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# 1 Introduction

This document is applicable to LH79520-10 card engine. For this card engine, the Power Down Control register's power, clock, and oscillator bits on the CODEC must always be enabled (set to 0). Without this setting, the card engine will lock at system reset.

# 2 Audio CODEC Additional Info: Setting and Configuring

Attention must be made when writing to the CODEC control registers, specifically the '"Power Down Control" (CODEC offset + 0000110). The bits "OFF" (power - bit D7), "CLK" (clock - bit D6), and "OSC" (oscillator – D5) *must* be set to '0'.

The LH79520 processor turns off all external clocks during system reset. Therefore, the CODEC signal "MFP34-CODEC_CLKOUT" is routed to be the bus clock signal during system reset via the card engine CPLD to provide a bus clock to the system. Without a bus clock, the SDRAM will come up in an unknown state and will then attempt to drive the bus, consequently locking the system. Hence, on reset, the CODEC clock is used to drive the bus clock to bring SDRAM up in a known state and allow the card engine to function properly.

# 3 Summary

The CODEC power, clock, and oscillator must always be enabled (set to 0).