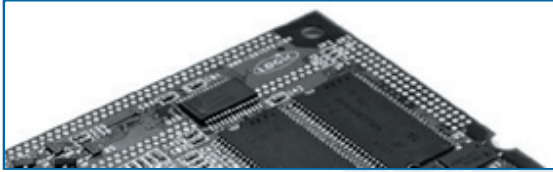




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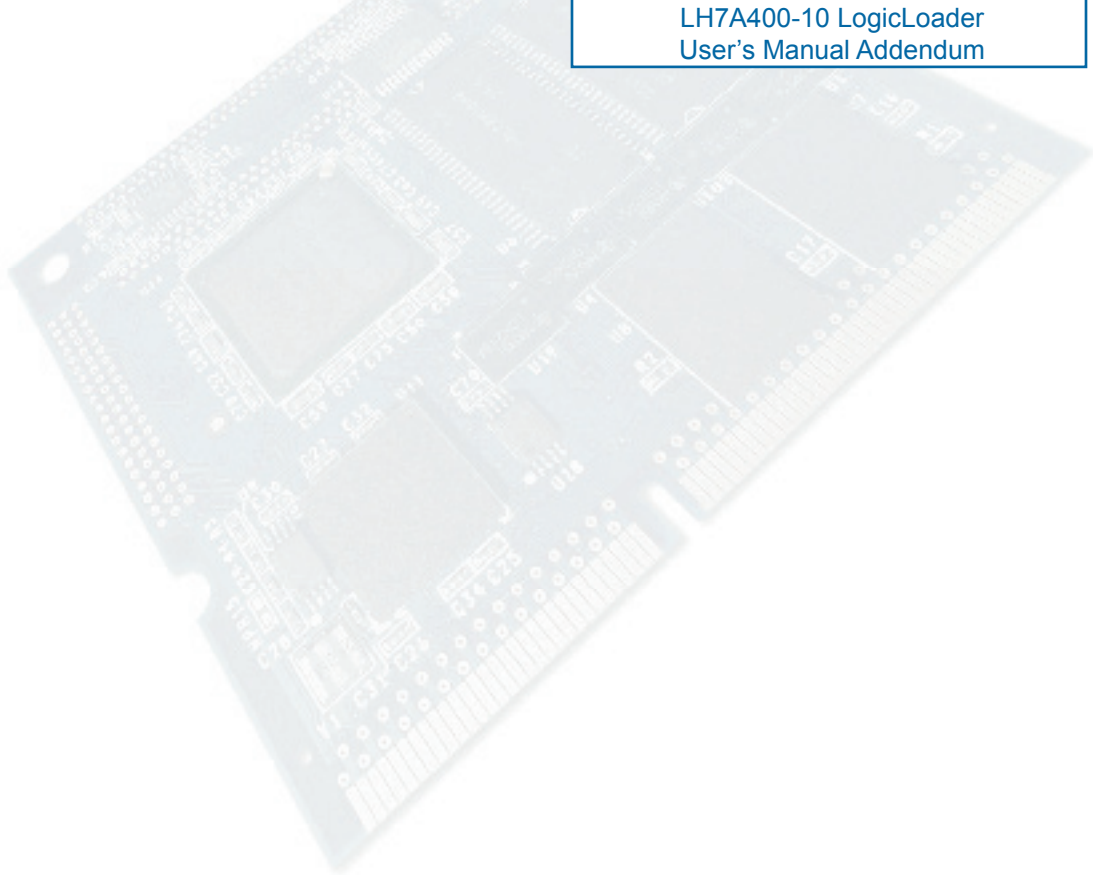
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Card Engine

LH7A400-10 LogicLoader
User's Manual Addendum



REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	LoLo Ver.	APPROVAL	DATE
A	Bruce Rovner	Release	-	B.R.	7/24/03
B	James Wicks	Figure 1.1 Revision	-	B.R.	10/17/2003
C	Chris Rempel, Bruce Rovner	Updated for LogicLoader Version 1.4 Release	1.4	B.R.	3/31/04
D	Aaron Stewart	Added Supported Options in LogicLoader	1.4.4	M.E.	12/3/04
E	Aaron Stewart, Bruce Rovner	Update for LogicLoader 2.03 release. Updated Section 1 diagrams for exec and execution format. Updated supported options table for hardware support description.	2.0.4	H.R.	10/14/05

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1 LH7A400-10 Memory Map Diagrams

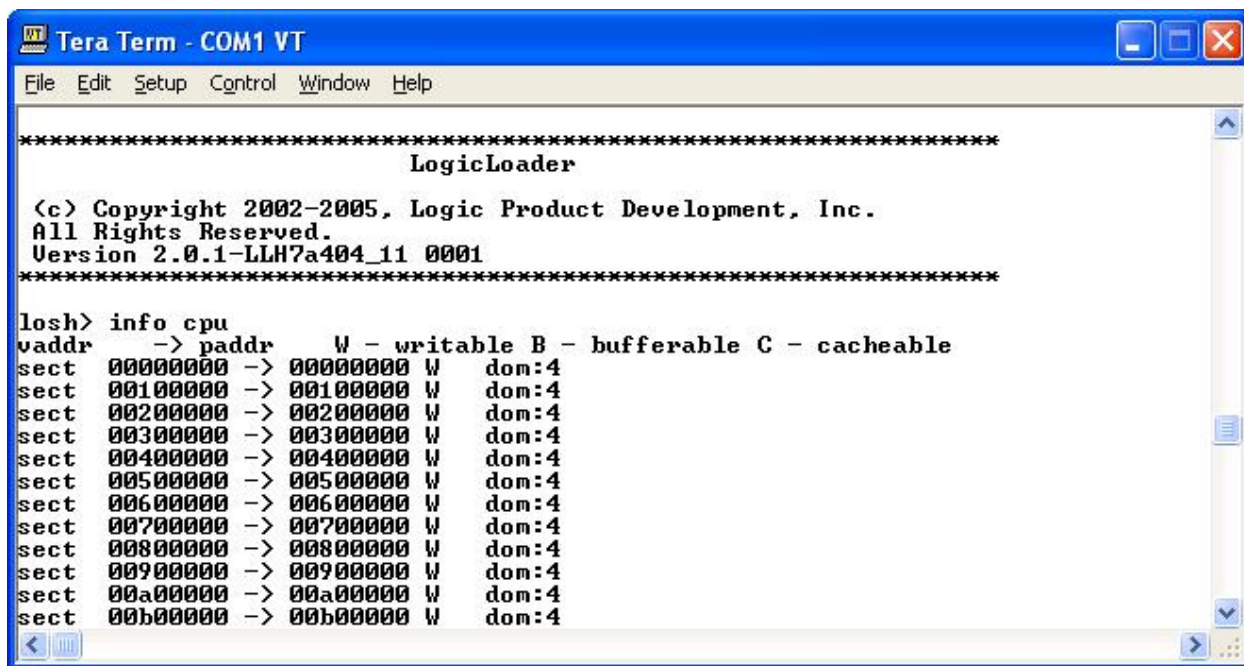
1.1 SDRAM Configuration

The LH7A400-10 Card Engine is designed to accommodate SDRAM of different sizes. Under LogicLoader's default configuration, all memory installed is accessible, however on 64MB card engines the SROMLL bit is set to make two separate 32MB physical chunks. The MMU is then configured to make the two 32MB chunks appear as a single 64MB virtual chunk.

For further documentation: please refer to the Sharp LH7A400 User Guide for more information on the SDRAM controller. Please refer to the ARM 922T Technical Reference Manual for more information on the MMU.

1.2 MMU Remap: Physical Memory to Logical Memory

LogicLoader sets up the MMU to remap physical memory to logical memory. Type 'info cpu' at the losh prompt to see how LogicLoader remaps physical memory to logical memory. If you need to address a device outside of the default address map, use the 'remap' command to make additional address space accessible from within LogicLoader.



```

*****
                LogicLoader
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All Rights Reserved.
Version 2.0.1-LLH7a404_11 0001
*****

losh> info cpu
vaddr  -> paddr    W - writable B - bufferable C - cacheable
sect  00000000 -> 00000000 W   dom:4
sect  00100000 -> 00100000 W   dom:4
sect  00200000 -> 00200000 W   dom:4
sect  00300000 -> 00300000 W   dom:4
sect  00400000 -> 00400000 W   dom:4
sect  00500000 -> 00500000 W   dom:4
sect  00600000 -> 00600000 W   dom:4
sect  00700000 -> 00700000 W   dom:4
sect  00800000 -> 00800000 W   dom:4
sect  00900000 -> 00900000 W   dom:4
sect  00a00000 -> 00a00000 W   dom:4
sect  00b00000 -> 00b00000 W   dom:4

```

Figure 1.1: Type "info cpu" to see the MMU remap

Note: the figures you see may differ from those presented in this example.

1.3 Physical Hardware Memory Map

Note: memory regions may require the use of the 'remap' command to be accessible.

LH7A400-10 Logical Memory Map during execution of LoLo
for 64M SDRAM

0xFFFFFFFF	NOT USED
0xC4000000	SDRAM
0xC0000000	RESERVED
0xB0014000	INTERNAL STATIC MEMORY (80 KB on-chip SRAM)
0xB0000000	
0x80003800	ADVANCED HIGH PERFORMANCE BUS REGISTERS
0x80002000	ADVANCED PERIPHERAL BUS REGISTERS
0x80000000	EXTERNAL I/O (FAST)
0x70000000	EXTERNAL I/O (SLOW)
0x60000000	PCMCIA - 2
0x50000000	PCMCIA - 1
0x40000000	NOT USED
0x10000000	FLASH MEMORY
0x00000000	

Figure 1.2: LH7A400-10 Hardware Memory Map

1.4 LogicLoader and the Configuration Block in Flash Memory

LogicLoader is programmed into the card engine's resident flash array. The optional Configuration Block may be added with the 'config CREATE' command.

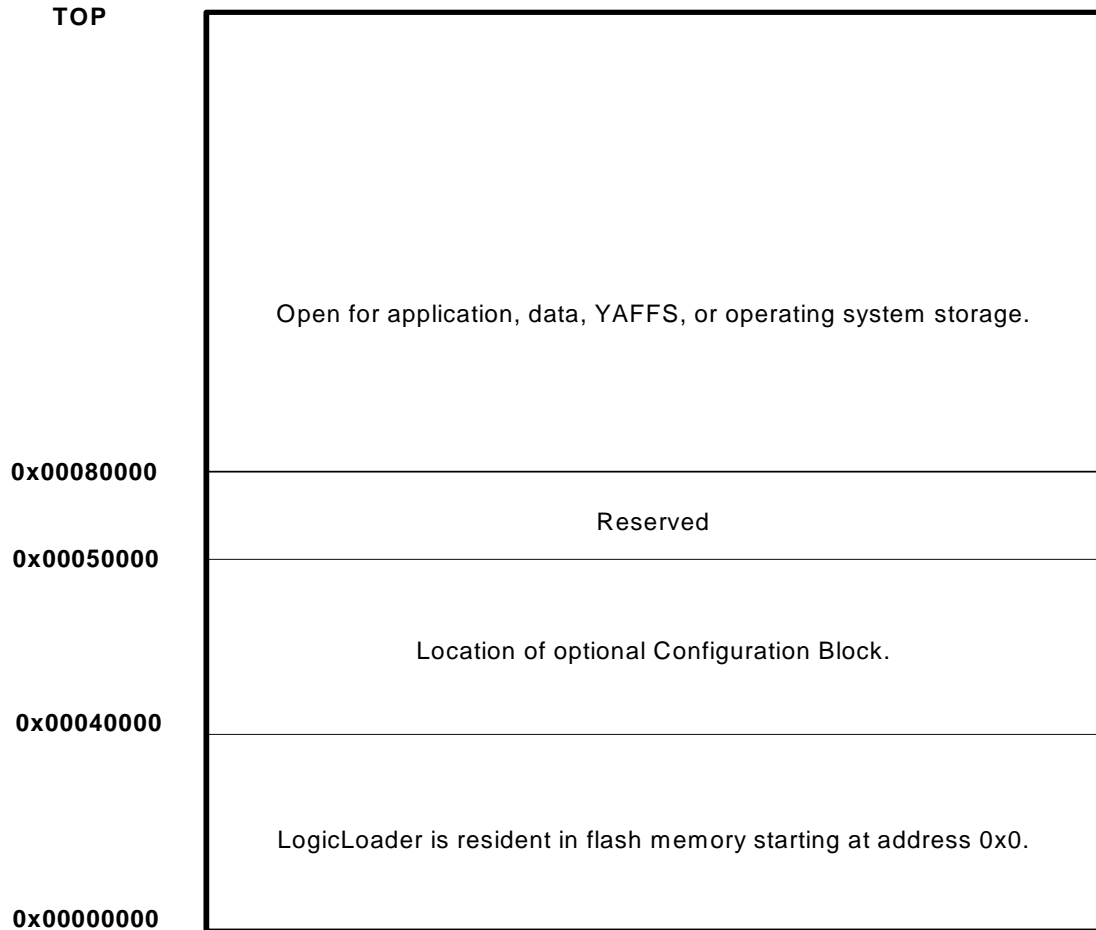


Figure 1.3: Flash Memory Layout

1.5 LogicLoader’s Location in RAM

LogicLoader executes out of RAM. The diagram below depicts run time location of LogicLoader.

Run-time location of LogicLoader:

At reset, LogicLoader relocates itself from flash memory to system SDRAM. LogicLoader then spends the remainder of its run-time executing out of system SDRAM.

Note: the size of LogicLoader’s code and variable sections are estimates. This size depends on the exact features built into the LogicLoader image and may change with new releases. The location of LogicLoader’s stack is dynamically determined at run-time based on the size of the code and variable section. Therefore, the location of the stack is provided as an estimate in this diagram.

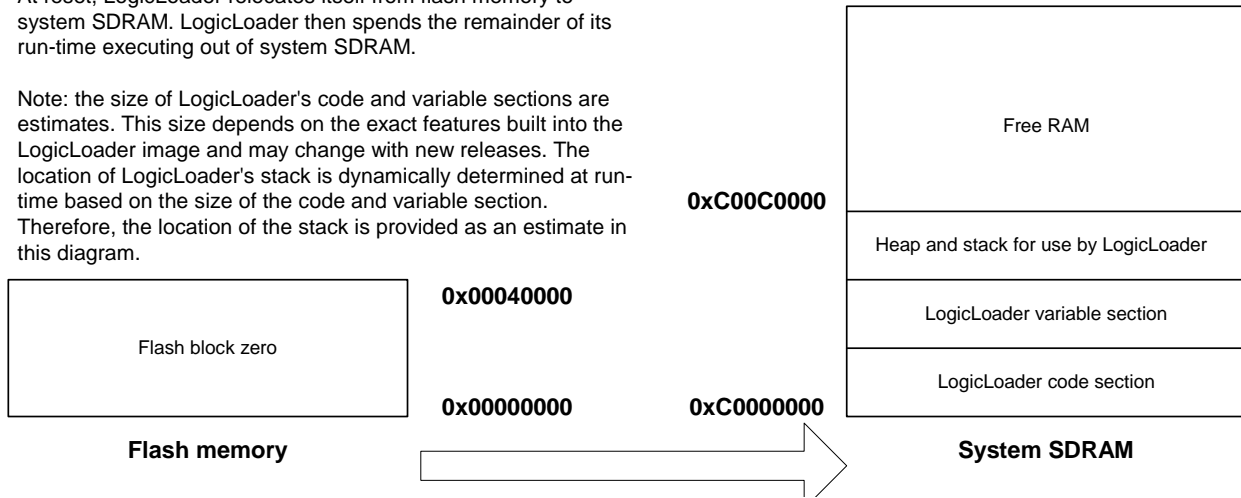


Figure 1.4: LogicLoader RAM Execution Environment

2 LH7A400-10 LogicLoader Functionality

2.1 Supported Hardware Peripherals

The table below lists LH7A400-10-specific peripherals supported by LogicLoader.

Hardware Peripheral	Support (Y/N)	Details
Audio	N	--
Display:	Y	LogicLoader supports 8 and 16 bits per pixel; custom displays can be supported by using the config block
LCD-3.5-QVGA-10	Y	Display kit with LCD part number LQ035Q7DB02
LCD-3.5-QVGA-20	Y	Display kit with LCD part number LQ035Q7DB02
LCD-5.7-QVGA-10	Y	Display kit with LCD part number LQ057Q3DC02
LCD-3.6-QVGA-10	Y	Display kit with LCD part number LQ036Q1DA01
LCD-6.4-VGA-10	Y	Display kit with LCD part number LQ64D343
LCD-10.4-VGA-10	Y	Display kit with LCD part number LQ10D368
LCD-12.1-SVGA-10	Y	Display kit with LCD part number LQ121S1DG41
Ethernet	Y	10/100MBit support; MAC address stored in dedicated serial EEPROM; static IP address can be supported by using the config block
Flash Memory	Y	NOR flash only
IrDA	N	--
Memory Card Expansion:	Y	CompactFlash memory cards are supported only. 16 -> 256MB CompactFlash memory cards have been verified.
IO Mode PCMCIA/ CF	N	--
Memory Mode CF	Y	Recommended: SanDisk, Toshiba, PNY
SD/MMC	Y	--
Smart Card	Y	--
Processor:		
Cache	Y	Copy-back mode
Clock	Y	200MHz CPU / 100MHz Bus
Power Management	N	--
MMU	Y	Use 'remap' command to access unmapped regions of memory
PS/2	N	--
RTC	N	--
SDRAM	Y	32 or 64 MBytes; CAS-2, auto sizing
SSP	N	--
Serial Port:		
UARTA	Y	115200 baud standard, RTS flow only; 2400 to 460800 baud can be supported by using the config block
UARTB	N	--
UARTC	N	--
Touch Screen	N	--
USB Host	N	--
USB Function	N	--
Misc:		
GPIO	Y	Use 'w' and 'x' commands to access data direction and data registers to control GPIO lines per register description in processor and IO Controller specification documents.
Status	Y	Toggles to show system "heartbeat"
Mode Line 2	Y	QuickBoot Feature details: LogicLoader will typically pause 500 mS to look for the 'q' key on UARTA. However, if the Mode Line 2 (uP_MODE2) is grounded, this 500 mS timeout is skipped and the boot script runs immediately.
Serial EEPROM	Y	128 bytes – use "echo" command to write to /dev/serial_eeprom

3 Disclaimer

Logic strives to provide the most up to date information. However, the list of supported features in this document is partial and subject to change.

The Supported Options list was created to describe the supported features for fully populated standard card engine builds. If the card engine in use is a custom build or has some hardware feature omitted, the commands related to those hardware features may not function.

If you need software support on demand, please contact Logic Product Development sales at: product.sales@logicpd.com.