DLP® LightCommander™ Digital Micromirror Device (DMD) Board Hardware Specification

Hardware Documentation

Logic // Products
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Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
1	RL, JCA	Initial release	KTL	04/15/10

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1 Introduction

The DLP LightCommander is a modular development kit that provides users the ability to optimize components to create a development experience best suited for their application needs. One of those components is the Digital Micromirror Device (DMD) board that contains the DLP5500 DMD. This Hardware Specification provides the technical details of the DMD board.

2 DMD Board Overview

2.1 DMD Board Block Diagram

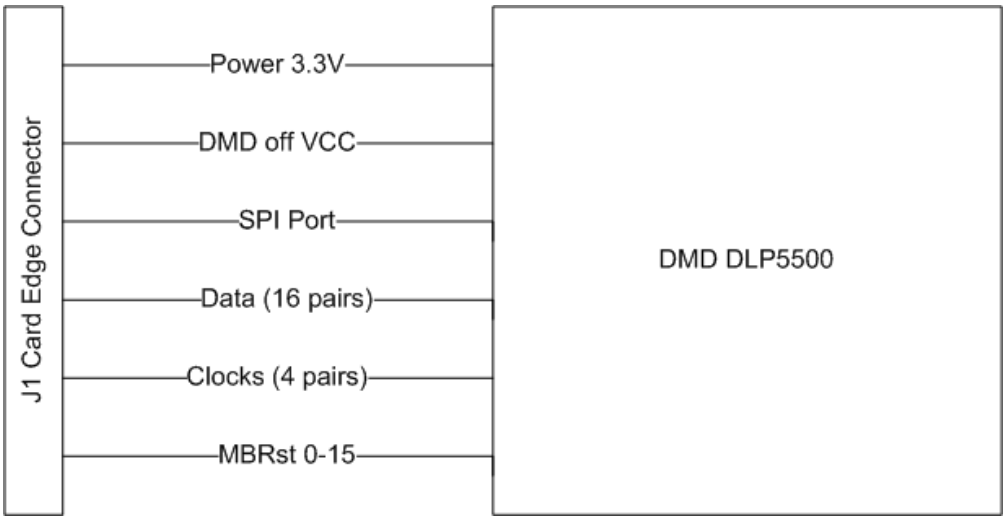


Figure 2.1: DMD Board Block Diagram

2.2 DLP5500 DMD Overview

The TI 0.55 XGA Series 450 (DLP5500) Digital Micromirror Device (DMD) is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP5500 can be used to modulate the amplitude, direction, and/or phase of incoming (illumination) light.

More details pertaining to the DLP5500 DMD can be found in TI documentation on the DLP5500 product page: www.ti.com and search for “DLP5500.”

3 DMD Board Operating Conditions

3.1 Absolute Power Maximum Ratings

The stress ratings in Table 3.1 are only for transient conditions. Operation at, or beyond, absolute maximum ratings conditions may affect reliability and cause permanent damage to the board and its components. The DMD is not designed to operate continuously at absolute maximum conditions.

These ratings are dependent on the DMD that is populated on the board. If a DMD other than DLP5500 is used, these ratings will need to be adjusted to that DMD’s specifications.

Table 3.1: Absolute Power Maximum Ratings

Parameter	Schematic Net Name	Rating	Unit	Notes
HVCMOS Supply Voltage	VCC_DMD_OFF	-0.5 to 9	V	1, 2
LVCMOS Supply Voltage	VCC_3P3V	-0.5 to 4	V	1, 2
Input Voltage (MBRST)	MBRST1:15	-28 to 28	V	1, 2
Input Voltage (Other)	All Inputs excluding MBRST1:15	-0.5 to VCC_3P3V + 0.3	V	1, 2, 3
High Level Output Current @V_{OH} = 2.4V: I_{OH}	DMD_DO	-20	mA	1
High Level Output Current @V_{OL} = 0.4V: I_{OL}	DMD_DO	15	mA	1

Notes:

1. Specification data taken from Texas Instruments' DLP5500 DMD Datasheet.
2. All voltages given with respect to DGND.
3. This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS differential inputs must not exceed 700mV or damage may occur to the internal termination resistors.

3.2 Recommended Power Operating Conditions

These ratings are dependent on the DMD that is populated on the board. If a DMD other than DLP5500 is used, these ratings will need to be adjusted to that DMD's specifications.

Table 3.2: Recommended Power Operating Conditions

Parameter	Schematic Net Name	Min	Typical	Max	Unit	Notes
HVCMOS Supply Voltage	VCC_DMD_OFF	8.25	8.5	8.75	V	1, 2
LVCMOS Supply Voltage	VCC_3P3V	3.0	3.3	3.6	V	1, 2
Input Voltage MBRST	MBRST1:15	-27	-	26.5	V	1, 2
LVCMOS Input VIH		1.7	2.5	VCC_3P3V + 0.3	V	1, 2
LVCMOS Input VIL		-0.3	-	0.7	V	1, 2

Notes:

1. Specification data taken from Texas Instruments' DLP5500 DMD Datasheet.
2. All voltages given with respect to DGND.

3.3 Environmental Specifications

These ratings are dependent on the DMD that is populated on the board. If a DMD other than DLP5500 is used, these ratings will need to be adjusted to that DMD's specifications.

Table 3.3: Environmental Specifications

Parameter	Min	Max	Unit
Operating Temperature	0	70	°C
Storage Temperature	-40	80	°C

3.4 Optical Specifications

The DLP5500 has an XGA resolution of 1024 x 768 pixels.

4 J1 Connector Pin Descriptions

The DMD board has a card edge with 140 gold-plated contacts that connects to the controller board. The following table provides the signals and descriptions for each of the 140 gold-plated contacts.

Table 4.1: J1 Connector Pin Descriptions

J1 Pin	Signal	I/O	Signal Type	Description
1	VCC_3P3V	I	LVCMOS	Power supply for low voltage CMOS logic in DMD.
2	DGND	I		Ground. Connect to digital ground.
3	VCC_3P3V	I	LVCMOS	Power supply for low voltage CMOS logic in DMD.
4	DMD_D_Bp15	I	LVDS	LVDS bus B data 15 positive.
5	DGND	I		Ground. Connect to digital ground.
6	DMD_D_Bn15	I	LVDS	LVDS bus B data 15 negative.
7	DMD_D_Bn13	I	LVDS	LVDS bus B data 13 negative.
8	DGND	I		Ground. Connect to digital ground.
9	DMD_D_Bp13	I	LVDS	LVDS bus B data 13 positive.
10	RFU	NC		Reserved for future use. Do not connect.
11	DGND	I		Ground. Connect to digital ground.
12	RFU	NC		Reserved for future use. Do not connect.
13	RFU	NC		Reserved for future use. Do not connect.
14	DGND	I		Ground. Connect to digital ground.
15	RFU	NC		Reserved for future use. Do not connect.
16	DMD_D_Bp11	I	LVDS	LVDS bus B data 11 positive.
17	DGND	I		Ground. Connect to digital ground.
18	DMD_D_Bn11	I	LVDS	LVDS bus B data 11 negative.
19	DMD_D_Bn9	I	LVDS	LVDS bus B data 9 negative.
20	DGND	I		Ground. Connect to digital ground.
21	DMD_D_Bp9	I	LVDS	LVDS bus B data 9 positive.
22	RFU	NC		Reserved for future use. Do not connect.
23	DGND	I		Ground. Connect to digital ground.
24	RFU	NC		Reserved for future use. Do not connect.
25	RFU	NC		Reserved for future use. Do not connect.
26	DGND	I		Ground. Connect to digital ground.
27	RFU	NC		Reserved for future use. Do not connect.
28	DMD_D_Bp7	I	LVDS	LVDS bus B data 7 positive.
29	DGND	I		Ground. Connect to digital ground.
30	DMD_D_Bn7	I	LVDS	LVDS bus B data 7 negative.
31	DMD_D_CLKBn	I	LVDS	LVDS bus B clock negative.
32	DGND	I		Ground. Connect to digital ground.
33	DMD_D_CLKBp	I	LVDS	LVDS bus B clock positive.
34	DMD_SCTRL_Bp	I	LVDS	LVDS bus B sync positive.
35	DGND	I		Ground. Connect to digital ground.
36	DMD_SCTRL_Bn	I	LVDS	LVDS bus B sync negative.
37	DMD_D_Bn5	I	LVDS	LVDS bus B data 5 negative.
38	DGND	I		Ground. Connect to digital ground.
39	DMD_D_Bp5	I	LVDS	LVDS bus B data 5 positive.

J1 Pin	Signal	I/O	Signal Type	Description
40	RFU	NC		Reserved for future use. Do not connect.
41	DGND	I		Ground. Connect to digital ground.
42	RFU	NC		Reserved for future use. Do not connect.
43	RFU	NC		Reserved for future use. Do not connect.
44	DGND	I		Ground. Connect to digital ground.
45	RFU	NC		Reserved for future use. Do not connect.
46	DMD_D_Bp3	I	LVDS	LVDS bus B data 3 positive.
47	DGND	I		Ground. Connect to digital ground.
48	DMD_D_Bn3	I	LVDS	LVDS bus B data 3 negative.
49	DMD_D_Bn1	I	LVDS	LVDS bus B data 1 negative.
50	DGND	I		Ground. Connect to digital ground.
51	DMD_D_Bp1	I	LVDS	LVDS bus B data 1 positive.
52	RFU	NC		Reserved for future use. Do not connect.
53	DGND	I		Ground. Connect to digital ground.
54	RFU	NC		Reserved for future use. Do not connect.
55	RFU	NC		Reserved for future use. Do not connect.
56	DGND	I		Ground. Connect to digital ground.
57	RFU	NC		Reserved for future use. Do not connect.
58	DMD_nPWRDN	I	LVCMOS	Active low reset signal.
59	DGND	I		Ground. Connect to digital ground.
60	DMD_SCP_DI	I	LVCMOS	SPI data input.
61	DMD_SCP_CLK	I	LVCMOS	SPI clock.
62	DMD_DO	O	LVCMOS	SPI data output.
63	DMD_SCP_nEN	I	LVCMOS	SPI chip enable.
64	MBRST0	I	HVCMOS	Mirror bias reset signal.
65	MBRST1	I	HVCMOS	Mirror bias reset signal.
66	MBRST2	I	HVCMOS	Mirror bias reset signal.
67	MBRST3	I	HVCMOS	Mirror bias reset signal.
68	MBRST4	I	HVCMOS	Mirror bias reset signal.
69	MBRST5	I	HVCMOS	Mirror bias reset signal.
70	MBRST6	I	HVCMOS	Mirror bias reset signal.
71	MBRST7	I	HVCMOS	Mirror bias reset signal.
72	MBRST14	I	HVCMOS	Mirror bias reset signal.
73	VCC_DMD_OFF	I	HVCMOS	Power for high voltage CMOS logic in DMD.
74	MBRST12	I	HVCMOS	Mirror bias reset signal.
75	VCC_DMD_OFF	I	HVCMOS	Power for high voltage CMOS logic in DMD.
76	DGND	I		Ground. Connect to digital ground.
77	MBRST15	I	HVCMOS	Mirror bias reset signal.
78	MBRST10	I	HVCMOS	Mirror bias reset signal.
79	MBRST13	I	HVCMOS	Mirror bias reset signal.
80	MBRST8	I	HVCMOS	Mirror bias reset signal.
81	MBRST11	I	HVCMOS	Mirror bias reset signal.
82	DGND	I		Ground. Connect to digital ground.
83	MBRST9	I	HVCMOS	Mirror bias reset signal.
84	RFU	NC		Reserved for future use. Do not connect.

J1 Pin	Signal	I/O	Signal Type	Description
85	DGND	I		Ground. Connect to digital ground.
86	RFU	NC		Reserved for future use. Do not connect.
87	RFU	NC		Reserved for future use. Do not connect.
88	DGND	I		Ground. Connect to digital ground.
89	RFU	NC		Reserved for future use. Do not connect.
90	DMD_D_Ap1	I	LVDS	LVDS bus A data 1 positive.
91	DGND	I		Ground. Connect to digital ground.
92	DMD_D_An1	I	LVDS	LVDS bus A data 1 negative.
93	DMD_D_An3	I	LVDS	LVDS bus A data 3 negative.
94	DGND	I		Ground. Connect to digital ground.
95	DMD_D_Ap3	I	LVDS	LVDS bus A data 3 positive.
96	RFU	NC		Reserved for future use. Do not connect.
97	DGND	I		Ground. Connect to digital ground.
98	RFU	NC		Reserved for future use. Do not connect.
99	RFU	NC		Reserved for future use. Do not connect.
100	DGND	I		Ground. Connect to digital ground.
101	RFU	NC		Reserved for future use. Do not connect.
102	DMD_D_Ap5	I	LVDS	LVDS bus A data 5 positive.
103	DGND	I		Ground. Connect to digital ground.
104	DMD_D_An5	I	LVDS	LVDS bus A data 5 negative.
105	DMD_SCTRL_An	I	LVDS	LVDS bus A sync negative.
106	DGND	I		Ground. Connect to digital ground.
107	DMD_SCTRL_Ap	I	LVDS	LVDS bus A sync positive.
108	DMD_D_CLKAp	I	LVDS	LVDS bus A clock positive.
109	DGND	I		Ground. Connect to digital ground.
110	DMD_D_CLKAn	I	LVDS	LVDS bus A clock negative.
111	DMD_D_An7	I	LVDS	LVDS bus A data 7 negative.
112	DGND	I		Ground. Connect to digital ground.
113	DMD_D_Ap7	I	LVDS	LVDS bus A data 7 positive.
114	RFU	NC		Reserved for future use. Do not connect.
115	DGND	I		Ground. Connect to digital ground.
116	RFU	NC		Reserved for future use. Do not connect.
117	RFU	NC		Reserved for future use. Do not connect.
118	DGND	I		Ground. Connect to digital ground.
119	RFU	NC		Reserved for future use. Do not connect.
120	DMD_D_Ap9	I	LVDS	LVDS bus A data 9 positive.
121	DGND	I		Ground. Connect to digital ground.
122	DMD_D_An9	I	LVDS	LVDS bus A data 9 negative.
123	DMD_D_An11	I	LVDS	LVDS bus A data 11 negative.
124	DGND	I		Ground. Connect to digital ground.
125	DMD_D_Ap11	I	LVDS	LVDS bus A data 11 positive.
126	RFU	NC		Reserved for future use. Do not connect.
127	DGND	I		Ground. Connect to digital ground.
128	RFU	NC		Reserved for future use. Do not connect.
129	RFU	NC		Reserved for future use. Do not connect.

J1 Pin	Signal	I/O	Signal Type	Description
130	DGND	I		Ground. Connect to digital ground.
131	RFU	NC		Reserved for future use. Do not connect.
132	DMD_D_Ap13	I	LVDS	LVDS bus A data 13 positive.
133	DGND	I		Ground. Connect to digital ground.
134	DMD_D_An13	I	LVDS	LVDS bus A data 13 negative.
135	DMD_D_An15	I	LVDS	LVDS bus A data 15 negative.
136	DGND	I		Ground. Connect to digital ground.
137	DMD_D_Ap15	I	LVDS	LVDS bus A data 15 positive.
138	VCC_3P3V	I	LVCMOS	Power supply for low voltage CMOS logic in DMD.
139	DGND	I		Ground. Connect to digital ground.
140	VCC_3P3V	I	LVCMOS	Power supply for low voltage CMOS logic in DMD.

5 DMD Board Mechanical Specifications

5.1 DMD Board Mechanical Characteristics

Table 5.1: DMD Board Size and Weight

Parameter	Min	Typical	Max	Unit
Dimensions	—	80(w) x 56(l)	—	mm
Weight	—	25	—	g

5.2 J1 Connector

The DMD board has a card edge with 140 gold-plated contacts (reference designator J1) to connect with the controller board. The controller board's mating connector is a Samtec mini edge-card socket. Samtec provides mechanical drawings of the surface mount footprint for this socket on their MEC8-DV Series product webpage.

Table 5.2: Gold Connector Information

Ref Designator	Manufacturer	Connector P/N	Mating Connector P/N	Product Webpage
J1	None	None	MEC8-170-02-L-DV	www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=MEC8-DV

5.3 DMD Socket

The DLP5500 DMD connects to the DMD board via a zero insertion force (ZIF) socket. The ZIF socket specification document can be found on Foxconn's website.

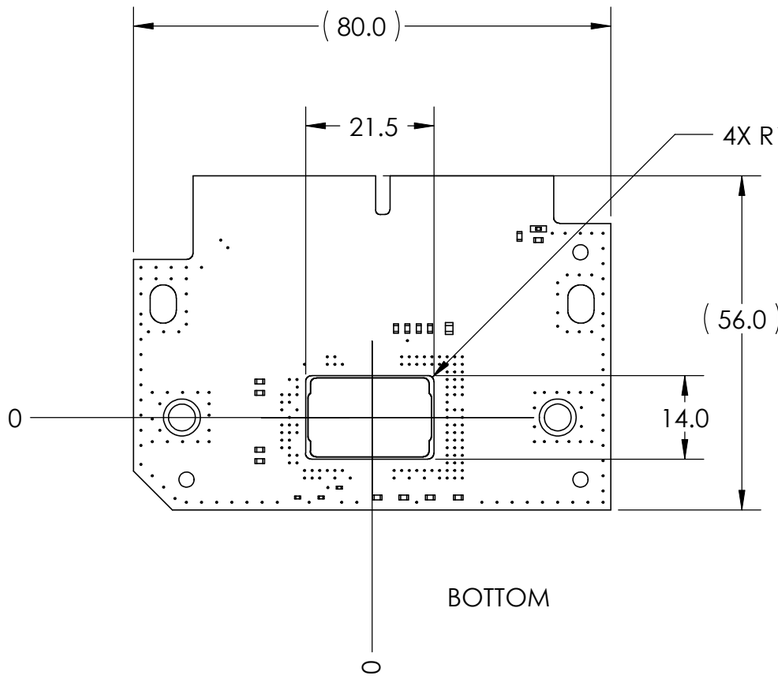
Table 5.3: DMD Socket Information

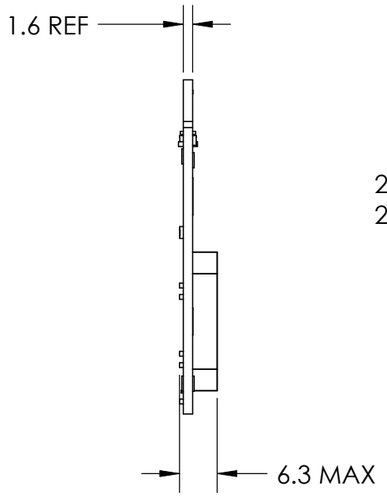
Ref Designator	Manufacturer	Connector P/N	Mating Connector P/N	Manufacturer Website
U1	Foxconn	PZ14927-1541-01F	DLP5500FYA (DMD)	www.foxconn.com/NWInG/products/default.asp

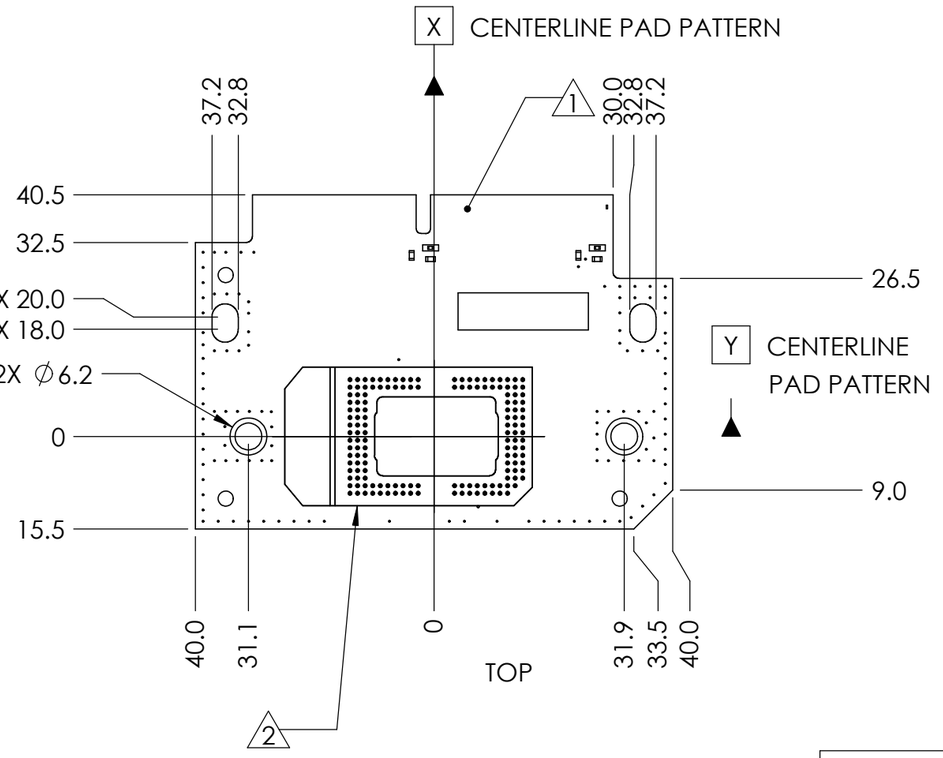
6 DMD Board Mechanical Drawings

The following page provides mechanical drawings of the DMD board.

REVISIONS			
REV.	ECO NUMBER	DESCRIPTION	DATE
1	-	INITIAL ENGINEERING RELEASE	04.14.10







NOTES:

1. CARD EDGE SPECIFICATION: REFER TO SAMTEC MEC8-170-02-L-DV RECOMMENDED MATING CARD LAYOUT
2. DMD SOCKET SPECIFICATION: FOXCONN PZ14927-1541-01F ALSO SEE TI DOCUMENT 2509474 FOR DETAILED DMD LOCATION SPECIFICATION
3. DO NOT SCALE DRAWING

THIS DRAWING PREPARED IN ACCORDANCE WITH ASME Y14.5-2000

ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE SPECIFIED

X	± 0.5
X.X	± 0.2
X.XX	± 0.1
X°	± 1°

THIRD ANGLE PROJECTION

ENG: KAG	DATE: 04.14.10	SIZE: B	TITLE: ASSEMBLY, DLP LIGHT COMMANDER DMD BOARD
CHECK: PMH	DATE: 04.14.10		REV: 1
MGR	DATE	SCALE: 1:1	DWG NO: 1015669
MANF	DATE		SHEET: 1 OF 1

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