Geode LX SOM-ETX Design Guideline

Application Note 301

Logic Product Development
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Abstract

This document serves as a guide for engineers designing custom ETX baseboards for the Geode LX SOM-ETX module.

REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
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1 Introduction

1.1 Objective

The intention of this Application Note is to serve as a guide for engineers designing custom baseboards (ETX carrier boards) for the Geode LX SOM-ETX module. This document provides reference schematics and descriptions for implementing the various Geode LX peripheral functions.

Further documentation: Please reference AMD's *Geode LX Processor Data Book* (publication ID 33234) and *Geode™ LX ETX Module Baseboard Design Guide* (publication ID 40586), both available from their Embedded Developer website (http://wwwd.amd.com/amd/developer.nsf/). Also available for reference are Logic's *Geode Mini-ITX Baseboard Schematic* (http://www.logicpd.com/downloads/807/) and *Geode LX SOM-ETX Schematic* (http://www.logicpd.com/downloads/804/).

1.2 Target Audience

This paper is intended for hardware engineers designing baseboards, ETX carrier boards, and custom application boards that will utilize the Geode LX SOM-ETX module.

1.3 Assumptions

It is assumed that the reader has an engineering background, as well as experience with personal computer buses and peripheral interfaces. A working knowledge of multi-layer printed circuit board (PCB) design practices is also assumed.

1.4 Scope

The circuits presented in this document are typical application circuits—it is possible that *they may not be suitable for all applications*. For example, additional components may need to be added to these circuits in order to meet specific Electro-static Discharge (ESD) or safety isolation requirements. Such regulations, and the techniques required to meet them, vary by industry and are beyond the scope of this document.

1.5 ETX Benefits

Logic Product Development's Geode LX SOM-ETX accelerates your product's time-to-market, and provides the following advantages:

- Product-ready hardware and software solutions allow immediate application development that results in a shorter product development cycle with less time, less cost, less risk… more innovation.
  - Less time—time to market solution allows software application development to begin immediately
  - Less cost—significantly lowers development cost
  - Less risk—complex portion of product design ready
  - More innovation—allows you to focus on other aspects of your design
- Common form factor footprint.
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle—worry free component obsolescence

- Low cost hardware solution—custom configurations are available to meet your design requirements and price points.

2 ETX Block Diagram

A block diagram of the Geode LX SOM-ETX is displayed below.

In the following sections of this document, each major component will be presented as it applies to its appropriate external connector (X1, X2, X3, X4).

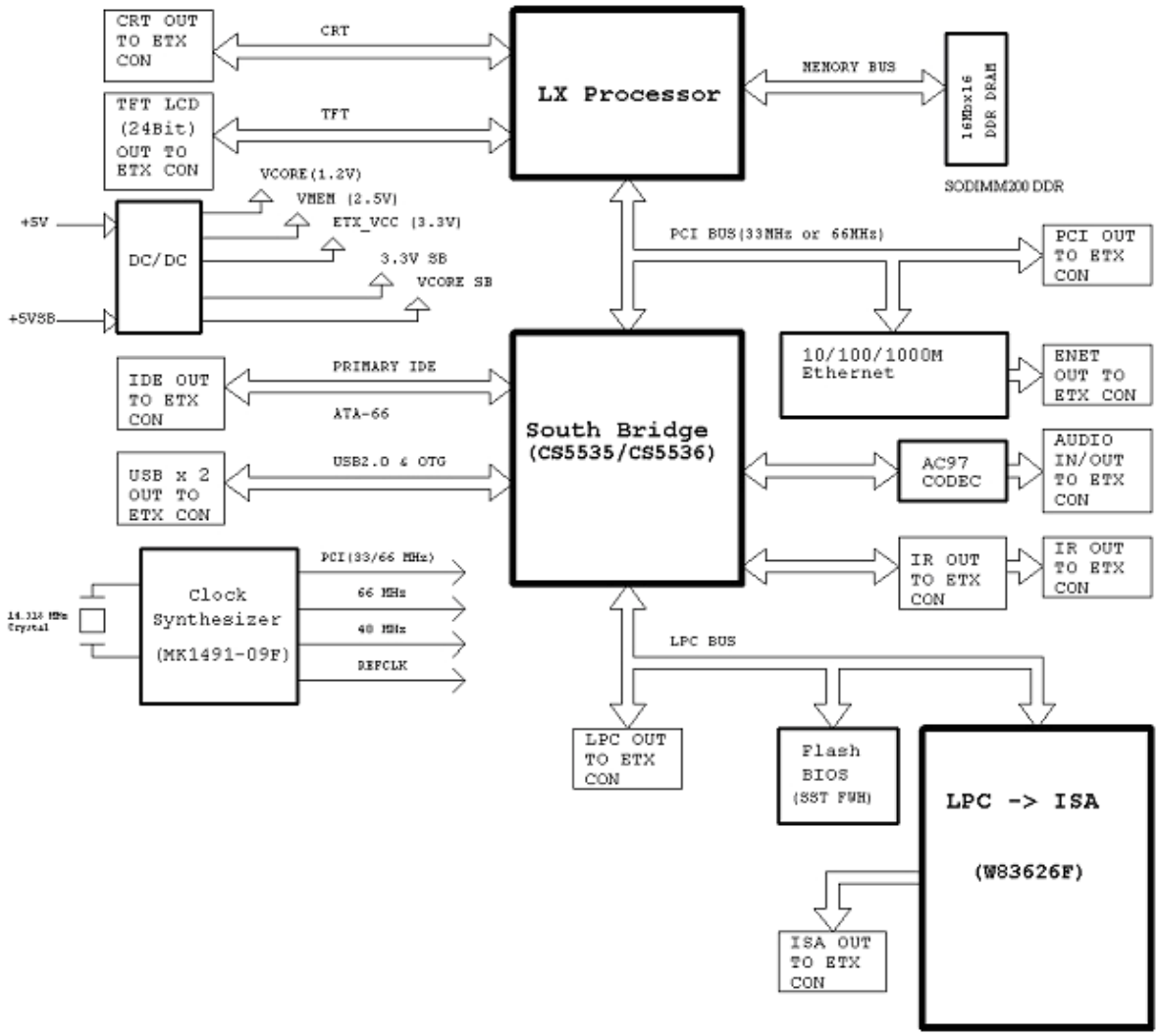

Figure 2.1: ETX Block Diagram

3 Power Supplies

The Geode LX SOM-ETX module requires only one voltage source for proper operation (5 V DC). The ETX module has onboard voltage regulators to create the other required voltages.

The ETX module requires two power supplies from the baseboard: 5 V and 5 VSB. 5 V should be provided to the ETX X1, X2, X3, and X4 connectors (J4, J5, J6, and J7 on ETX module PCB). The ATX 5VSB signal should be tied to X4 (J7) pin 3 net VCC5SB. Depending on the features installed, the Geode LX SOM-ETX module can expect to draw 1 A from the 5 VSB power source and 1.5 A from the 5 V power source under normal operating conditions. Current consumption will vary depending on peripheral usage. Please reference AMD's *Geode LX Processor Databook* for more detailed power estimates.

If a 5 V DC power source is used, proper supply should be allotted for all peripheral devices that may load it. For example, USB host ports each must be able to supply a maximum of 500 mA. The Geode LX SOM-ETX is capable of supporting four USB 2.0 host ports: 500 mA × 4(ports) = 2 A at 5 V.

ETX connector X1 (J4 on ETX module PCB) pins 12, 16, and 24 are intended to supply 3.3 V to a baseboard module for low current needs. The maximum allowed combined load is 500 mA.

NOTE: Do not connect the 3.3 V pins to an external power supply—they are output from the ETX module. If this occurs, the ETX module will be permanently damaged.

4 ATX Power Control Circuitry

The ATX power control circuit can be used to control the power on/off functions of the supply. The 5VSB signal provides standby power to the board only powering the power on/off circuitry. The PWRBTN# signal (X4 – J7.7) will enable the PS_ON# output when a rising edge is seen on the PWRBTN# signal and the Geode LX SOM-ETX module is in an off state. The PWRBTN# signal is pulled up to the VCC3SB supply on the module.

A custom baseboard can tie a momentary push button switch to the PWRBTN# signal and to ground to complete the power on/off circuitry. The PS_ON# signal is an output from the ETX module that can be connected to a standard ATX supply's PS_ON# signal to turn on the supply. Please reference the Geode LX Mini-ITX design schematics, located on AMD's developer website (http://wwwd.amd.com/amd/developer.nsf/), for an implementation example.

5 Reset, Power Monitor

Reset can be invoked by driving the SYS_RST# signal (X4 – J7.11) low. This can be implemented with a simple momentary push button switch tied to ground.

The PCI_RST# output signal (X1 – J4.93) is driven low when the ETX module is in reset. This signal can be used to reset custom baseboard components, typically PCI-type components.

6 Clocking Options

Please reference AMD's *Geode LX Processor Data Book* for specific details on ETX module clock states.

The external bus and PCI bus operate at 33 MHz or 66 MHz, depending on the speed of the PCI devices. If SEL66_33# (X3 – J6.52) is high, the bus will operate at 66 MHz; if SEL66_33# is low, the bus will operate at 33 MHz.

The PCI bus is not asynchronous. It will operate at the speed of the lowest PCI device on the bus. If the slowest device designed in, or used by, a PCI card is 33 MHz the entire PCI bus will operate at 33 MHz. Careful considerations should be taken about overall bus performance if a 33 MHz PCI device is to be used. A PCI–PCI slot expander card circumvents this issue by utilizing an asynchronous PCI–PCI bridge and is included with the AMD Geode LX DB800 Development Kit from Logic.

The CPU multiplier controls the internal speed core and memory clocks. Its settings are determined either by the default settings in the BIOS or by user-defined settings modified in the BIOS. For a drawing of the clock generator circuit, please reference the *Geode LX SOM-ETX Schematic*, available for download at: http://www.logicpd.com/downloads/804/.

7 DDR RAM

The Geode LX SOM-ETX module supports up to 512 MB of PC3200 DDR SDRAM in a SODIMM form factor. None of the DDR SDRAM signals go off-board. For more information on the DDR SDRAM interface, please see AMD's *Geode LX Processor Data Book*.

8 Connector X1 (PCI, USB, Audio)

Of the 100 pins available on connector X1, the assignments are described in the table below. For a drawing of the X1 connector, please reference the *Geode LX SOM-ETX Schematic*, available for download at: http://www.logicpd.com/downloads/804/. For a drawing of a typical PCI connector, please reference Logic's *Geode Mini-ITX Baseboard Schematic*, available for download at: http://www.logicpd.com/downloads/807/.

Assignment	Number of Pins	Description
Power/GND/No Connect Signals		
5V	6	Input 5 V ± 0.25 V
3.3V	3	Output 3.3 V ± 0.165 V; 500 mA max load
Gnd	10	Input, Digital Ground
VCCSA	1	Output 3.3 VA ± 0.165 VA for audio reference voltage
AGND_AUDIO	1	Analog Ground for audio interface
NC	12	Not connected
PCI Signals		
AD[31:0]	32	This is the PCI multiplexed Address and Data Bus.
C/BE#[3:0]	4	These are the PCI Command/Byte Enables.
PAR	1	This is the composite Parity bit for the AD[31:0] and the C/BE# bits. (Even Parity)
PCI_RST#	1	Active Low. When active, resets all PCI devices.
CLK_EXT	1	An individual clock line for an external PCI slot.

Assignment	Number of Pins	Description
REQ1#_PCI0	1	Active Low, a combination Bus Request and Bus Grant pair for an external slot. When a device wishes to become a Master and use the PCI Bus, it must first assert its Bus Request to the arbiter. (The arbiter is contained within the Geode LX processor.) When it receives a Bus Grant, it may drive the Bus.
GNT1#_PCI0	1	Active Low, a combination Bus Request and Bus Grant pair for an external slot. When a device wishes to become a Master and use the PCI Bus, it must first assert its Bus Request to the arbiter. (The arbiter is contained within the AMD Geode LX processor.) When it receives a Bus Grant, it may drive the Bus.
INTA#	1	Active Low AMD Geode CS553x companion chip GPIO0. This signal is also connected to AMD Geode LX INTA#. Should be tied to PCI slot INTA#.
INTB#	1	Active Low AMD Geode CS553x companion chip GPIO7. Should be tied to PCI slot INTB#.
INTC#	1	Active Low AMD Geode CS553x companion chip GPIO12. Should be tied to PCI slot INTC#.
INTD#_SLPBUT	1	Active Low AMD Geode CS553x companion chip GPIO13/SLEEP_BUT. Should be tied to PCI slot INTD#. Note: This signal can alternately be used to put the system to sleep.
FRAME#	1	Active Low. The initiator asserts this signal to begin an operation.
DEVSEL#	1	Active Low. The target asserts this signal to indicate that its address space has been selected.
IRDY#	1	Active Low. Initiator Ready is the initiators response to a read or a write.
TRDY#	1	Active Low. Target Ready is the target's response to a read or a write.
STOP#	1	Active Low. The target will assert this signal to request the initiator to stop the operation.
SERIRQ	1	This is the serial interrupt request.
PME#	1	Active Low. This pin is for a power management event.
USB Signals		
USBPWR_EN[2:1]	2	Active High. These signals are intended to be used to enable an external USB power source. When low, the external power source is off.
USB[3:0]-	4	These are the negative differential side of the USB data.
USB[3:0]+	4	These are the positive differential side of the USB data.
Audio Signals		
LINE_IN_L	1	This is the auxiliary input left.
LINE_IN_R	1	This is the auxiliary input right.
MIC	1	Microphone input.
HP_OUT_L	1	This is the line-level stereo out left.
HP_OUT_R	1	This is the line-level stereo out right.

8.1 PCI Slot Differences

For details on PCI design please reference the most recent release of the PCI Local Bus specification. At the time of this writing, PCI Local Bus Specification v. 2.2 was current.

The following is an excerpt from AMD's document, *AMD Geode™ LX ETX Module Baseboard Design Guide* (publication ID 40586):

> “Support for 5V PCI cards will require a level translator. The processor supports up to three external masters. Two of the three are used by on-board devices. The CS553x companion chip uses one and the Ethernet interface uses the other. Therefore, the ETX module supports one additional REQ/GNT pair. This may be expanded through the use of an external device to allow for additional masters. Refer to the application note *AMD Geode™ GX Processors Request/Grant Pair Expansion* (publication ID 32319). This application note may be used on the Geode LX processor as well. Devices that do not support 66 MHz PCI bus clock frequency must assert SEL66_33# low. This is pin B49 on the PCI connector. The processor (and the ETX specification) does not support PCI_LOCK#, PCI_PERR#, or PCI_SERR#. These signals must be pulled up to 3.3V with individual 10K ohm resistors on baseboard devices that have these features (including PCI slots).”

Most PCI signals are connected in parallel to all the slots or devices. The exceptions are the following pins from each slot or device.

8.1.1 IDSEL

The IDSEL signal is connected to a different AD line for each slot. AD23 is connected to the Ethernet controller on the Geode LX ETX module. AD25 is connected to the AMD Geode CS553x companion chip on the Geode LX ETX module. AD24 represents slot 3 and is available to the baseboard and should be used for the PCI connector.

8.1.2 PCI_CLK

The PCI_CLK signal is connected to a different ETX PCI clock signal for each slot. CLK_EXT is available to the baseboard and is intended for use on slot 3.

The trace length for all PCI clocks should be matched and controlled. PCI clock routes should be separated as far from other signal traces as possible. PCI clock signals should be routed as controlled-impedance traces, with trace impedance in the 60 Ohm to 70 Ohm range. Only one PCI device or slot should be driven from each ETX PCI clock output.

8.1.3 PCI_INT

Most PCI devices use INTA# only and do not require a connection for INTB#, INTC#, or INTD#. However, for maximum flexibility all PCI_INT# signals should be routed to the external slots. On the ETX module, INTA# is connected to the AMD Geode CS553x companion chip GPIO0. INTB# is connected to the AMD Geode CS553x companion chip GPIO7. INTC# is connected through the AMD Geode CS553x companion chip GPIO12. INTD#_SLPBUT is connected to the AMD Geode CS553x companion chip GPIO13/SLEEP_BUT.

8.2 USB 2.0 High Speed Host Ports

There are four pairs of USB high-speed differential signals. Special care must be taken when routing these signals on the custom designed baseboard. Please refer to the USB 2.0 specification v. 2.0 (www.usb.org) for details and PCB layout guidelines. Failure to follow the recommended guidelines will result in unreliable operation.

The four pairs are:

- USB0+ and USB0-
- USB1+ and USB1-
- USB2+ and USB2-
- USB3+ and USB3- (if using the CS5536 companion chip, this port can operate as a host or device port)

The USB controller used on the ETX is contained in the AMD Geode CS553x companion chip and is connected to the PCI interface on the Geode LX as Device ID = 25. It operates as a 32-bit

66 MHz device. **Please note:** Only the CS5536 companion chip supports USB 2.0 and USB Function or Host on port USB3.

The following is an excerpt from AMD's document, *AMD Geode™ LX ETX Module Baseboard Design Guide* (publication ID 40586):

> "Because of the sub-optimal pin assignments on the ETX connector for USB 2.0 High Speed mode, this module does not provide for USB ports 0 and 1 on the ETX connector and are instead routed to a separate header. This header is pin-compatible with most chassis-mounted USB connector assemblies. To use these ports on the baseboard, this header will have to be added to a baseboard design and an appropriate cable assembly will need to be part of the overall system."

There are two USBPWR_ENx signals that can be used to control power to any of the four ports. The signal USB_OC# (X4 – J7.19) is shared by all four ports and is an output from the power control devices to indicate that an over-current condition has occurred. For drawings that depict a dual-host port implementation example and a quad-host port implementation example, please refer to Logic's *Geode Mini-ITX Baseboard Schematic*, available for download at: http://www.logicpd.com/downloads/807/.

8.3 Audio

Microphone-in, line-in, and headphone-out are provided, as well as SPDIF-in and -out.

9 Connector X2 (ISA, LPC, Audio)

According to the ETX standard, this connector is generally dedicated to signals associated with ISA bus devices. Of the 100 pins available on connector X2, the assignments are described in the table below. For a drawing of the X2 connector, please reference the *Geode LX SOM-ETX Schematic*, available for download at: http://www.logicpd.com/downloads/804/.

Assignment	Number of Pins	Description
Power/GND/No Connect Signals		
5V	4	Input, 5 V ± 0.25 V
Gnd	8	Input, Digital Ground
NC	3	Not Connected
ISA Signals		
ISA_SA[19:0]	20	Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory.
ISA_SD[15:0]	16	Data bits for any peripheral device.
ISA_MASTER#	1	This signal allows a bus master to gain control of the system address, data, and control lines.
ISA_DREQ[6:5,2:0]	5	Active High. DMA controller request.
ISA_DACK[6:5,2:0]#	5	Active Low. DMA controller acknowledge.
ISA_IRQ[12:9,5:3]	7	Active High. ISA Interrupt requests.
ISA_IOCHRDY	1	This is the I/O channel ready signal. It can be pulled low to extend read or write cycles on the bus when required.
ISA_AEN	1	Active High. This signal indicates a DMA transfer cycle.
ISA_BALE	1	Active High. BALE is a pulse generated at the beginning of any bus cycle initiated by a CPU module.

Assignment	Number of Pins	Description
ISA_IOR#	1	Active Low. I/O read indicates a read cycle to an I/O device.
ISA_IOW#	1	Active Low. I/O write indicates a write cycle to an I/O device.
ISA_MEMR#	1	Active Low. Memory read indicates a read cycle to a memory device.
ISA_MEMW#	1	Active Low. Memory write indicates a write cycle to a memory device.
ISA_RSTDRV	1	Active High. This is the reset for all devices on the ISA bus.
ISA_SBHE#	1	Bus High Enable is used to indicate a data transfer on the upper byte of the data bus.
ISA_IOCS16#	1	This signal determines if a 16-bit to 8-bit conversion is needed for memory bus cycles. When high, 16-bit CPU cycles are converted to two 8-bit cycles. When low, access to peripherals is done at 16-bit width.
ISA_14.318CLKOUT	1	14.31818 MHz frequency output.
ISA_TC	1	Active High. Indicates one of the DMA channels has transferred all data.
ISA_SYSCLK	1	This output clock frequency is 8.25 MHz.
LPC Signals		
LAD[3:0]	4	Low pin count (LPC) bus. Address, control, and data information is provided on these signals.
LFRAME#	1	Indicates the start or termination of a cycle on the LPC bus.
LDRQ#	1	DMA request on the LPC bus.
CLK_LPC_EXT	1	External LPC clock. Operates at 33 MHz.
Audio Signals		
SPDIF_IN	1	S/PDIF audio input.
SPDIF_OUT	1	S/PDIF audio output.

9.1 ISA – Populated on Select ETX Assemblies

The ISA bus on the Geode LX is created through the use of Winbond's W83626F LPC-to-ISA Bridge chip. This chip provides a transparent LPC-to-ISA bus conversion but with some limitations. The following is an excerpt from AMD's document, *AMD Geode™ LX ETX Module Baseboard Design Guide* (publication ID 40586):

> "ISA is supported through a bridge from the LPC bus. There are limitations to the level of ISA support. Only 8-bit DMA is supported. In addition, the CS5536 has an issue in regards to LPC-to-ISA bridges that try to take advantage of the subtractive decode feature of the LPC bus. Refer to AMD Geode™ CS5535/CS5536 Companion Devices LPC-to-ISA Bridge (publication ID 33329). When using DMA, only one device (LPC-ISA bridge or LPC-SIO) may use LDRQ#. Some of the signals on the ISA connector (X2) have been reassigned."

9.2 LPC

The Geode LX implements a Low Pin Count (LPC) interface through the Geode CS553x companion chip.

10 Connector X3 (Video, VGA, TFT, IrDA)

The purpose of this connector is to provide access to the video display, flat panel display, and IrDA available from the Geode LX. Of the 100 pins available on connector X3, the assignments are described in the table below. For a drawing of the X3 connector, please reference the *Geode LX SOM-ETX Schematic*, available for download at: http://www.logicpd.com/downloads/804/.

Assignment	Number of Pins	Description
Power/GND/No Connect Signals		
5V	5	Input, 5 V ± 0.25 V
Gnd	15	Input, Digital Ground
NC	47	Not connected
Video Signals		
AGND_VGA	1	Analog Ground for video interface
CRT_SCL, CRT_SDA	2	I2C bus from video controller
RED, BLUE, GREEN, HSYNC, VSYNC	5	CRT video pins
DRGB[23:18,15:10,7:2]	18	Video data bits
Clock Signals		
TV_DOT_CLK	1	Dot clock input
DOTCLK_SEL	1	Dot clock select. Selects between TV_DOT_CLK and CLK_48_DOT
CLK_48_SIO	1	48 MHz clock output
CLK_LPC_SIO	1	33 MHz clock output
IrDA Signals		
IOC_IRRX	1	Infrared receive signal
IOC_IRTX	1	Infrared transmit signal
PCI Signals		
SEL66_33#	1	PCI bus speed select. When high, bus operates at 66 MHz. When low, bus operates at 33 MHz.

10.1 Video

The video controller used on the Geode LX SOM-ETX is integrated into the AMD LX processor. It provides capability to simultaneously operate LCD/CRT and LCD/TV display combinations. It contains up to 32 MB of shared video memory (shared with the main system DDR SDRAM).

The Insyde BIOS has support for the following Zoom Display kits:

- 12.1” 800 x 600 Zoom Display Kit

Visit http://www.logicpd.com/eps/displaykits/LCD-12.1-SVGA-10/ for more information on available display kits.

10.2 Video Processor

10.2.1 CRT

The CRT interface on the Geode LX provides support for CRT resolutions up to:

- 1920 x 1440 x 32 bpp at 85 Hz
- 1600 x 1200 x 32 bpp at 100 Hz

For a drawing of a CRT interface example, please reference Logic’s *Geode Mini-ITX Baseboard Schematic*, available for download at: http://www.logicpd.com/downloads/807/.

10.2.2 TFT

The TFT controller on the Geode LX converts video data into digital output suitable for driving a TFT flat panel LCD. The output supports the industry standard 18-bit or 24-bit active matrix thin film transistor (TFT). It supports panels up to a 24-bit interface and up to a 1600 x 1200 resolution.

10.2.3 VIP/VOP

This module provides connectivity to the baseboard for the VIP/VOP (DRGB) signals from the processor. Some signals on the ETX connector have been reassigned to provide this feature.

10.3 IrDA

The Geode LX offers IrDA signals through the Geode CS553x companion chip. The IrDA interface supports SIR, ASK-IR, and DASK-IR.

11 Connector X4 (Ethernet, SMBUS, Power Control, VIP, IDE)

The purpose of this connector is to provide access to the Ethernet, I2C, power control, video, and IDE available from the Geode LX. Of the 100 pins available on connector X4, the assignments are described in the table below. For a drawing of the X4 connector, please reference the *Geode LX SOM-ETX Schematic*, available for download at: http://www.logicpd.com/downloads/804/.

Assignment	Number of Pins	Description
Power/GND/No Connect Signals		
5V	6	Input, 5 V ± 0.25 V
VCC5SB	1	Input, 5 V ± 0.25 V, Connect to a 5 V, 500 mA SB source if available, if not then connect to 5 V main rail.
VBAT	1	Input, 3 V backup cell input, typically connected to a 3 V lithium backup cell for RTC operation and CMOS register non-volatility in the absence of system power.
V_DAC	1	Output, connect to center tap on some Ethernet magnetics.
AGND_ENET	1	Analog Ground for Ethernet interface
Gnd	7	Input, Digital Ground
NC	1	Not connected
Ethernet Signals		
ENETTX+_BIDA+ ENETTX-_BIDA-	2	This is the first Ethernet pair in 1000 Base-T. It is the transmit pair in 10 Base-T and 100 Base-TX.
ENETRD+_BIDB+ ENETRD-_BIDB-	2	This is the second Ethernet pair in 1000 Base-T. It is the receive pair in 10 Base-T and 100 Base-TX.
BIDC+ BIDC-	2	This is the third Ethernet pair in 1000 Base-T.
BIDD+ BIDD-	2	This is the fourth Ethernet pair in 1000 Base-T.
LED0_L10M LED1_L100M LED2_FULL LED3_L1G	4	These are the LED signals for Ethernet.
Video Signals		

Assignment	Number of Pins	Description
DRGB[31:24,17,16, 9,8,1,0]	14	Video data bits
VIP[7:0]	8	Video input port data lines.
VIPCLK, VIPSYNC	2	Video input port control signals.
LDEMOD_VIPVSYNC	1	This signal is either the flat panel display enable or the video input port vertical sync signal.
DISPEN_VOPBLANK	1	This signal can be either the flat panel backlight display enable or the video out port blank signal.
VDDEN_VIPHSYNC	1	This signal can be either the LCD VDD enable or the video input port horizontal sync signal.
IDE Signals		
PIDE_D[15:0]	16	IDE data bus.
PIDE_A[2:0]	3	IDE address bus.
IDE_CABLEID	1	This signal allows the system to determine if high-speed transfer modes should be enabled.
PIDE_RST#, PIDE_DRQ, PIDE_IOW#, PIDE_IOR#, PIDE_RDY, PIDE_ACK#, PIDE_INTRQ, PIDE_CS#[1:0]	9	IDE control signals.
GPIO6	1	General purpose I/O connected to the CS553x companion chip.
LOW_BAT#	1	This signal is a low battery detect.
MFGPT7_C1	1	General purpose counter #7.
DOTCLK_VOPCLK	1	DOT clock output.
SMBUS Signals		
SMB_SCL, SMB_SDA	2	System Management Bus (SMBUS)
USB Signals		
USB_ID	1	USB_ID is used to determine which kind of plug is connected to the USB receptacle.
USB_VBUS	1	This signal is the USB bus voltage.
Misc. Signals		
WORK_AUX	1	This signal is meant to control all external power sources except memory power sources.
PS_ON#, PWRBTN#	2	ATX power supply support
USB_OC#	1	USB over current sense
SYS_RST#	1	Active low. Board reset input.
PCBEEP	1	This is the legacy PC/AT speaker beep.

11.1 Ethernet

A Realtek RTL8110SB Gigabit Ethernet controller is provided to give connectivity to one 10/100/1000 Ethernet port. It is intended that the isolation magnetics be contained on the baseboard. The Realtek recommended device for the magnetics is Pulse Engineer's H5007, but other manufacturers exist.

NOTE: Implementing this interface on baseboards requires the data signals on both sides of the transformer to be routed as differential pairs, which match the impedance characteristics and follow all other differential pair layout considerations. Please refer to Realtek's reference design *RTL8100C & RTL8110S(B/C) co-lay application circuits* for details. (http://www.realtek.com.tw/, search for "RTL8110SB" and navigate to the "Downloads" section to find the downloadable .pdf of the reference design.)

11.2 IDE

The IDE interface on the Geode LX SOM-ETX is controlled by the Geode CS553x companion chip and is connected to the primary port on the ETX connector. It is compliant with ATA-5 specifications. The IDE interface supports one channel, two devices. Care must be taken in designing a baseboard intended to either support modules with a secondary IDE port or this module. 100 MB/s transfer speeds require an 80-conductor cable and careful layout of the IDE traces on the baseboard.

11.3 SMBUS

System Management Bus (SMBUS) is a two-wire, bi-directional serial bus, which provides a simple, efficient method of data exchange between devices. This two-wire bus minimizes the interconnection between the devices.

The interface is designed to operate up to 100 KHz with maximum bus loading and timing. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pf.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

The SMBUS clock line is available at X4 (J7.23).
The SMBUS data line is available at X4 (J7.24).

11.4 Power Control

In order to comply with the ETX power control standard, the Geode LX provides circuitry to control an ATX power supply. It involves the implementation of three signals: the push button input, the power-on control output, and the 5V_SB voltage line, which is used to power this circuitry even though the power may be off.

12 Additional Features

12.1 CompactFlash

This connector provides connectivity to CompactFlash memory devices. The CompactFlash card is intended to operate in TrueIDE mode - hot-swapping functionality is not available. For a drawing of the CompactFlash connector, please reference Logic's *Geode Mini-ITX Baseboard Schematic*, available for download at: http://www.logicpd.com/downloads/807/. Please contact Logic Product Development for more details on this interface.

12.2 PS/2 Keyboard and Mouse

These functions are expected to be provided by the baseboard through the use of a SIO on LPC.

12.3 Floppy

This function is expected to be provided by the baseboard through the use of a SIO on LPC.

12.4 Parallel Port

This function is expected to be provided by the baseboard through the use of a SIO on LPC.

13 Deviations from the ETX Standard

There are some differences between the ETX standard v3.0 SOM pinout and the design of the LX SOM-ETX. Great care has been taken to ensure that the power and ground connections are the same; and pins assigned as inputs, if used, are still inputs and pins assigned as outputs, if used, are still outputs. No damage will result if the Geode LX SOM-ETX is inserted into a standard ETX baseboard. The table below summarizes all pin differences between the ETX Standard v3.0 and the LX SOM-ETX.

X1		
Pin	**ETX Spec v3.0**	**LX SOM-ETX**
X1-3	PCICLK3	NC
X1-4	PCICLK4	NC
X1-8	PCICLK2	NC
X1-9	PCI REQ3#	NC
X1-10	PCI GNT3#	NC
X1-11	PCI GNT2#	NC
X1-13	PCI REQ2#	NC
X1-14	PCI GNT1#	NC
X1-15	PCI REQ1#	NC
X1-54	PCI SERR#	NC
X1-55	PCI GPER#	NC
X1-59	LOCK#	NC
X1-76	USB0#	NC
X1-80	USB1#	NC
X1-88	USB0	NC
X1-92	USB1	NC
X1-18	RESERVED	USBPWR_EN1
X1-56	RESERVED	USBPWR_EN2

X2		
Pin	**ETX Spec v3.0**	**LX SOM-ETX**
X2-38	ISA M16#	NC
X2-62	ISA REFSH#	NC
X2-97	ISA IOCHK#	NC
X2-8	DREQ7	Y-BL
X2-10	DACK7#	X-TL
X2-21	LA17	LAD0
X2-23	LA18	LAD1
X2-24	IRQ14	X+BR
X2-25	LA19	LAD2
X2-26	IRQ15	X+TR
X2-27	LA20	LAD3
X2-29	LA21	LFRAME#
X2-31	LA22	LDRQ#
X2-33	LA23	CLK_LPC_EXT
X2-56	IRQ6	SPDIF_IN
X2-58	IRQ7	SPDIF_OUT
X2-70	DREQ3	COMP2
X2-72	DACK3#	COMP1
X2-80	SMEMR#	WIPER
X2-86	SMEMW#	PENDOWN
X2-90	NOWS#	BATMON

X3		
Pin	**ETX Spec v3.0**	**LX SOM-ETX**
X3-14	LCDD019	NC
X3-42	LCD LTGIO0	NC
X3-45	LCD BIASON	NC
X3-46	LCD DIGON	NC
X3-47	Video COMP	NC
X3-48	Video Y	NC
X3-49	Video SYNC	NC
X3-50	Video C	NC
X3-51	LPT/FLPY#	NC
X3-55	LPT – STB#	NC
X3-56	LPT – AFD#	NC
X3-57	RESERVED	NC
X3-58	LPT - PD7	NC
X3-60	LPT – ERR#	NC

X4		
Pin	**ETX Spec v3.0**	**LX SOM-ETX**
X4-9	KBINH	NC
X4-4	PWGIN	LDEMOD_VIPSYNC
X4-10	LILED#	LED1_L100M
X4-13	ROMKBCS#	USB_ID
X4-15	EXT_PRG	MFGPT7_C1
X4-16	I2CLK	USB_VBUS
X4-20	GPCS#	WORK_AUX
X4-21	EXTSMI#	DOTCLK_VOPCLK
X4-22	I2DAT	LED3_L1G
X4-25	SIDE_CS3#	VIPCLK
X4-26	SMBALRT#	DISPEN_VOPBLANK
X4-27	SIDE_CS1#	VIPSYNC
X4-28	DASP_S	VDDEN_VIPHSYNC
X4-29	SIDE_A2	VIP0

X3-62	LPT - PD6	NC
X3-63	RXD2	NC
X3-64	LPT – INIT#	NC
X3-67	RTS2#	NC
X3-68	LPT - PD5	NC
X3-69	DTR2#	NC
X3-70	LPT - SLIN#	NC
X3-71	DCD2#	NC
X3-72	LPT - PD4	NC
X3-73	DSR2#	NC
X3-74	LPT - PD3	NC
X3-75	CTS2#	NC
X3-76	LPT - PD2	NC
X3-77	TXD2	NC
X3-78	LPT - PD1	NC
X3-79	RI2#	NC
X3-80	LPT - PD0	NC
X3-83	RXD1	NC
X3-84	LPT – ACK#	NC
X3-85	RTS1#	NC
X3-86	LPT - BUSK#	NC
X3-87	DTR1#	NC
X3-88	LPT – PE	NC
X3-89	DCD1#	NC
X3-90	LPT - SLCT#	NC
X3-91	DSR1#	NC
X3-92	MSCLK	NC
X3-93	CTS1#	NC
X3-94	MSDAT	NC
X3-95	TXD1	NC
X3-96	KBCLK	NC
X3-97	RI1	NC
X3-98	KBDAT	NC
X3-9	DETECT#	TV_DOT_CLK
X3-12	LCDD018	AGND_VGA
X3-41	JILI_DAT	CLK_48_SIO
X3-43	JILI_CLK	CLK_LPC_SIO

X4-31	SIDE_A0	VIP1
X4-35	PDIAG_S	VIP2
X4-37	SIDE_A1	VIP3
X4-39	SIDE_INTRQ	VIP4
X4-43	SIDE_AK#	VIP5
X4-45	SIDE_RDY	VIP6
X4-47	SIDE_IOR#	VIP7
X4-51	SIDE_IOW#	DRGB0
X4-53	SIDE_DRQ	DRGB1
X4-55	SIDE_D15	DRGB8
X4-57	SIDE_D0	DRGB9
X4-59	SIDE_D14	DRGB16
X4-61	SIDE_D1	DRGB17
X4-63	SIDE_D13	DRGB24
X4-67	SIDE_D2	DRGB25
X4-69	SIDE_D12	DRGB26
X4-71	SIDE_D3	DRGB27
X4-73	SIDE_D11	DRGB28
X4-75	SIDE_D4	DRGB29
X4-77	SIDE_D10	DRGB30
X4-79	SIDE_D5	DRGB31
X4-83	SIDE_D9	BIDD-
X4-85	SIDE_D6	BIDD+
X4-87	SIDE_D8	BIDC-

14 Support Services

In order to access our most recent documentation, please visit the downloads section of the Logic web site at http://www.logicpd.com/auth/ .

If you have questions or need additional help with designing ETX baseboards for Geode LX SOM-ETX modules in custom applications, please contact Logic Product Development for more information. (http://www.logicpd.com/support/)

Please keep in mind that Logic has additional support services and support packages available for purchase. In addition, Logic provides a free Technical Discussion Group and FAQs for our products. (http://www.logicpd.com/support/)

15 SOM-ETX Mechanical Drawings

15.1 Hirose Connector Footprint

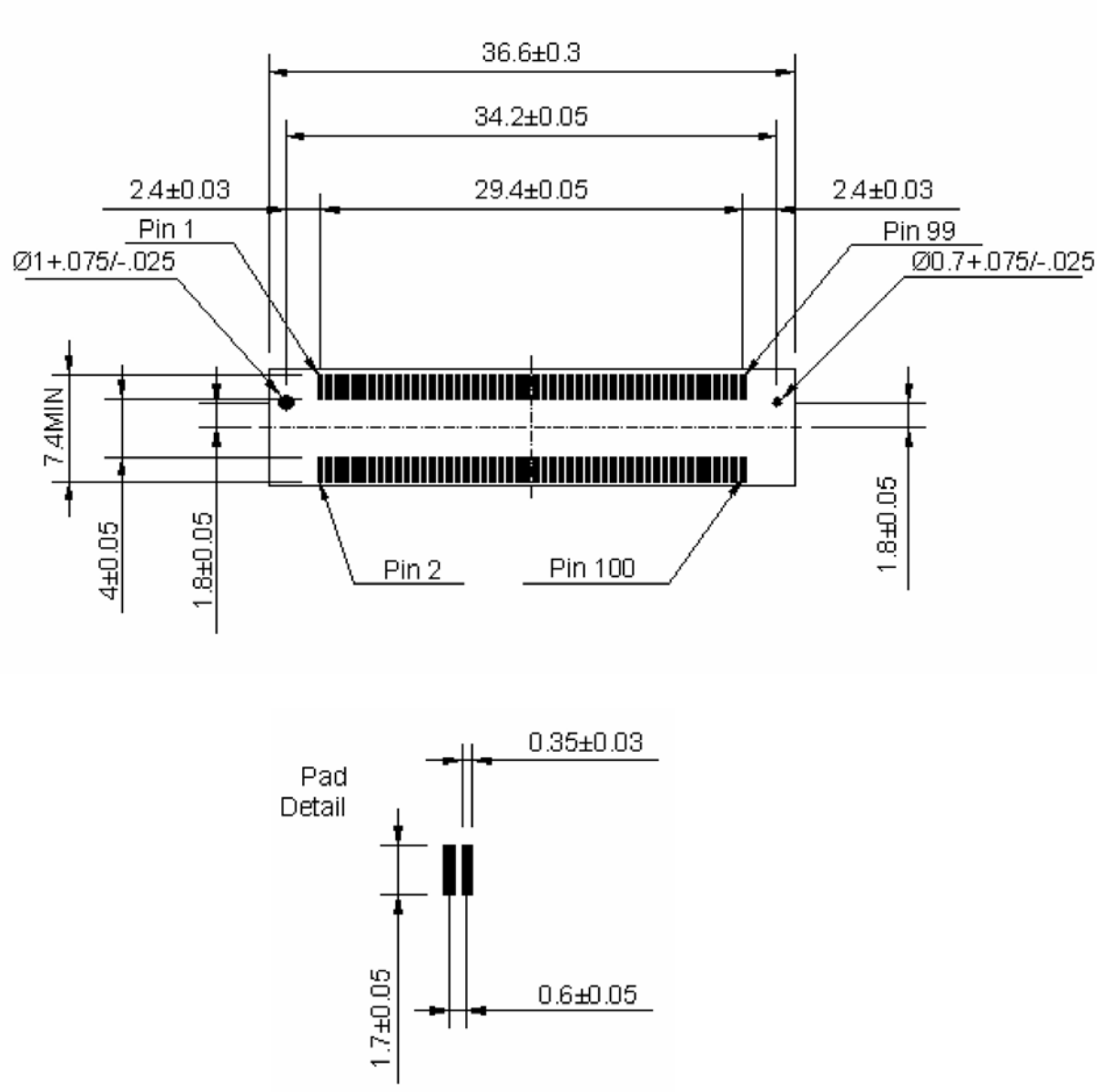

Figure 15.1: Hirose Connector Footprint

15.2 Geode LX SOM-ETX Footprint

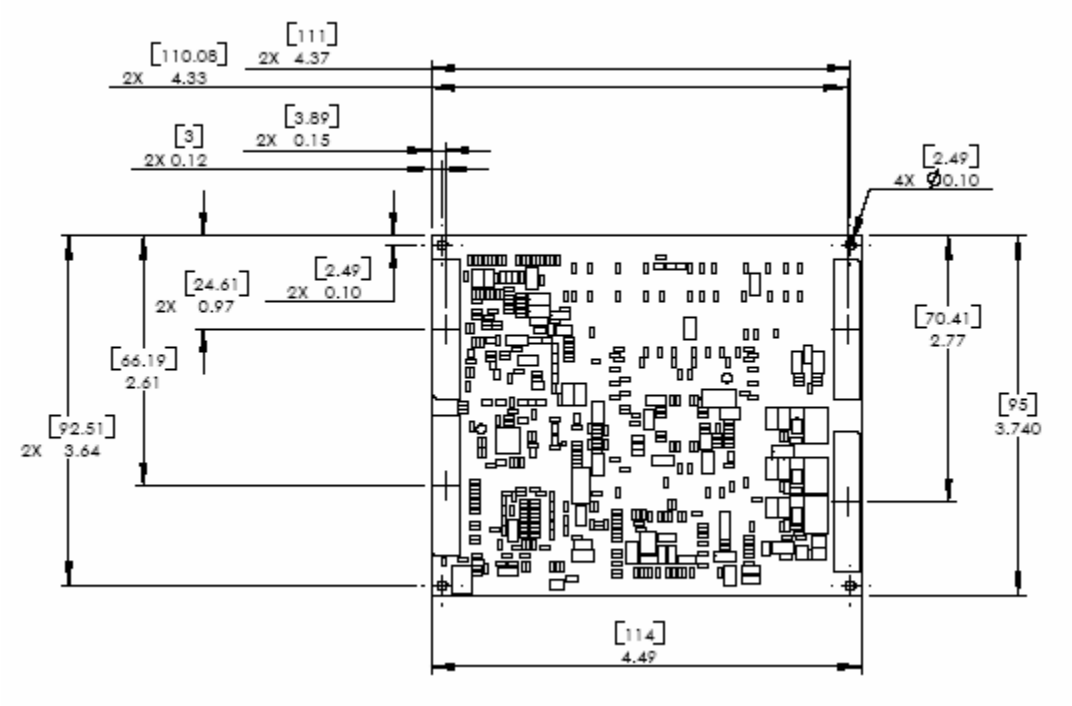

Figure 15.2: LX SOM-ETX Footprint

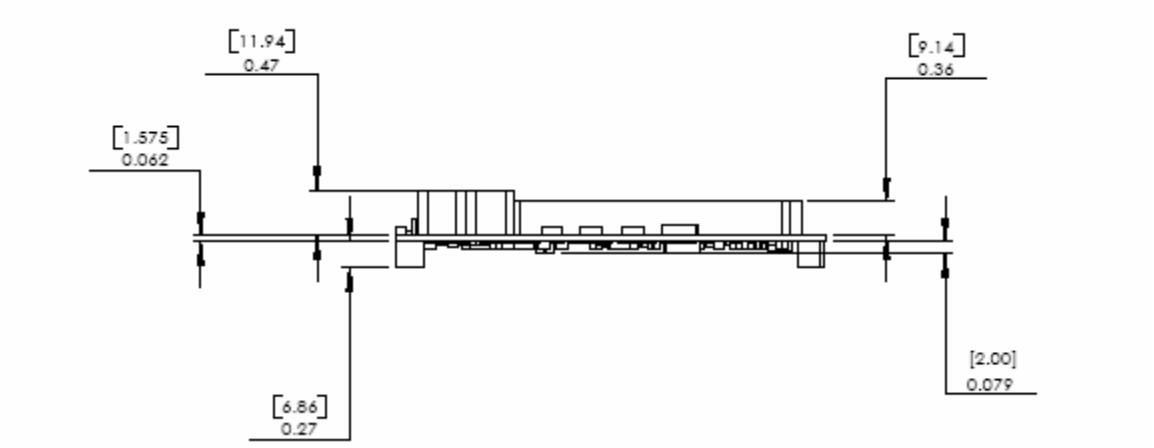

Figure 15.3: LX SOM-ETX Side View

15.3 Mating ETX Footprint

This layout drawing for the mating baseboard is from the standard ETX Specification version 3.

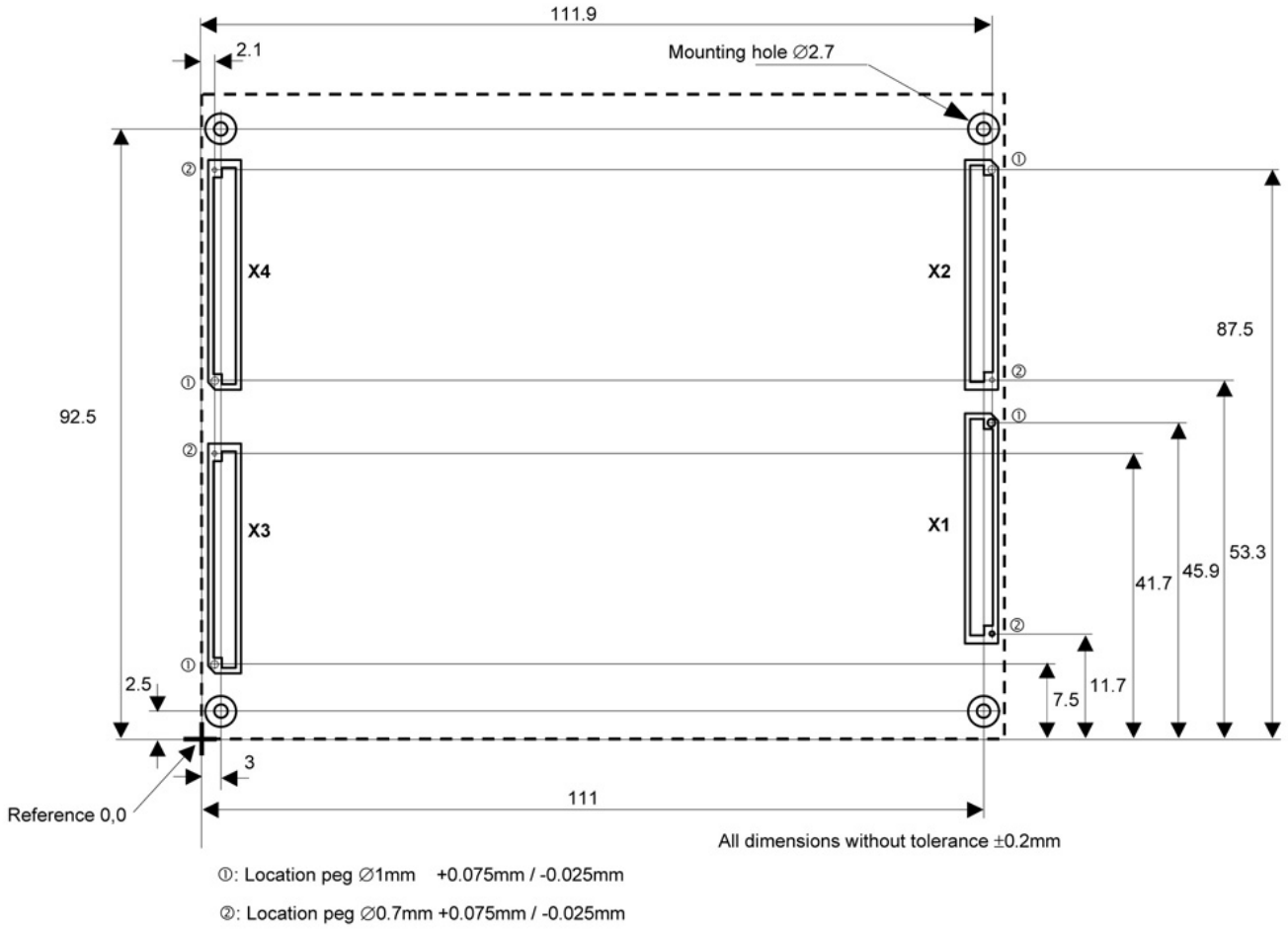

Figure 15.4: Mating ETX Footprint