OMAP3430
SOM-LV

SOM-LV

LOGIC

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REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	Schematic PN & REV	APPROVAL	DATE
1	Nathan Kro, Kurt Larson	Internal Release	1007969 Rev 6	NJK	02/22/08
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Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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1 Introduction

1.1 Product Overview

The OMAP3430 System on Module (SOM) is a compact, product-ready hardware and software solution that fast forwards embedded designs.

Based on Texas Instruments' OMAP3430 processor and designed in the SOM-LV Type III form factor, the OMAP3430 module offers essential features for handheld and embedded networking applications.

The OMAP3430 processor requires complex design and manufacturing as a result of the tight 0.4 mm pitch BGAs and Package On Package (POP) memory. Because these advanced technologies are located on the SOM, the developer is protected from the high risk and high cost of designing around those complexities. The SOM uses a standard form factor which allows developers to reuse existing baseboard designs when upgrading to new OMAP processors. This frees the developer from worries about part obsolescence while also extending roadmap possibilities for their end-product.

By starting with the corresponding Zoom™ Development Kit, engineers can write application software on the same hardware that will be used in the final product.

The OMAP3430 SOM-LV is ideal for applications in the medical, point-of-sale, industrial, and security markets. From patient monitoring and medical imaging, to card payment terminals and bar code readers, to CCTV cameras and intruder alarms, the OMAP3430 SOM-LV allows for powerful versatility and long-life products.

1.2 Acronyms

ADC	Analog to Digital Converter
BSP	Board Support Package
BTB	Board-to-Board
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access
ESD	Electrostatic Discharge
FIFO	First In First Out
GPIO	General Purpose Input Output
GPMC	General Purpose Memory Controller
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Circuit Sound
IC	Integrated Circuit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LDO	Low Dropout (Regulator)
LoLo	LogicLoader™
McBSP	Multi-channel Buffered Serial Port
OTG	On-the-Go (USB)
PCB	Printed Circuit Board
PCMCIA	Personal Computer Memory Card Internation Association (PC Cards)
PHY	Physical Layer
PLL	Phase Lock Loop
POP	Package On Package
PWM	Pulse Width Modulation

RTC	Real Time Clock
SDIO	Secure Digitial Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
STN	Super-Twisted Nematic (LCD)
TFT	Thin Film Transistor (LCD)
TI	Texas Instruments
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit

1.3 Scope of Document

This Hardware Specification is unique to the design and use of the OMAP3430 SOM-LV as designed by Logic and does not intend to include information outside of that scope. Detailed information about the Texas Instruments (TI) OMAP3430 processors or any other device component on the SOM can be found in their respective manuals and specification documents. Individual documents mentioned within this Hardware Specification include:

- *LogicLoader User's Manual* (available from Logic at http://www.logicpd.com/auth/)
- *OMAP3430 SOM-LV Schematics* (available from Logic at http://www.logicpd.com/auth/)
- *OMAP3430 Reference Manual* (available from TI's website)
- *USB 2.0 Specification* (available from USB.org at http://www.usb.org/developers/docs/)

1.4 SOM-LV Interface

Logic's common SOM-LV interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common SOM-LV footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

In fact, encapsulating a significant amount of your design onto the SOM-LV reduces any long-term risk of obsolescence. If a component on the SOM-LV design becomes obsolete, Logic will simply design for an alternative part that is transparent to your product. Furthermore, Logic tests all SOMs prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

1.5 OMAP3430 SOM-LV Block Diagram

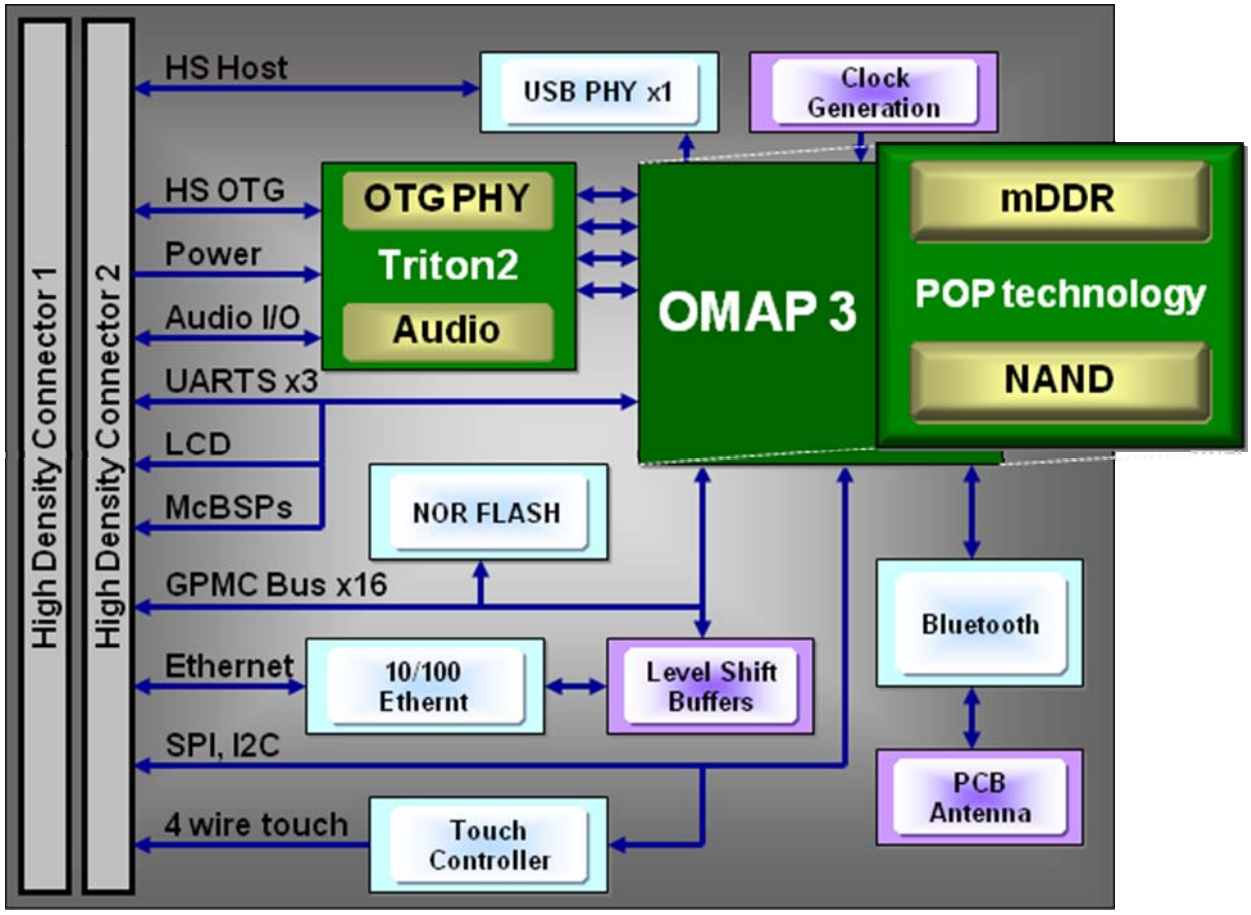

Figure 1.1: OMAP3430 SOM-LV Block Diagram

1.6 Electrical, Mechanical, and Environmental Specifications

1.6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC 3.3 V Supply Voltage	3.3V	0.0 to 3.6	V
DC Main Battery Input Voltage	MAIN_BATTERY	0.0 to 4.5	V
RTC Backup Battery Voltage	BACKUP_BATT	0.0 to 3.3	V

NOTE: These stress ratings are only for transient conditions. Operation at, or beyond, absolute maximum rating conditions may affect reliability and cause permanent damage to the SOM-LV and its components.

1.6.1.1 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC Main Battery Input Voltage	2.7	3.3	4.5	V	
DC Main Battery Active Current (4)	—	0.208	—	mA	4
DC Main Battery Active Current (5)	—	0.174	—	mA	5

Parameter	Min	Typical	Max	Unit	Notes
DC Main Battery Suspend Current	—	—	—	mA	
DC Main Battery Standby Current	—	—	—	mA	
DC 3.3 V Voltage	3.0	3.3	3.6	V	
DC 3.3 V Active Current (4)	—	0.16	—	mA	4
DC 3.3 V Active Current (5)	—	0.072	—	mA	5
DC 3.3 V Suspend Current	—	—	—	mA	
DC 3.3 V Standby Current	—	—	—	mA	
DC RTC Backup Battery Voltage	1.8	3.2	3.3	V	
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40		85	°C	
Storage Temperature	-40	25	85	°C	
Dimensions	—	31 x 76.2 x 7.4	—	mm	
Weight	—	14	—	Grams	2
Connector Insertion/Removal	—	50	—	Cycles	
Input Signal High Voltage	0.65 x VREF	—	VREF	V	3
Input Signal Low Voltage	-0.3	—	0.35 x VREF	V	3
Output Signal High Voltage	VREF - 0.2	—	VREF	V	3
Output Signal Low Voltage	GND	—	0.2	V	3

Notes:

1. General note: CPU power rails are sequenced on the module.
2. May vary depending on SOM-LV configuration.
3. VREF represents the peripheral I/O supply reference for the specific CPU voltage rail.
4. Full Run [Active], while(1) loop in LogicLoader. No peripherals attached.
5. Full Run [Active], while(1) loop in LogicLoader with Ethernet in D2 power state (off).

2 Electrical Specification

2.1 Processor

2.1.1 OMAP3430 Processor

The OMAP3430 SOM-LV uses TI's high-performance OMAP3430 processor. This device features the Superscalar ARM® Cortex™-A8 RISC core and provides many integrated on-chip peripherals, including:

- Superscalar ARM® Cortex™-A8 RISC core
  - Vectored floating point unit
  - 16 Kbytes instruction L1 cache
  - 16 Kbytes data L1 cache
  - 256 Kbyte L2 cache
  - 64 Kbyte RAM
  - 96 Kbyte ROM
- Integrated LCD Controller
  - Up to 1024 x 768 x 24 bit color
- Three UARTs
- I2S codec interface
- One high-speed USB 2.0 On-the-Go (OTG) and one USB 2.0 host interfaces
- Many general purpose I/O (GPIO) signals
- Programmable timers
- Real time clock (RTC)
- Low power modes

See TI's *OMAP3430 Reference Manual* and *Data Sheet* for additional information.
http://www.ti.com/omap

IMPORTANT NOTE: Please visit http://www.ti.com/omap for errata on the OMAP3430.

2.1.2 OMAP3430 Processor Block Diagram

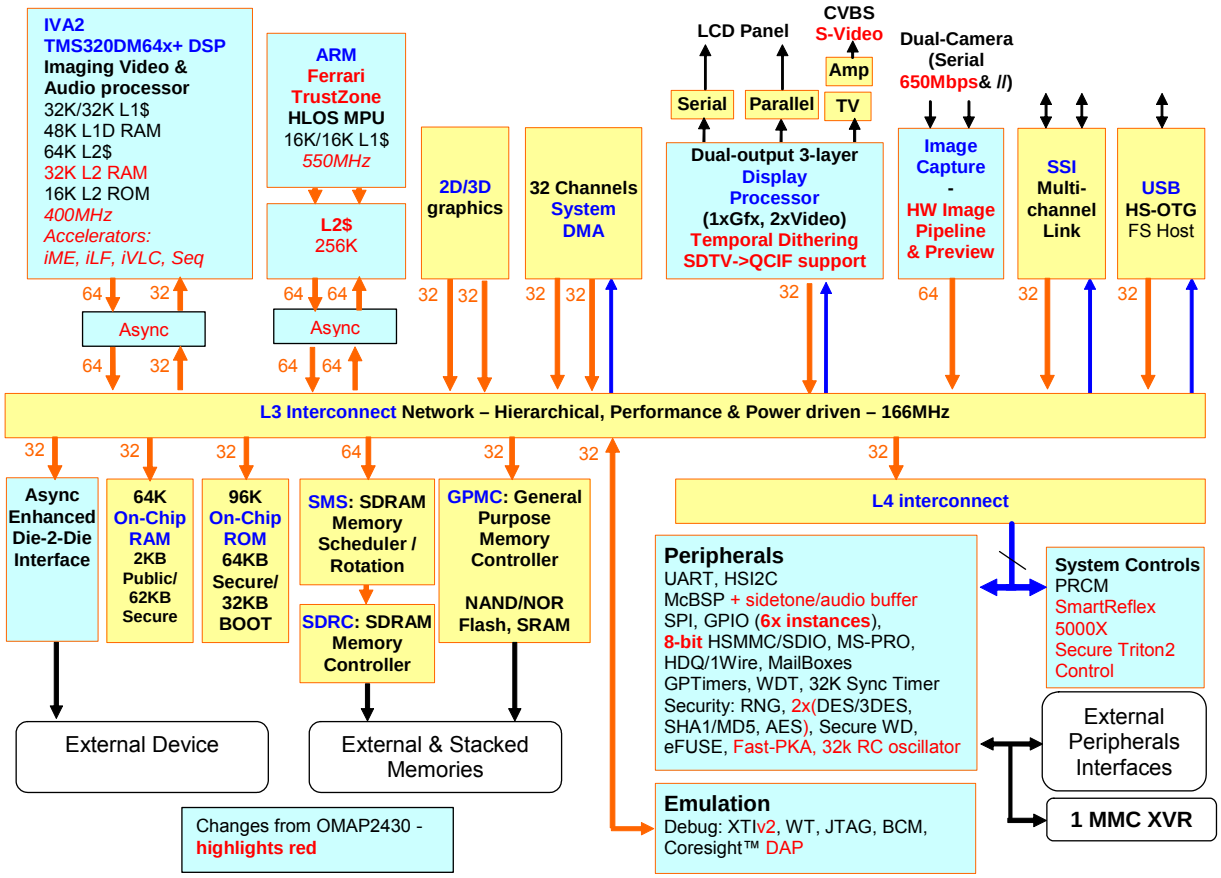

Figure 2.1: OMAP3430 Processor Block Diagram

2.2 Clocks

The OMAP3430 requires an oscillator and crystal to enable proper internal timing. A 26.000 MHz oscillator is used to generate many of the processor's internal clocks via a series of Phase Lock Loops (PLLs) and signal dividers. To generate the core CPU clock, the 26.000 MHz signal is run through a Digital PLL controlled by the PRCM registers. Divisors are used to divide down the internal bus frequency to set the LCD, memory controller, camera interface, etc.

IMPORTANT NOTE: Please see TI's OMAP3430 Technical Reference Manual for additional information about processor clocking.

The second required crystal runs at 32.768 kHz and is connected directly to the Triton2 (TWL4030). The 32.768 kHz clock is used for PMIC and CPU start up and as a reference clock for the Real Time Clock (RTC) Module.

The CPU's microcontroller core clock speed is initialized by software on the SOM-LV. The SDRAM bus speed is set at 166 MHz in LogicLoader. Other clock speeds, such as core speed and specific serial baud rates, can be supported and modified in software for specific user applications.

The SOM-LV provides an external bus clock, uP_BUS_CLK. This clock is driven by the GPMC_CLK pin.

OMAP3430 Microcontroller Signal Name	SOM-LV Net Name	Default Software Value in LogicLoader
CORE	N/A	Up to 550 MHz
SDRC_CLK	SDRC_CLK	166 MHz
GPMC_CLK	uP_BUS_CLK	Not configured

2.3 Memory

2.3.1 Package On Package Memory (Mobile DDR and NAND)

The OMAP3430 processor uses Package On Package (POP) technology to stack BGA memory devices on top of the CPU BGA. The OMAP3430 uses a 32-bit memory bus to interface to mobile DDR SDRAM and a 16-bit memory bus to interface to NAND. The POP devices can be ordered in two density options at time of publication:

- 128 MB Mobile DDR and 256 MB NAND
- 256 MB Mobile DDR and 512 MB NAND

Logic's default memory configuration on the SOM-LV included in the Zoom Development Kit is specified as 128 MB Mobile DDR and 256 MB NAND.

2.3.2 NOR Flash

The SOM-LV uses the 16-bit GPMC memory bus to interface to a single NOR flash memory chip. The onboard SOM-LV NOR flash memory can be configured as 0, 8, 16, 32, or 64 MB to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 8 MB on the SOM-LV included in the standard Zoom Development Kit. Because flash is one of the most expensive components on the SOM-LV, it is important to contact Logic when determining the necessary flash size for final product configuration. NAND flash is a lower cost alternative that should be considered for final product configuration.

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, SD memory, CompactFlash®, or NAND flash. See the Zoom Development Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.3 PC Card Interface

The OMAP3430 CPU does not directly support PCMCIA or CompactFlash slots. The SOM-LV uses internal logic to provide the necessary signals for the ComapctFlash interface, creating support for a single external memory-mode only Compact Flash card. The Zoom Development Kit reference design includes a hot-swappable CompactFlash connector. Additional CompactFlash slots can be added using the GPMC bus. Contact platformsupport@logicpd.com for more information on implementing additional slots.

2.4 10/100 Ethernet PHY

The SOM-LV uses an SMSC LAN9211 Ethernet MAC+PHY to provide an easy-to-use networking interface. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides an example circuit schematic in the Zoom Development Kit schematics for reference. Please note the TX+/- and RX+/- pairs must be routed as differential pairs on the baseboard PCB.

2.5 Bluetooth

The SOM-LV uses a TI BRF6300 BlueLink to provide a Bluetooth interface. The BRF6300 is connected to the OMAP3430 through McSPI1 and PCM.

2.6 Audio Codec

The OMAP3430 processor has multiple Multi-channel Buffered Serial Port (McBSP) interfaces that support PCM and I2S formats. Both PCM and I2S serial paths drive the built-in TWL4030 audio codec. From the TWL4030, the outputs are CODEC_OUTL and CODEC_OUTR; these signals are available from the expansion connectors.

The codec in the TWL4030 performs up to full-duplex codec functions and supports variable sample rates from 8–96k samples per second. See the “Audio” chapter in the *TWL4030 Technical Reference Manual* for more information.

NOTE: The SOM-LV also offers alternate serial interfaces for other codec devices. If you are looking for a different codec option, Logic has previously interfaced different high-performance audio codecs into other SOMs. Contact Logic for assistance in selecting an appropriate audio codec for your application.

2.7 Display Interface

The OMAP3430 has a built-in LCD controller supporting STN, color STN, and TFT panels at a resolution of up to XGA 1024 x 768 x 24-bit color. See the *OMAP3430 Technical Reference Manual* for further information on the integrated LCD controller. The signals from the OMAP3430 LCD controller are organized by bit and color and can be interfaced through the expansion connectors. Logic has written drivers for panels of different types and sizes. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

2.8 Serial Interfaces

The SOM-LV comes with the following serial channels: UARTA, UARTB, UARTC, SPI, and two I2C ports. If additional serial channels are required, please contact Logic for reference designs. Please see the *OMAP3430 Technical Reference Manual* for further information regarding serial communications.

2.8.1 UARTA

UARTA has been configured as the main SOM-LV serial port based on the processor UART1. It is an asynchronous 16C750-compatible UART. This UART provides a high-speed serial interface that uses 64 byte First In / First Out (FIFO) and is capable of sending and receiving serial data simultaneously. The signals from the SOM-LV are 1.8V Transistor-Transistor Logic (TTL) level signals, not RS232 level signals. The end-product design must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the Zoom OMAP3430 Development Kit. When choosing an RS232 transceiver, the designer should keep in mind cost, availability, ESD protection, and data rates.

The UARTA baud rate is set to a default 115.2 Kbits/sec, though it supports most common serial baud rates.

2.8.2 UARTB

Serial Port UARTB (processor UART3) is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the SOM-LV are TTL level signals, not RS232 level signals. The UARTB baud rate can also be set to most common serial baud rates.

2.8.3 UARTC

Serial port UARTC (processor UART2) is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the SOM-LV are TTL level signals, not RS232 level signals. The UARTC baud rate can also be set to most common serial baud rates.

2.8.4 McSPI

The SOM-LV provides an external SPI port with multiple chip selects.

2.8.5 I2C

The SOM-LV supports two dedicated external I2C ports. The clock and data signals for both ports have 4.7K pull-up resistors to their respective power rails. Please see TI's *OMAP3430 Technical Reference Manual* for further information.

2.9 USB Interface

The SOM-LV supports one USB 2.0 high-speed host port and one USB 2.0 OTG port which can function as a host or device/client. Both ports can operate at up to 480 Mbit/sec. The processor has the USB controller internal to the OMAP for both the host and OTG port. The SOM-LV has one external PHY and one PHY built into the TWL4030 to support the two interfaces. The external PHY is an NXP ISP1702. For more information on using both the USB host and OTG interfaces, please see the *OMAP3430 Technical Reference Manual*.

IMPORTANT NOTE: In order for USB to be correctly implemented on the SOM-LV, additional impedance matching circuitry may be required on the USBx_D+ and USBx_D- signals before they can be used. USB 2.0 requirements specify the signals must be routed as differential pairs with a 90 ohm differential impedance. Refer to the *USB 2.0 Specification* for detailed information.

2.10 ADC/Touch Interface

The SOM-LV uses TI's TSC2004 touch screen controller (TSC). The controller includes a 12-bit analog-to-digital converter (ADC). This TSC is used to support standard 4-wire resistive touch panels. The TSC has 5 A/D signals that are available externally off the connectors. The device is connected to the CPU by the OMAP I2C3 interface. Please see the *TSC2004 Datasheet* for more information.

2.11 General Purpose I/O

Logic designed the SOM-LV to be flexible and provide multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the SOM-LV that interface to the OMAP3430 and TWL4030. See the "Pin Descriptions & Functions" Section of this document for more information. If certain peripherals are not desired, such as the LCD controller, chip selects, IRQs, or UARTs, then more GPIO pins become available.

2.12 Onboard Logic Interfaces

The onboard logic interfaces are used to create additional functionality on the SOM-LV with the support of a few discrete logic components.

2.13 Expansion/Feature Options

The SOM-LV was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the expansion connectors. It is possible for a user to expand the SOM-LV's functionality even further by adding host bus or ISA bus devices. Some features that are implemented on the OMAP3430, but are not discussed herein, include: RTC, pulse width modulation (PWM), Secure Digital, SIM card, MMC cards, SDIO cards, graphics accelerator, DSP codecs, Image Processing Unit, 1wire interface, and the debug module. See the *OMAP3430 Technical Reference Manual* and the *SOM-LV Schematics* for more details. Logic has experience implementing additional options, including other audio codecs, Ethernet ICs, co-processors, and components on SOMs. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The OMAP3430 SOM-LV was designed to meet multiple applications for users with specific design and budget requirements. As a result, this SOM-LV supports a variety of embedded operating systems and supports the following hardware configurations:

- Flexible memory footprint: 128 or 256 MB mobile DDR SDRAM
- Flexible NOR flash footprint: 0, 8, 16, or 32 MB NOR flash
- Flexible NAND flash footprint: 0, 256, or 512 MB
- Optional SMSC LAN9211 10/100 Ethernet PHY
- Optional TI BRF6300 Bluetooth

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

The SOM-LV has a reset input (MSTR_nRST) and a reset output (RESET_nOUT/SYS_nRESWARM). External devices use MSTR_nRST to assert reset to the product. The SOM-LV uses RESET_nOUT to indicate to other devices that the SOM-LV is in reset.

3.2.1 Master Reset (MSTR_nRST)—Reset Input

Logic suggests that custom designs implementing the OMAP3430 SOM-LV use the MSTR_nRST signal as the “pin-hole” reset used in commercial embedded systems. The MSTR_nRST triggers a power-on-reset event to the OMAP3430 processor and resets the entire CPU.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition. (Powering up in a low or bad power condition will cause data corruption and, possibly, temporary system lockup). See the “Power Management” section of this document for further details. Either one of the following two conditions will cause a system-wide reset: power on the MSTR_nRST signal or a low pulse on the MSTR_nRST signal.

Low Pulse on MSTR_nRST Signal:

A low pulse on the MSTR_nRST signal, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that for any external assertion source that triggers the MSTR_nRST signal, analog or digital, de-bouncing should be used to generate a clean, one-shot reset signal.

3.2.2 SOM-LV Reset (RESET_nOUT/SYS_nRESWARM)—Reset output

All hardware peripherals should connect their hardware-reset pin to the RESET_nOUT (SYS_nRESWARM) signal on the expansion connector. Internally, all SOM-LV peripheral hardware reset pins are connected to the RESET_nOUT net.

If the output of the onboard voltage-monitoring circuit is asserted (active low), the user can expect to lose information stored in RAM. The data loss occurs because the CPU is reset to its reset defaults.

3.3 Interrupts

The OMAP3430 incorporates the ARM Cortex-A8 interrupt controller which provides many inter-system interrupt sources and destinations. Most external GPIO signals can also be configured as interrupt inputs by configuring their pin control registers. Logic BSPs setup and process all onboard system and external SOM-LV interrupt sources. Refer to TI's *OMAP3430 Reference Manual* for further information on using interrupts.

3.4 JTAG Debugger Interface

The JTAG connection on the OMAP3430 allows recovery of corrupted flash memory, real-time application debug, and DSP development. There are several third-party JTAG debuggers available for TI microcontrollers. The following signals make up the JTAG interface to the OMAP3430 processor: TDI, TMS, TCK, TDO, nTRST, RTCK, EMU0, and EMU1. These signals should interface directly to a 20-pin 0.1" through-hole connector, as shown on the Zoom Development Kit baseboard reference schematics.

IMPORTANT NOTE: When laying out the 20-pin connector, realize that it may not be numbered as a standard 20-pin 0.1" insulation displacement connector (IDC) through-hole connector. See the Zoom Development Kit reference design for further details. Each JTAG tool vendor may define the 20-pin IDC connector pin-out differently.

3.5 ETM Adapter Interface

The Embedded Trace Macrocell (ETM) interface signals are available through connector J5 on the SOM-LV. Logic sells an adapter board that converts the available signals on J5 to the standard Mictor connector interface used by most common third-party ETM tool providers. The connector supports ETM_D[15:0], ETM_CLK, ETM_CTL, and the JTAG signals listed in Section 3.4.

3.6 Power Management

3.6.1 System Power Supplies

In order to ensure a flexible design, the SOM-LV has the following power areas: MAIN_BATTERY, 5V, 3.3V, BACKUP_BATT. All power areas are inputs to the SOM-LV. The module also provides reference voltages to specific peripheral areas. Reference voltages are named VREF_xxxx on the expansion connectors, are outputs from the SOM-LV, and should be used as reference voltage inputs to level shifting devices on baseboard designs.

3.6.1.1 MAIN_BATTERY

The MAIN_BATTERY input is the main source of power for the SOM-LV. This input expects a voltage within typical single lithium-ion battery limits which generally operate from 2.8 V to 4.2 V. If a lithium-ion battery is not used as the main power source, it is recommended to supply a fixed 3.3 V supply. The TWL4030 power management controller takes the MAIN_BATTERY rail input and creates all onboard voltages. If the design is required to maintain RAM contents in a critical power situation (e.g., low battery, loss of power), the MAIN_BATTERY supply should be maintained above the minimum level at all costs (see Section 2, "Electrical Specification"). Logic suggests using the Standby mode to prepare the system for a critical power condition. In this

way, the SDRAM is placed into self-refresh and the processor is placed into the Standby state. (Please note the description of Standby mode in Section 3.6.3.3 below.) The MAIN_BATTERY supply must stay within the acceptable levels specified in Section 2, “Electrical Specification,” unless experiencing power down or critical power conditions.

3.6.1.2 5V

The 5V input is not required for product operation. The 5V input is only used when the charge path components are populated on the SOM-LV. These optional charge path circuits allow in-system charging of a single cell lithium-ion battery source when a 5 V power is applied to the 5 V supply. Some designs will require a separate battery charging circuit on the baseboard to charge the main battery source. Charge current is limited to 1 Amp.

3.6.1.3 3.3V

The 3.3V rail is used to power a few legacy interfaces on the SOM-LV which require 3.3 V. The baseboard should provide 3.3 V to the SOM-LV when 10/100 Ethernet is required on the final product. Typically this can be implemented as a low dropout (LDO) or switching regulator connected to the MAIN_BATTERY power source on the baseboard. The 3.3V supply must stay within the acceptable levels specified in Section 2, “Electrical Specification” unless experiencing power down or critical power conditions. Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering off this supply.

3.6.1.4 BACKUP_BATT

The BACKUP_BATT power rail is used to power the onboard TWL4030, power management state machine, and RTC circuit when MAIN_BATTERY is not present. Always power this rail to maintain the clock and power state of the product. A lithium-ion coin cell typically supplies power to this rail. The TWL4030 overrides this input when MAIN_BATTERY is applied.

3.6.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The SOM-LV was designed with these aspects in mind while also providing maximum flexibility in software and system integration.

On the OMAP3430 there are many different software configurations that drastically affect power consumption: microcontroller core clock frequency, bus clock frequency, peripheral clocks, bus modes, power management states; peripheral power states and modes; product user scenarios; interrupt handling; and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be modified later in the operating system and application software. Information for these items can be found in the appropriate documents such as the *LogicLoader User’s Manual* or the specific BSP manual.

3.6.3 Microcontroller

The OMAP3430 processor’s power management scheme was designed for the cellular handset market, so naturally the static and dynamic power consumption has very flexible controls allowing designers to tweak the processor to minimize end-product power consumption. Logic software BSPs take advantage of Dynamic Power Switching and SmartReflex Adaptive Voltage Control to maximize power savings.

3.6.3.1 Run State

Run is the normal operating state for the SOM-LV in which oscillator outputs and all clocks are hardware enabled. The OMAP3430 can enter Run mode from any state. A Standby-to-Run transition occurs on any valid wakeup event, such as the assertion or any enabled interrupt signal. All required power supplies are active in this state. Please see TI's *OMAP3430 Technical Reference Manual* for further information.

3.6.3.2 Suspend State

Suspend is the hardware power-down state for the SOM-LV, allowing for lower power consumption. The Suspend state is designed to reduce power consumption while the OMAP3430 is waiting for an event, such as a keyboard input. In Logic BSPs, the Suspend state is entered by asserting the nSUSPEND signal or through software commands. All power supplies remain active and system context is retained. An internal or external wakeup event can cause the processor to transition back to Run mode. Please see TI's *OMAP3430 Reference Manual* for further information.

3.6.3.3 Standby State

Standby is the lowest power state for the SOM-LV. This state is entered in Logic BSPs by asserting the nSTANDBY signal or through software commands. The OMAP3430 processor is put into the lowest power state and all clocks are stopped. The MAIN_BATTERY power rail should be maintained if the low-power DDR SDRAM contents wish to be retained. Internal or external wakeup events can cause a return to the Run state.

3.7 ESD Considerations

The SOM-LV was designed to interface to a customer's peripheral board, while remaining low cost and adaptable to many different applications. The SOM-LV does not provide any onboard ESD protection circuitry—this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

On the OMAP3430 microcontroller, all address mapping for the GPMC chip select signals is listed below.

Mapped “Chip Select” signals for the OMAP are available as outputs from the microcontroller and are assigned as follows:

Chip Select	Offset	Device/Feature	Notes
nCS0		POP NAND / boot NOR	Boot chip select for POP NAND device or external NOR when POP does not include NAND.
nCS1		10/100 Ethernet	SMSC LAN9211
nCS2		ON-/OFF-board NOR boot	Intel P30 series
nCS3		External Memory Mode CompactFlash	
nCS4		External nCS_A	Available for use by an off-board external device
nCS5		External nCS_B	Available for use by an off-board external device

Please consult the *LogicLoader User’s Manual* and the *LogicLoader User’s Manual Addendum* for the OMAP3430 for complete memory map information.

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of LogicLoader (bootloader). Many of the signals defined in the tables below can be configured as input or outputs—all GPIOs on the OMAP3430 processor can be configured as either inputs or outputs—and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull-ups/pull-downs).

5.1 J1 Connector 240-Pin Descriptions

J1 Pin#	Signal Name	I/O	Voltage	Description
1	RFU	I/O	NA	Reserved for future use. Do not connect.
2	RFU	I/O	NA	Reserved for future use. Do not connect.
3	RFU	I/O	NA	Reserved for future use. Do not connect.
4	RFU	I/O	NA	Reserved for future use. Do not connect.
5	RFU	I/O	NA	Reserved for future use. Do not connect.
6	RFU	I/O	NA	Reserved for future use. Do not connect.
7	RFU	I/O	NA	Reserved for future use. Do not connect.
8	RFU	I/O	NA	Reserved for future use. Do not connect.
9	RFU	I/O	NA	Reserved for future use. Do not connect.
10	RFU	I/O	NA	Reserved for future use. Do not connect.
11	DGND	I	GND	Ground. Connect to digital ground.
12	DGND	I	GND	Ground. Connect to digital ground.
13	uP_nWAKEUP	I	MAIN_BATTERY	Active low. Software can use this signal as an interrupt to transition to RUN state from lower power states. Software is required for proper operation. This signal has a 4.75K pull-up.
14	ETHER_TX+	O	3.3V	This output pair drives 10/100 Mb/s data to the transmit lines. Route as differential pair with ETHER_TX-. Requires external magnetics. See example LV-Baseboard design for reference components.
15	nSUSPEND	I	1.8V	Software can use this signal to enter low power states from RUN mode. Software is required for correct operation.
16	ETHER_TX-	O	3.3V	This output pair drives 10/100 Mb/s data to the transmit lines. Route as differential pair with ETHER_TX+. Requires external magnetics. See example LV-Baseboard design for reference components.
17	nSTANDBY	I	1.8V	Software can use this signal to enter low power states from RUN mode. Software is required for correct operation.
18	ETHER_RX+	I	3.3V	This input pair receives 10/100 Mb/s data from the receive lines. Route as differential pair with ETHER_RX-. Requires external magnetics. See example LV-Baseboard design for reference components.
19	USB1_ID	I/O	5.0V	Tie to pin four of a USB 2.0 OTG compliant connector. This signal negotiates host/device operation with an external USB product. See example LV-Baseboard design for reference components.

J1 Pin#	Signal Name	I/O	Voltage	Description
20	ETHER_RX-	I	3.3V	This input pair receives 10/100 Mb/s data from the receive lines. Route as differential pair with ETHER_RX+. Requires external magnetics. See example LV-Baseboard design for reference components.
21	USB1_VBUS	I/O	5.0V	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected or can provide power to USB Device peripherals. See example LV-Baseboard design for reference components.
22	ACT_nLNK_LED/LAN_LED2	O	3.3V	Active low. Asserts when there is valid Ethernet connection. Deasserts during Ethernet traffic indicating activity. See example LV-Baseboard design for reference components.
23	USB1_nOC	I	1.8V	Active low. USB OTG over current flag. Indicates to PHY an over current condition exists on the USB OTG port.
24	SPD_LED_n100M_10M/LAN_LED1	O	3.3V	Active low. Asserts to indicate operation speed, either 10Mbs (high) or 100Mbs (low) connection. See example LV-Baseboard design for reference components.
25	USB1_PWR_nEN	O	1.8V	Active low. USB OTG power enable. Enables power to the external USB power switch.
26	VREF_ETHERNET (3.3V_A)	O	3.3V	Output from the SOM-LV that drives the impedance network and magnetics. Specific to Ethernet PHY requirements. See example LV-Baseboard design for reference components.
27	USB1_D+	I/O	Variable	USB OTG port 1 I/O data plus signal. Route as differential pair with USB1_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
28	RFU	I/O	NA	Reserved for future use. Do not connect.
29	USB1_D-	I/O	Variable	USB OTG port 1 I/O data minus signal. Route as differential pair with USB1_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
30	RFU	I/O	NA	Reserved for future use. Do not connect.
31	DGND	I	GND	Ground. Connect to digital ground.
32	DGND	I	GND	Ground. Connect to digital ground.
33	USB2_D+	I/O	Variable	USB Host port 2 I/O data plus signal. Route as differential pair with USB2_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
34	uP_GPIO_7	I/O	1.8V	TWL4030 GPIO available to user. Connected to TWL4030 GPIO.2.
35	USB2_D-	I/O	Variable	USB Host port 2 I/O data minus signal. Route as differential pair with USB2_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
36	uP_GPIO_6	I/O	1.8V	TWL4030 GPIO available to user. Connected to TWL4030 GPIO.15.
37	USB2_nOC	I	3.3V	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.
38	uP_GPIO_5	I/O	1.8V	TWL4030 GPIO available to user. Connected to TWL4030 GPIO.7.

J1 Pin#	Signal Name	I/O	Voltage	Description
39	USB2_PWR_nEN	O	5.0V	Active low. USB Host power enable. Enables power to the external USB power switch. See example LV-Baseboard design for reference components.
40	uP_D0	O	1.8V	Processor GPMC bus data bit 0.
41	RFU	I/O	NA	Reserved for future use. Do not connect.
42	uP_D1	O	1.8V	Processor GPMC bus data bit 1.
43	RFU	I/O	NA	Reserved for future use. Do not connect.
44	uP_D2	O	1.8V	Processor GPMC bus data bit 2.
45	RFU	I/O	NA	Reserved for future use. Do not connect.
46	uP_D3	O	1.8V	Processor GPMC bus data bit 3.
47	RFU	I/O	NA	Reserved for future use. Do not connect.
48	uP_D4	O	1.8V	Processor GPMC bus data bit 4.
49	3.3V_nEN (DGND)	O	1.8V	3.3V external enable pin. Active low, signals to the baseboard the 3.3V supply should be enabled.
50	uP_D5	O	1.8V	Processor GPMC bus data bit 5.
51	DGND	I	GND	Ground. Connect to digital ground.
52	DGND	I	GND	Ground. Connect to digital ground.
53	A0 (DGND)	O	1.8V	Processor GPMC bus address bit 0. (see note 1)
54	uP_D6	O	1.8V	Processor GPMC bus data bit 6.
55	A1 (uP_LA1)	O	1.8V	Latched Processor GPMC bus address bit 1. (see note 1)
56	uP_D7	O	1.8V	Processor GPMC bus data bit 7.
57	A2 (uP_LA2)	O	1.8V	Latched Processor GPMC bus address bit 2. (see note 1)
58	uP_D8	O	1.8V	Processor GPMC bus data bit 8.
59	A3 (uP_LA3)	O	1.8V	Latched Processor GPMC bus address bit 3. (see note 1)
60	uP_D9	O	1.8V	Processor GPMC bus data bit 9.
61	A4 (uP_LA4)	O	1.8V	Latched Processor GPMC bus address bit 4. (see note 1)
62	uP_D10	O	1.8V	Processor GPMC bus data bit 10.
63	A5 (uP_LA5)	O	1.8V	Latched Processor GPMC bus address bit 5. (see note 1)
64	uP_D11	O	1.8V	Processor GPMC bus data bit 11.
65	A6 (uP_LA6)	O	1.8V	Latched Processor GPMC bus address bit 6. (see note 1)
66	uP_D12	O	1.8V	Processor GPMC bus data bit 12.
67	A7 (uP_LA7)	O	1.8V	Latched Processor GPMC bus address bit 7. (see note 1)
68	uP_D13	O	1.8V	Processor GPMC bus data bit 13.
69	A8 (uP_LA8)	O	1.8V	Latched Processor GPMC bus address bit 8. (see note 1)
70	uP_D14	O	1.8V	Processor GPMC bus data bit 14.
71	DGND	I	GND	Ground. Connect to digital ground.
72	DGND	I	GND	Ground. Connect to digital ground.
73	A9 (uP_LA9)	O	1.8V	Latched Processor GPMC bus address bit 9. (see note 1)
74	uP_D15	O	1.8V	Processor GPMC bus data bit 15.
75	A10 (uP_LA10)	O	1.8V	Latched Processor GPMC bus address bit 10. (see note 1)
76	D16 (RFU)	I/O	NA	Reserved for future use. Do not connect.
77	A11 (uP_LA11)	O	1.8V	Latched Processor GPMC bus address bit 11. (see note 1)
78	D17 (RFU)	I/O	NA	Reserved for future use. Do not connect.
79	A12 (uP_LA12)	O	1.8V	Latched Processor GPMC bus address bit 12. (see note 1)

J1 Pin#	Signal Name	I/O	Voltage	Description
80	D18 (RFU)	I/O	NA	Reserved for future use. Do not connect.
81	A13 (uP_LA13)	O	1.8V	Latched Processor GPMC bus address bit 13. (see note 1)
82	D19 (RFU)	I/O	NA	Reserved for future use. Do not connect.
83	A14 (uP_LA14)	O	1.8V	Latched Processor GPMC bus address bit 14. (see note 1)
84	D20 (RFU)	I/O	NA	Reserved for future use. Do not connect.
85	A15 (uP_LA15)	O	1.8V	Latched Processor GPMC bus address bit 15. (see note 1)
86	D21 (RFU)	I/O	NA	Reserved for future use. Do not connect.
87	A16 (uP_LA16)	O	1.8V	Latched Processor GPMC bus address bit 16. (see note 1)
88	D22 (RFU)	I/O	NA	Reserved for future use. Do not connect.
89	A17 (uP_A1)	O	1.8V	Processor GPMC bus address bit 17. (see note 1)
90	D23 (RFU)	I/O	NA	Reserved for future use. Do not connect.
91	DGND	I	GND	Ground. Connect to digital ground.
92	DGND	I	GND	Ground. Connect to digital ground.
93	A18 (uP_A2)	O	1.8V	Processor GPMC bus address bit 18. (see note 1)
94	D24 (RFU)	I/O	NA	Reserved for future use. Do not connect.
95	A19 (uP_A3)	O	1.8V	Processor GPMC bus address bit 19. (see note 1)
96	D25 (RFU)	I/O	NA	Reserved for future use. Do not connect.
97	A20 (uP_A4)	O	1.8V	Processor GPMC bus address bit 20. (see note 1)
98	D26 (RFU)	I/O	NA	Reserved for future use. Do not connect.
99	A21 (uP_A5)	O	1.8V	Processor GPMC bus address bit 21. (see note 1)
100	D27 (RFU)	I/O	NA	Reserved for future use. Do not connect.
101	A22 (uP_A6)	O	1.8V	Processor GPMC bus address bit 22. (see note 1)
102	D28 (RFU)	I/O	NA	Reserved for future use. Do not connect.
103	A23 (uP_A7)	O	1.8V	Processor GPMC bus address bit 23. (see note 1)
104	D29 (RFU)	I/O	NA	Reserved for future use. Do not connect.
105	A24 (uP_A8)	O	1.8V	Processor GPMC bus address bit 24. (see note 1)
106	D30 (RFU)	I/O	NA	Reserved for future use. Do not connect.
107	A25 (uP_A9)	O	1.8V	Processor GPMC bus address bit 25. (see note 1)
108	D31 (RFU)	I/O	NA	Reserved for future use. Do not connect.
109	uP_nWAIT	I	1.8V	Active low. Processor bus GPMC_WAIT1 signal. Used to extend bus transactions beyond programmed wait states. The external device signals completion of the cycle by deasserting the uP_nWAIT signal. This signal has a 1K pull-up.
110	VREF_DATA_BUS (VIO_1V8)	O	1.8V	Voltage reference output created on SOM-LV for the data bus.
111	DGND	I	GND	Ground. Connect to digital ground.
112	DGND	I	GND	Ground. Connect to digital ground.
113	uP_nIRQD (CSI_D11)	I	1.8V	Active low. Software can use as a hardware interrupt.
114	RFU	I/O	NA	Reserved for future use. Do not connect.
115	uP_nIRQC	I	1.8V	Active low. Software can use as a hardware interrupt.
116	RFU	I/O	NA	Reserved for future use. Do not connect.

J1 Pin#	Signal Name	I/O	Voltage	Description
117	uP_nIRQB	I	1.8V	Active low. Software can use as a hardware interrupt.
118	RFU	I/O	NA	Reserved for future use. Do not connect.
119	uP_nIRQA	I	1.8V	Active low. Software can use as a hardware interrupt.
120	RFU	I/O	NA	Reserved for future use. Do not connect.
121	RFU	I/O	NA	Reserved for future use. Do not connect.
122	uP_UARTC_CTS	I	1.8V	Clear To Send signal for UART2.
123	BUFF_DIR_DATA	O	1.8V	When low, external buffers should drive data from external devices towards the SOM-LV. (SOM-LV is reading) When high, external buffers should drive data from the SOM-LV towards external devices. (SOM-LV is writing).
124	uP_UARTC_RTS	O	1.8V	Ready To Send signal for UART2.
125	uP_nOE	O	1.8V	Active low. Used to indicate processor is reading from external devices.
126	uP_UARTC_RX	I	1.8V	Serial Data Receive signal for UART2.
127	uP_nWE	O	1.8V	Low indicates processor is writing. High indicates processor is reading.
128	uP_UARTC_TX	O	1.8V	Serial Data Transmit signal for UART2.
129	DGND	I	GND	Ground. Connect to digital ground.
130	DGND	I	GND	Ground. Connect to digital ground.
131	uP_BUS_CLK	O	1.8V	Processor bus clock. Frequency varies based on software setup.
132	uP_UARTB_RX	I	1.8V	Serial Data Receive signal for UART3.
133	uP_DREQ0	I	1.8V	DMA Request signal for DMA4. Connected to SYS_nDMAREQ3 of the OMAP34300.
134	uP_UARTB_TX	O	1.8V	Serial Data Transmit signal for UART3.
135	uP_DREQ1	I	1.8V	DMA Request signal for DMA4. Connected to SYS_nDMAREQ1 of the OMAP34300.
136	uP_UARTB_CTS	I	1.8V	Clear To Send signal for UART3.
137	uP_nBE0	O	1.8V	Processor bus Byte Lane Enable 0 bits [7:0]
138	uP_UARTB_RTS	O	1.8V	Ready To Send signal for UART3.
139	uP_nBE1	O	1.8V	Processor WEIM bus Byte Lane Enable 1 bits [15:8]
140	uP_GPO_4	I/O	1.8V	TWL4030 GPIO available to user. Connected to TWL4030 GPIO.0. This signal has a 4.7K pull-down resistor.
141	uP_nCS_B_EXT	O	1.8V	External Chip select available for customer use.
142	uP_GPIO_3	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_111.
143	uP_nCS_A_EXT	O	1.8V	External Chip select available for customer use.
144	VREF_I2C2 (VIO_1V8)	O	1.8V	Reference voltage output for I2C DATA and CLK signals.
145	SLOW_nCS (uP_nCS_B_EXT)	O	1.8V	External Chip select available for customer use.
146	uP_I2C2_SDA	I/O	1.8V	I2C channel 2 data signal. This signal has a 4.7K pull-up to the reference voltage onboard.
147	FAST_nCS (uP_nCS_A_EXT)	O	1.8V	External Chip select available for customer use.
148	uP_I2C2_SCL	I/O	1.8V	I2C channel 2 clock signal. This signal has a 4.7K pull-up to the reference voltage onboard.
149	DGND	I	GND	Ground. Connect to digital ground.
150	DGND	I	GND	Ground. Connect to digital ground.
151	RFU	I/O	NA	Reserved for future use. Do not connect.
152	VREF_UARTA (VIO_1V8)	O	1.8V	Voltage reference output for UART1 signals.
153	RFU	I/O	NA	Reserved for future use. Do not connect.

J1 Pin#	Signal Name	I/O	Voltage	Description
154	uP_UARTA_DSR	I	1.8V	Data Set Ready signal for UART1.
155	RFU	I/O	NA	Reserved for future use. Do not connect.
156	uP_UARTA_DTR	O	1.8V	Data Terminal Ready signal for UART1.
157	RFU	I/O	NA	Reserved for future use. Do not connect.
158	uP_UARTA_RX	I	1.8V	Data Receive signal for UART1.
159	RFU	I/O	NA	Reserved for future use. Do not connect.
160	uP_UARTA_TX	O	1.8V	Data Transmit signal for UART1.
161	LCD_PANEL_PWR	O	1.8V	LCD Panel Power signal.
162	uP_UARTA_CTS	I	1.8V	Clear To Send signal for UART1.
163	LCD_BACKLIGHT_PWR	O	1.8V	LCD Backlight Power signal. Active High.
164	uP_UARTA_RTS	O	1.8V	Ready To Send signal for UART1.
165	LCD_HSYNC	O	1.8V	LCD Horizontal Sync signal.
166	uP_GPIO_2	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_31.
167	LCD_VSYNC	O	1.8V	LCD Vertical Sync Signal.
168	PWM0	O	1.8V	PWM output 0.
169	DGND	I	GND	Ground. Connect to digital ground.
170	DGND	I	GND	Ground. Connect to digital ground.
171	LCD_DCLK	O	1.8V	LCD Data Clock output.
172	BACKUP_BATT	I	1.8V-3.3V	External input that supplies power to the onboard power management controller and RTC interface. This signal should be powered by a coin-cell type battery or an always-on power source.
173	RFU	I/O	NA	Reserved for future use. Do not connect.
174	5V	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used.
175	LCD_MDISP	O	1.8V	LCD MDISP signal.
176	5V	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used.
177	RFU	I/O	NA	Reserved for future use. Do not connect.
178	5V	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used.
179	RFU	I/O	NA	Reserved for future use. Do not connect.
180	3.3V	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
181	RFU	I/O	NA	Reserved for future use. Do not connect.
182	3.3V	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
183	LCD_VREF (VPLL2)	O	1.8V	Voltage reference output for the LCD interface.
184	3.3V	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
185	R1 (LCD_D11)	O	1.8V	LCD R1 data bit when operating in 16 bpp 5:6:5 color mode.
186	TOUCH_LEFT	I	max 3.0V	Touch panel LEFT input signal.
187	R2 (LCD_D12)	O	1.8V	LCD R2 data bit when operating in 16 bpp 5:6:5 color mode.
188	TOUCH_RIGHT	I	max 3.0V	Touch panel RIGHT input signal.
189	DGND	I	GND	Ground. Connect to digital ground.
190	DGND	I	GND	Ground. Connect to digital ground.
191	R3 (LCD_D13)	O	1.8V	LCD R3 data bit when operating in 16 bpp 5:6:5 color mode.
192	TOUCH_BOTTOM	I	max 3.0V	Touch panel BOTTOM input signal.

J1 Pin#	Signal Name	I/O	Voltage	Description
193	R4 (LCD_D14)	O	1.8V	LCD R4 data bit when operating in 16 bpp 5:6:5 color mode.
194	TOUCH_TOP	I	max 3.0V	Touch panel TOP input signal.
195	R5 (LCD_D15)	O	1.8V	LCD R5 data bit when operating in 16 bpp 5:6:5 color mode.
196	A/D4	I	max 2.7V	Analog to digital converter input. Connected to TWL4030 ADCIN5.
197	G0 (LCD_D5)	O	1.8V	LCD G0 data bit when operating in 16 bpp 5:6:5 color mode.
198	A/D3	I	max 2.7V	Analog to digital converter input. Connected to TWL4030 ADCIN4.
199	G1 (LCD_D6)	O	1.8V	LCD G1 data bit when operating in 16 bpp 5:6:5 color mode.
200	A/D2	I	max 2.7V	Analog to digital converter input. Connected to TWL4030 ADCIN3.
201	G2 (LCD_D7)	O	1.8V	LCD G2 data bit when operating in 16 bpp 5:6:5 color mode.
202	A/D1	I	max 3.0V	Analog to digital converter input. Connected to Touch chip's AUX input.
203	G3 (LCD_D8)	O	1.8V	LCD G3 data bit when operating in 16 bpp 5:6:5 color mode.
204	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
205	G4 (LCD_D9)	O	1.8V	LCD G4 data bit when operating in 16 bpp 5:6:5 color mode.
206	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
207	G5 (LCD_D10)	O	1.8V	LCD G5 data bit when operating in 16 bpp 5:6:5 color mode.
208	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
209	DGND	I	GND	Ground. Connect to digital ground.
210	DGND	I	GND	Ground. Connect to digital ground.
211	B1 (LCD_D0)	O	1.8V	LCD B1 data bit when operating in 16 bpp 5:6:5 color mode.
212	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
213	B2 (LCD_D1)	O	1.8V	LCD B2 data bit when operating in 16 bpp 5:6:5 color mode.
214	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
215	B3 (LCD_D2)	O	1.8V	LCD B3 data bit when operating in 16 bpp 5:6:5 color mode.
216	uP_GPIO_1	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_11.
217	B4 (LCD_D3)	O	1.8V	LCD B4 data bit when operating in 16 bpp 5:6:5 color mode.
218	uP_GPIO_0	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_133.
219	B5 (LCD_D4)	O	1.8V	LCD B5 data bit when operating in 16 bpp 5:6:5 color mode.
220	uP_SPI_CS1	O	1.8V	McSPI3 interface chip select 1 output.
221	ONE_WIRE (BATT_LINE)	I/O	1.8V	Bi-directional battery management ONEWIRE interface. This signal has a 4.7K pull-up to VIO_1V8.

J1 Pin#	Signal Name	I/O	Voltage	Description
222	uP_SPI_CS0	O	1.8V	McSPI3 interface chip select 0 output.
223	uP_SW_nRESET (SYS_nRESWARM)	I	1.8V	Active low. Input to CPU and power management controller. This signal has a 4.7K pull-up to VIO_1V8.
224	uP_SPI_SOMI	I	1.8V	McSPI3 interface receive input.
225	RESET_nOUT (SYS_nRESWARM)	O	1.8V	Active low. Reset output from the CPU that drives all onboard reset inputs. This signal should be used to drive reset inputs on external chips that require similar timing to the onboard devices. The SYS_nRESWARM signal has a 4.7K pull-up to VIO_1V8.
226	uP_SPI_SIMO	O	1.8V	McSPI3 interface transmit output.
227	MSTR_nRST	I	1.8V	Active low. External reset input to the SOM-LV. This signal should be used to reset all devices on the SOM-LV including the CPU.
228	uP_SPI_SCLK	O	1.8V	McSPI3 serial clock signal.
229	DGND	I	GND	Ground. Connect to digital ground.
230	DGND	I	GND	Ground. Connect to digital ground.
231	VMMC2	O	VMMC2	VMMC2 LDO output from TWL4030 available to user.
232	TOUCH_nIRQ	O	1.8V	If touch chip is populated, this signal is the active low touch interrupt; do not connect. If touch chip is not populated, this signal is a proccesor GPIO available to user; connected to GPIO_153.
233	RFU	I/O	NA	Reserved for future use. Do not connect.
234	RFU	I/O	NA	Reserved for future use. Do not connect.
235	RFU	I/O	NA	Reserved for future use. Do not connect.
236	RFU	I/O	NA	Reserved for future use. Do not connect.
237	RFU	I/O	NA	Reserved for future use. Do not connect.
238	RFU	I/O	NA	Reserved for future use. Do not connect.
239	RFU	I/O	NA	Reserved for future use. Do not connect.
240	RFU	I/O	NA	Reserved for future use. Do not connect.

Note 1: The signals in parentheses are the net names specific to OMAP3430 SOM-LV; the non-parenenthetical names are the signal names that are general to the form factor module.

5.2 J2 Connector 240-Pin Descriptions

J2 Pin#	Signal Name	I/O	Voltage	Description
1	RFU	I/O	NA	Reserved for future use. Do not connect.
2	RFU	I/O	NA	Reserved for future use. Do not connect.
3	RFU	I/O	NA	Reserved for future use. Do not connect.
4	RFU	I/O	NA	Reserved for future use. Do not connect.
5	RFU	I/O	NA	Reserved for future use. Do not connect.
6	RFU	I/O	NA	Reserved for future use. Do not connect.
7	WLAN_nIRQ	O	1.8V	If Ethernet chip is populated, this signal is the active low Ethernet interrupt; do not connect. If Ethernet chip is not populated, this signal is a proccesor GPIO available to user; connected to GPIO_152.
8	RFU	I/O	NA	Reserved for future use. Do not connect.
9	ICT_TEST_MODE	I	1.8V	Used for test only. Do not connect.
10	uP_CLKOUT2_26MHz	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_186.
11	DGND	I	GND	Ground. Connect to digital ground.
12	DGND	I	GND	Ground. Connect to digital ground.
13	PCC_POWER_nEN (SIM0_VEN)	O	1.8V	Active low. Turns on power to CompactFlash/PC Card interface.

J2 Pin#	Signal Name	I/O	Voltage	Description
14	PCC_nOE (uP_nOE)	O	1.8V	Active low. CompactFlash/PC Card per transaction bus buffer Output Enable signal.
15	PCC_PCMCIA_nEN (SIM0_VEN)	O	1.8V	Active low. Enables CompactFlash control signals.
16	RFU	I/O	NA	Reserved for future use. Do not connect.
17	HSUSB1_D7	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_17.
18	uP_PCC_nWAIT	I	1.8V	Active low. CompactFlash/PC Card Wait signal.
19	HSUSB1_D6	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_20.
20	RFU	I/O	NA	Reserved for future use. Do not connect.
21	HSUSB1_D5	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_19.
22	RFU	I/O	NA	Reserved for future use. Do not connect.
23	HSUSB1_D4	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_18.
24	uP_PCC_CD2 (uP_PCC_CD1)	I	1.8V	CompactFlash/ PC Card Detect 2 input.
25	HSUSB1_D3	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_21.
26	uP_PCC_CD1	I	1.8V	CompactFlash/ PC Card Detect 1 input.
27	HSUSB1_D2	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_16.
28	RFU	I/O	NA	Reserved for future use. Do not connect.
29	HSUSB1_D1	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_15.
30	RFU	I/O	NA	Reserved for future use. Do not connect.
31	DGND	I	GND	Ground. Connect to digital ground.
32	DGND	I	GND	Ground. Connect to digital ground.
33	HSUSB1_CLK	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_13.
34	uP_PCC_RESET	O	1.8V	CompactFlash/PC Card Reset output.
35	HSUSB1_NXT	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_23.
36	PCC_nDRV (uP_nCS3)	O	1.8V	CompactFlash/PC Card buffer Drive output.
37	HSUSB1_STP	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_12.
38	PCC_nIOWR (VIO_1V8)	O	1.8V	Active low. CompactFlash/PC Card I/O Write output.
39	HSUSB1_DIR	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_22.
40	PCC_nWE (uP_nWE)	O	1.8V	Active low. CompactFlash/PC Card Write Enable output.
41	HSUSB1_D0	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_14.
42	PCC_nIORD (VIO_1V8)	O	1.8V	Active low. CompactFlash/PC Card I/O Read output.
43	HSUSB2_STP	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_25. If R71 not populated, reserved for future use; do not connect.
44	PCC_REG (VIO_1V8)	O	1.8V	CompactFlash/PC Card Reg access output.
45	HSUSB2_D1	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_29. If R71 not populated, reserved for future use; do not connect.
46	RFU	I/O	NA	Reserved for future use. Do not connect.
47	HSUSB2_D0	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_28. If R71 not populated, reserved for future use; do not connect.

J2 Pin#	Signal Name	I/O	Voltage	Description
48	PCC_nCE1A (uP_nCS3)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 1A.
49	MCSPI_CS1 (HSUSB2_D3)	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_182. If R71 not populated, reserved for future use; do not connect.
50	PCC_nCE2A (uP_nCS3)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 2A.
51	DGND	I	GND	Ground. Connect to digital ground.
52	DGND	I	GND	Ground. Connect to digital ground.
53	MCSPI2_CS0 (HSUSB2_D6)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_181. If R70 not populated, reserved for future use; do not connect.
54	VREF_PCMCIA (VIO_1V8)	O	1.8V	CompactFlash/PC Card Voltage reference output.
55	MCSPI2_SOMI (HSUSB2_D5)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_180. If R70 not populated, reserved for future use; do not connect.
56	A26 (uP_A10)	O	1.8V	Processor GPMC bus address bit 26. (see note 1)
57	MCSPI2_SIMO (HSUSB2_D4)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_179. If R70 not populated, reserved for future use; do not connect.
58	RFU	I/O	NA	Reserved for future use. Do not connect.
59	MCSPI2_CLK (HSUSB2_D7)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_178. If R70 not populated, reserved for future use; do not connect.
60	RFU	I/O	NA	Reserved for future use. Do not connect.
61	RFU	I/O	NA	Reserved for future use. Do not connect.
62	RFU	I/O	NA	Reserved for future use. Do not connect.
63	RFU	I/O	NA	Reserved for future use. Do not connect.
64	RFU	I/O	NA	Reserved for future use. Do not connect.
65	RFU	I/O	NA	Reserved for future use. Do not connect.
66	RFU	I/O	NA	Reserved for future use. Do not connect.
67	RFU	I/O	NA	Reserved for future use. Do not connect.
68	RFU	I/O	NA	Reserved for future use. Do not connect.
69	RFU	I/O	NA	Reserved for future use. Do not connect.
70	RFU	I/O	NA	Reserved for future use. Do not connect.
71	DGND	I	GND	Ground. Connect to digital ground.
72	DGND	I	GND	Ground. Connect to digital ground.
73	RFU	I/O	NA	Reserved for future use. Do not connect.
74	RFU	I/O	NA	Reserved for future use. Do not connect.
75	VIBRA_M	O	MAIN_BATTERY	Vibrator M signal for H-Bridge operation.
76	RFU	I/O	NA	Reserved for future use. Do not connect.
77	VIBRA_P	O	MAIN_BATTERY	Vibrator P signal for H-Bridge operation.
78	RFU	I/O	NA	Reserved for future use. Do not connect.
79	START_ADC	I	1.8V	This signal is the TWL4030 ADC conversion request.
80	VREF_MMC/SD1 (VMMC1)	O	VMMC1	MMC/SD1 interface voltage reference output.
81	RF_LED0	O	3.0V	Wireless LAN LED0 signal.
82	SD1_DATA3	I/O	VMMC1	MMC/SD2 Data 3 signal. This signal has a 10K pull-up to VMMC1.
83	RF_LED1	O	3.0V	Wireless LAN LED1 signal.
84	SD1_DATA2	I/O	VMMC1	MMC/SD2 Data 2 signal. This signal has a 10K pull-up to VMMC1.

J2 Pin#	Signal Name	I/O	Voltage	Description
85	uP_nWP	O	1.8V	Processor GPMC write protect signal.
86	SD1_DATA1	I/O	VMMC1	MMC/SD2 Data 1 signal. This signal has a 10K pull-up to VMMC1.
87	uP_nADV_ALE	O	1.8V	Processor GPMC address valid or address latch enable signal.
88	SD1_DATA0	I/O	VMMC1	MMC/SD2 Data 0 signal. This signal has a 10K pull-up to VMMC1.
89	RFID_EN	O	VMMC2	RFID device enable.
90	SD1_CMD	I/O	VMMC1	MMC/SD2 Command signal. This signal has a 10K pull-up to VMMC1.
91	DGND	I	GND	Ground. Connect to digital ground.
92	DGND	I	GND	Ground. Connect to digital ground.
93	KEY_COL7	I/O	1.8V	Keypad Column 7 signal.
94	SD1_CLK	O	VMMC1	MMC/SD2 Clock signal. This signal has a 10K pull-up to VMMC1.
95	KEY_COL6	I/O	1.8V	Keypad Column 6 signal.
96	VREF_I2C3 (VIO_1V8)	O	1.8V	I2C channel 3 voltage reference output.
97	KEY_COL5	I/O	1.8V	Keypad Column 5 signal.
98	uP_I2C3_SCL	I/O	1.8V	I2C channel 3 Clock signal.
99	KEY_COL4	I/O	1.8V	Keypad Column 4 signal.
100	uP_I2C3_SDA	I/O	1.8V	I2C channel 3 Data signal.
101	KEY_COL3	I/O	1.8V	Keypad Column 3 signal.
102	RFU	I/O	NA	Reserved for future use. Do not connect.
103	KEY_COL2	I/O	1.8V	Keypad Column 2 signal.
104	RFU	I/O	NA	Reserved for future use. Do not connect.
105	KEY_COL1	I/O	1.8V	Keypad Column 1 signal.
106	RFU	I/O	NA	Reserved for future use. Do not connect.
107	KEY_COL0	I/O	1.8V	Keypad Column 0 signal.
108	uP_TMS	I	1.8V	CPU JTAG Test Mode Signal.
109	KEY_ROW7	I/O	1.8V	Keypad Row 7 signal.
110	uP_TCK	I	1.8V	CPU JTAG Test Clock input signal.
111	DGND	I	GND	Ground. Connect to digital ground.
112	DGND	I	GND	Ground. Connect to digital ground.
113	KEY_ROW6	I/O	1.8V	Keypad Row 6 signal.
114	uP_TDO	O	1.8V	CPU JTAG Test Data Output from the CPU to the JTAG device.
115	KEY_ROW5	I/O	1.8V	Keypad Row 5 signal.
116	uP_nTRST	I	1.8V	CPU JTAG Test Reset input.
117	KEY_ROW4	I/O	1.8V	Keypad Row 4 signal.
118	uP_TDI	I	1.8V	CPU JTAG Test Data Input to the CPU from the JTAG device.
119	KEY_ROW3	I/O	1.8V	Keypad Row 3 signal.
120	uP_RTCK	O	1.8V	CPU JTAG Return Test Clock signal.
121	KEY_ROW2	I/O	1.8V	Keypad Row 2 signal.
122	VREF_JTAG (VIO_1V8)	O	1.8V	CPU JTAG reference voltage output.
123	KEY_ROW1	I/O	1.8V	Keypad Row 1 signal.
124	SIM0_VEN	O	VSIM	Smart card voltage enable.
125	KEY_ROW0	I/O	1.8V	Keypad Row 0 signal.
126	SIM0_nDETECT	I	VSIM	Smart card detect.
127	CSI_HSYNC	I/O	1.8V	Camera Sensor Interface Horizontal Sync signal.
128	SIM0_CLK	O	VSIM	Smart card clock output.
129	DGND	I	GND	Ground. Connect to digital ground.
130	DGND	I	GND	Ground. Connect to digital ground.
131	CSI_VSYNC	I/O	1.8V	Camera Sensor Interface Vertical Sync signal.
132	SIM0_IO/TX	I/O	VSIM	Smart card data inout signal.
133	CSI_D0	I	1.8V	Camera Sensor Interface Data bit 0.
134	RFU	I/O	NA	Reserved for future use. Do not connect.

J2 Pin#	Signal Name	I/O	Voltage	Description
135	CSI_D1	I	1.8V	Camera Sensor Interface Data bit 1.
136	SIM0_nRESET	O	VSIM	Smart card reset.
137	CSI_D2	I	1.8V	Camera Sensor Interface Data bit 2.
138	VREF_SIM (VSIM)	O	VSIM	Smart card reference voltage.
139	CSI_D3	I	1.8V	Camera Sensor Interface Data bit 3.
140	RFU	I/O	NA	Reserved for future use. Do not connect.
141	CSI_D4	I	1.8V	Camera Sensor Interface Data bit 4.
142	ICT_JTAG_TDO	O	1.8V	Used for test only. Do not connect.
143	CSI_D5	I	1.8V	Camera Sensor Interface Data bit 5.
144	ICT_JTAG_TMS	I	1.8V	Used for test only. Do not connect.
145	CSI_D6	I	1.8V	Camera Sensor Interface Data bit 6.
146	ICT_JTAG_TDI	I	1.8V	Used for test only. Do not connect.
147	CSI_D7	I	1.8V	Camera Sensor Interface Data bit 7.
148	ICT_JTAG_CLK	I	1.8V	Used for test only. Do not connect.
149	DGND	I	GND	Ground. Connect to digital ground.
150	DGND	I	GND	Ground. Connect to digital ground.
151	CSI_D8	I	1.8V	Camera Sensor Interface Data bit 8.
152	uP_GPIO_2	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_31.
153	CSI_D9	I	1.8V	Camera Sensor Interface Data bit 9.
154	uP_GPIO_1	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_11.
155	CSI_D10	I	1.8V	Camera Sensor Interface Data bit 10.
156	BT_PCM_DX	I/O	1.8V	TWL4030 GPIO available to user. Connected to TWL4030 GPIO.17.
157	CSI_D11	I	1.8V	Camera Sensor Interface Data bit 11.
158	BT_PCM_DR	I/O	1.8V	TWL4030 GPIO available to user. Connected to TWL4030 GPIO.16.
159	RFU	I/O	NA	Reserved for future use. Do not connect.
160	BT_PCM_VFS	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_143.
161	RFU	I/O	NA	Reserved for future use. Do not connect.
162	PCM_DX	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_141.
163	RFU	I/O	NA	Reserved for future use. Do not connect.
164	PCM_DR	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_140.
165	RFU	I/O	NA	Reserved for future use. Do not connect.
166	BT_PCM_CLK	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_142.
167	CSI_MCLK	O	1.8V	Camera Sensor Interface Master Clock signal.
168	EXT_BOOT_nSELECT	I	1.8V	Boot select signal (0 = external boot device, 1 = onboard NOR flash, if populated). This is accomplished by onboard logic: if signal EXT_BOOT_nSELECT is high, then NOR_nCS = uP_nCS2; if signal EXT_BOOT_nSELECT is low, then BOOT_nCS = uP_nCS2. This defaults to the onboard flash if left unconnected (pulled to 1.8V through a 10K resistor). Note: R57 must be populated to boot from NOR or an external device.
169	DGND	I	GND	Ground. Connect to digital ground.
170	DGND	I	GND	Ground. Connect to digital ground.
171	CSI_PCLK	I	1.8V	Camera Sensor Interface Pixel Clock signal.
172	BOOT_nCS	O	1.8V	Active Low. This signal is connected to uP_nCS2 when EXT_BOOT_nSELECT is low. When EXT_BOOT_nSELECT is high, this signal is inactive. This signal has a 4.7K pull-up to VIO_1V8.

J2 Pin#	Signal Name	I/O	Voltage	Description
173	VREF_CSI (VPLL2)	O	VPLL2	Camera Sensor Interface reference voltage output.
174	LCD_D23	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
175	VAUX3	O	VAUX3	Auxilary power supply available to user.
176	LCD_D22	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
177	TWL_CLK256FS	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_160.
178	LCD_D21	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
179	RFU	I/O	NA	Reserved for future use. Do not connect.
180	LCD_D20	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
181	CSI1_DY1	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DX1.
182	LCD_D19	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
183	CSI1_DX1	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DY1.
184	LCD_D18	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
185	CSI1_DY0	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DX0.
186	LCD_D17	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
187	CSI1_DX0	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DY0.
188	LCD_D16	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP34xx TRM for LCD bus mapping.
189	DGND	I	GND	Ground. Connect to digital ground.
190	DGND	I	GND	Ground. Connect to digital ground.
191	MCSPI1_SOMI	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_173.
192	TV_OUT2	O	VDAC	Analog TV_OUT2.
193	T2_REGEN	O	MAIN_BATTERY	Active high. External LDO enable signal generated by the TWL4030.
194	TV_OUT1	O	VDAC	Analog TV_OUT1.
195	ADCIN6	I	max 2.7V	Analog to digital converter input. Connected to TWL4030 ADCIN6.
196	ADCIN2	I	1.5V	Analog to digital converter input. Connected to TWL4030 ADCIN2.
197	WLAN_MMC3_DATA3	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_139.
198	ADCIN1	I	1.5V	Analog to digital converter input. Connected to TWL4030 ADCIN1.
199	WLAN_MMC3_DATA2	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_138.

J2 Pin#	Signal Name	I/O	Voltage	Description
200	ADCIN0	I	1.5V	Analog to digital converter input. Connected to TWL4030 ADCIN0.
201	WLAN_MMC3_DATA1	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_137.
202	IHF_RIGHT_M	O	MAIN_BATTERY	Hands-free speaker output right (M).
203	WLAN_MMC3_DATA0	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_136.
204	IHF_RIGHT_P	O	MAIN_BATTERY	Hands-free speaker output right (P).
205	WLAN_MMC3_CMD	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_175.
206	IHF_LEFT_M	O	MAIN_BATTERY	Hands-free speaker output left (M).
207	WLAN_MMC3_CLK	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_176.
208	IHF_LEFT_P	O	MAIN_BATTERY	Hands-free speaker output right (P).
209	DGND	I	GND	Ground. Connect to digital ground.
210	DGND	I	GND	Ground. Connect to digital ground.
211	MCSPI1_CLK	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_171.
212	MIC_IN	I	max 2.7V	Microphone input.
213	MCSPI1_SIMO	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_172.
214	MIC_SUB_M	I	MICBIAS2	Main microphone right input (M).
215	MCSPI1_CS0	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_174.
216	MIC_SUB_P	I	MICBIAS2	Main microphone right input (P).
217	MICBIAS2	O	MICBIAS2	Analog microphone bias 2.
218	MIC_MAIN_M	I	MICBIAS1	Main microphone left input (M).
219	MICBIAS1	O	MICBIAS1	Analog microphone bias 1.
220	MIC_MAIN_P	I	MICBIAS1	Main microphone left input (P).
221	MCBSP2_CLKX	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_117.
222	CODEC_INL	I	max 2.7V	Auxiliary left channel line in.
223	MCBSP2_FSX	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_116.
224	CODEC_INR	I	max 2.7V	Auxiliary right channel line in.
225	MCBSP2_DR	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_118.
226	CODEC_OUTL	O	max 2.7V	Left channel line out.
227	MCBSP2_DX	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_119.
228	CODEC_OUTR	O	max 2.7V	Right channel line out.
229	DGND	I	GND	Ground. Connect to digital ground.
230	DGND	I	GND	Ground. Connect to digital ground.
231	T2_CLKREQ	I/O	NA	Reserved for future use. Do not connect.
232	BT_IRQ	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_157.
233	uP_CLKOUT1_26MHz	O	1.8V	Processor SYS_CLKOUT1.
234	TWL_32K_CLK_OUT	O	1.8V	TWL4030 32kHz clock output.

J2 Pin#	Signal Name	I/O	Voltage	Description
235	RFU	I/O	NA	Reserved for future use. Do not connect.
236	RFU	I/O	NA	Reserved for future use. Do not connect.
237	RFU	I/O	NA	Reserved for future use. Do not connect.
238	RFU	I/O	NA	Reserved for future use. Do not connect.
239	RFU	I/O	NA	Reserved for future use. Do not connect.
240	RFU	I/O	NA	Reserved for future use. Do not connect.

6 Mechanical Specifications

6.1 Interface Connectors

The OMAP3430 SOM-LV connects to a PCB baseboard through two 240-pin board-to-board (BTB) socket connectors.

Ref Designator	Manufacturer	SOM-LV Connector P/N	Mating Connector P/N
J1, J2	Samtec	BTH-120-01-L-D-A	BSH-120-01-L-D-A

6.2 SOM-LV Mechanical Drawings

Notes:

1. All measurements are in mm.
2. All hole dimensions have a ± 0.01 mm tolerance.
3. Maximum component height on bottom of board is 3.8 mm.
4. Point of origin is the mounting hole filled in with a solid color.
5. Connector measurements point to connector alignment holes.

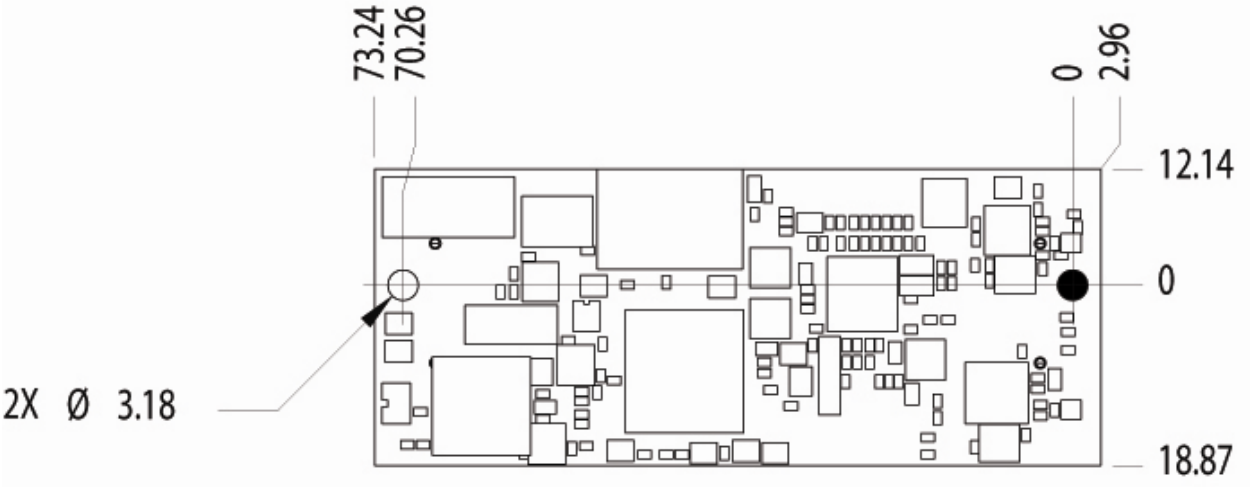

Figure 6.1: OMAP3430 SOM-LV Top View

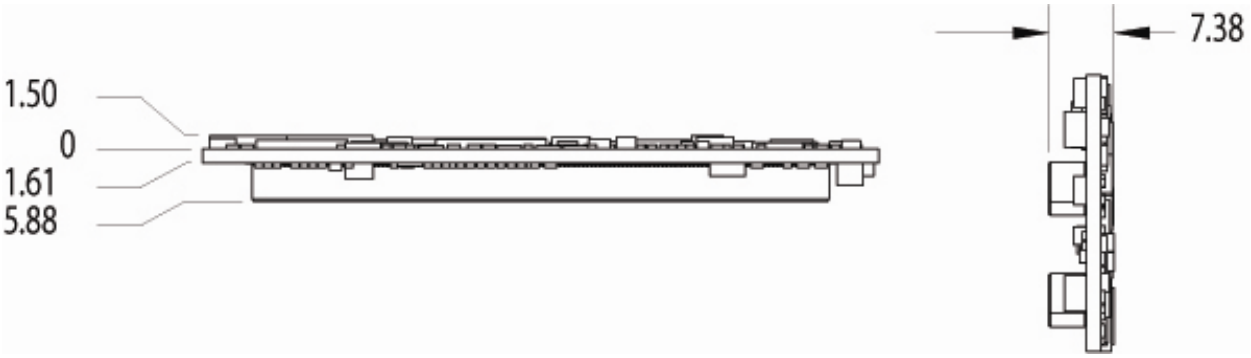

Figure 6.2: OMAP3430 SOM-LV Side View

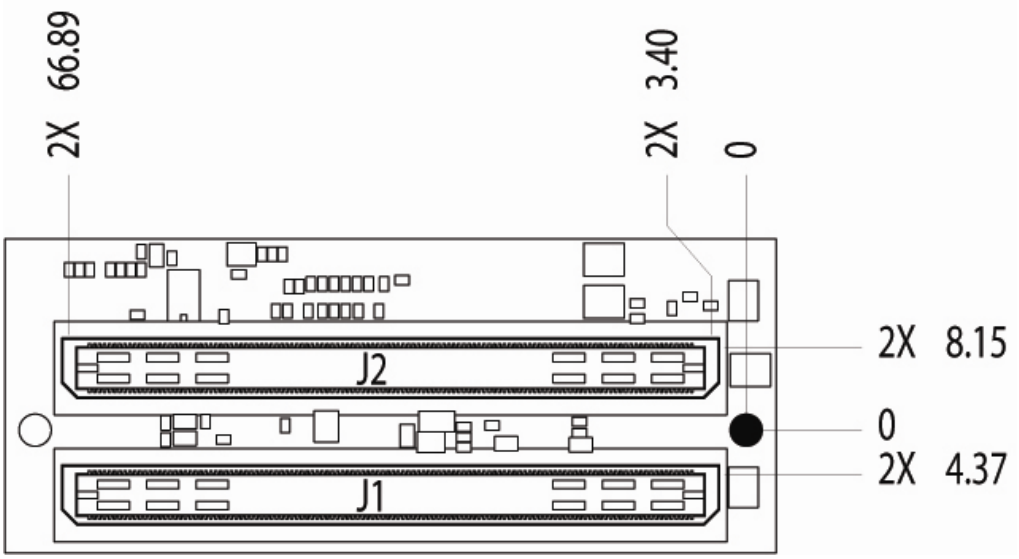

Figure 6.3: OMAP3430 SOM-LV Bottom View

6.3 Recommended Baseboard PCB Layout

Notes:

1. All measurements are in mm.
2. All hole dimensions have a ± 0.01 mm tolerance.
3. Within the layout area of the SOM-LV, the maximum component height on the application baseboard is 1.0 mm.
4. Point of origin is the mounting hole filled in with a solid color.
5. Connector measurements point to connector alignment holes.

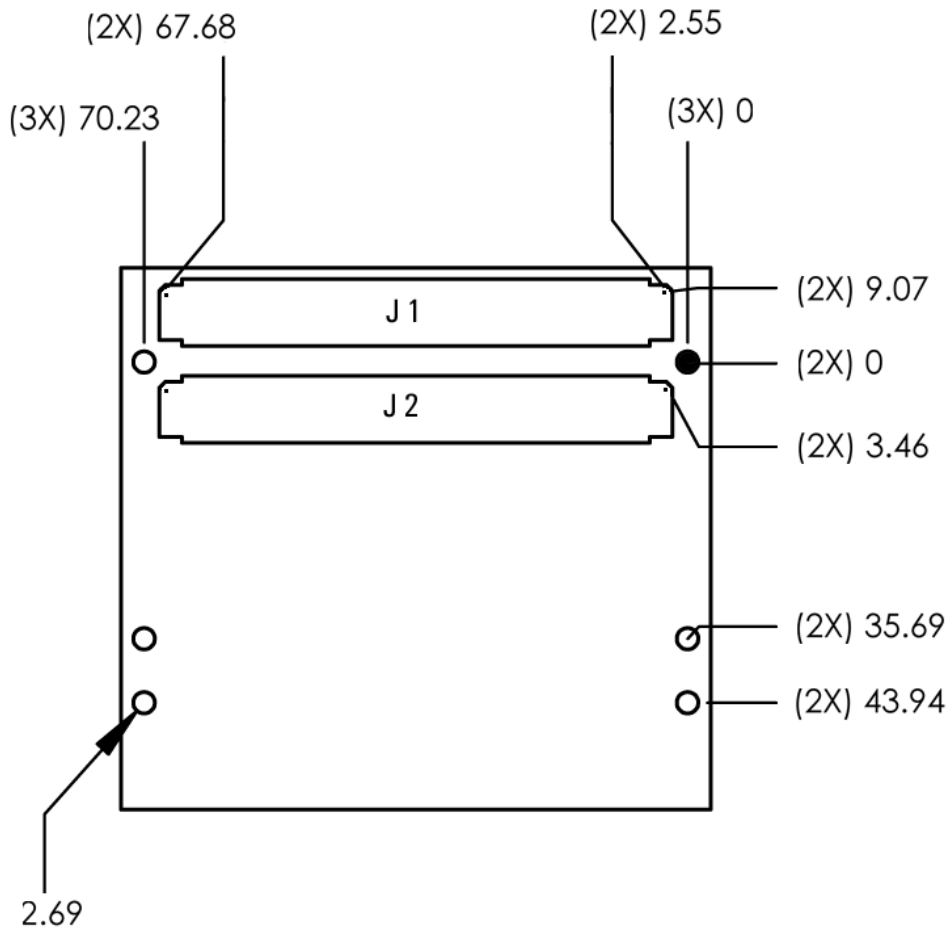

Figure 6.4: Baseboard Footprint for the SOM-LV