Multi-Card Engine Design

White Paper 184

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Abstract

An OEM's ability to use multiple card engines on the same base board allows for upgrades to more advanced products and/or different levels of functionality without changing the underlying hardware. Designing a base board for multiple card engines is called Multi-Card Engine Design. This white paper outlines common design practices, tools, and areas of concern to keep in mind when designing a base board for multiple card engines.

REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
1	Andrew Wawra	Preliminary Version	AW	05/2003
A	Kurt Larson	Release	HAR	12/01/2003
B	James Wicks	Card Engine Pin-out Chart Text	JAW	07/19/2004

1 Introduction

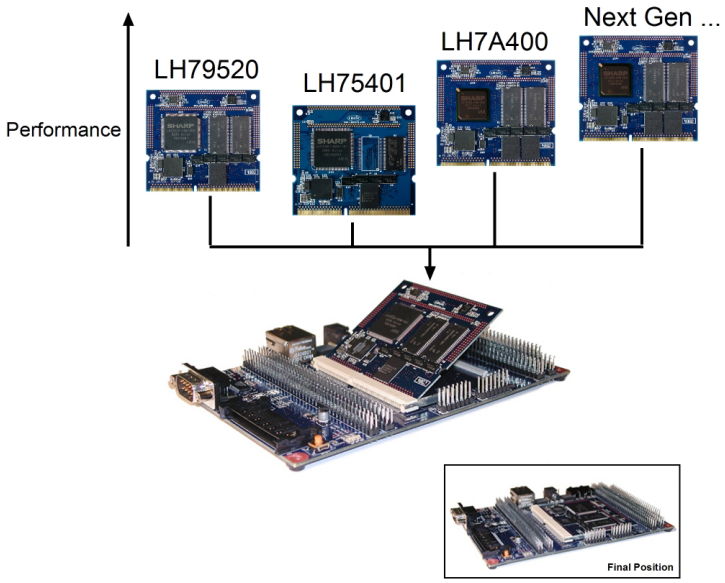
Multi-Card Engine design offers many advantages to OEM's developing products. This white paper explains these advantages in the following sections: Card Engine Concept, Card Engine Interface, and Card Engine Pin-Out Chart.

2 Card Engine Concept

Logic's card engines can greatly accelerate your product's time to market. In addition, the card engines provide the following advantages:

- Product Ready Hardware & Software solutions allow immediate application development which results in embedded product development cycle with less time, less cost, less risk, and more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More Innovation – Allows you to focus on your IP
- Common Card Engine Footprint (See Figure 1)
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

Figure 1: Card Engine Advantages



- Encapsulating a significant amount of your design onto the card engine reduces risk of obsolescence issues. If a component on the card engine design becomes obsolete you don't have to re-spin your board, Logic will design for alternative part that is transparent to your product. Manufacturing also becomes much easier. Card engines are delivered to you fully tested, making your manufacturing process simpler and less costly.

3 Card Engine Interface

The card engine's common interface allows you to easily migrate to new processors and technology. By using the common footprint, you can leverage Logic's work without having to re-spin your product.

The card engine interface is based on a 144-SODIMM connector and two 80 pin high density connectors. These connectors have generic signal designations across all card engine designs.

The signals from the 144-SODIMM connector contain the essential power and ground signals required to operate the card engine and the main host interface connection signals. The 144-SODIMM connector designated J1C contains the address, data, interrupt, host bus, Ethernet, SPI, Mode, and UARTA signals.

Expansion connector J1A contains the LCD, AC97, USB, AUDIO, Touch, Sense, and ADC signals.

Expansion connector J1B contains PCMCIA, IR, UARTB, UARTC, and Multi Function Pins. (MFP's) MFP's allow each card engine to use the variety of peripherals each processor supports, and are usually the area of greatest concern in multi-card engine design.

3.1 144-SODIMM Signals

3.1.1 Data Bus

The SODIMM connector has 32 pins dedicated for card engine data bus signals. Depending on the specific card engine chosen, the processor could have a 16 bit, 32 bit, or 64 bit internal data bus.

If the processor has a bus larger than 32 bits, only the lower 32 bits of the data bus will be provided external to the card engine. If the processor has 32 data bits or less, the entire data bus is provided off the card engine.

The data signal location, for a bus less than 32 bits, aligns at the locations of the lower bits of the 32 dedicated data signals on the card engine. For example, the LH75401 card engine has a 16 bit data bus. The processor data signals D0 to D15 are connected directly to the LH75401 card engine 144-SODIMM connector locations D0-D15. D16-D31 are *not connected* on the LH75401 card engine.

All 32 data signals are buffered on the card engine.

3.1.2 Address Bus

The SODIMM connector has dedicated locations for up to 28 address lines. Some card engines utilize processors that support less than all 28 address lines.

The Integrated Development Kit (IDK) reference design includes a CPLD that has memory mapped registers which utilize A25 down to A20 for address decoding. To allow the address decoding across all card engines on the IDK and similar designs, card engines based on processors with less that 25 address lines (e.g. LH75401-based card engines) shift their high order address lines up to fill the A25 down to A20 slots.

It is important to refer to the documentation for each specific card engine before a design begins to understand the routing of address lines A25-A20 on the SODIMM connector.

3.1.3 Ethernet Controller

Currently all card engines support an onboard 10/100 Ethernet controller. The Ethernet signals on the SODIMM connector have dedicated locations for TX and RX pairs, an nLINK, and nACT LED signals. Follow the Starter Development Kit (SDK) or IDK reference designs for proper connector interfacing including required impedance matching circuitry.

3.1.4 SPI

The availability of the SODIMM dedicated SPI interface is dependent on the availability of the SPI supported by the processor.

Some processors support multiple serial interfaces in which the superset is called a Synchronous Serial Port (SSP); these processors include compatibility with the following formats: Motorola SPI, National Semiconductor MICROWIRE, and Texas Instruments Synchronous Serial Interfaces.

Not all card engines support the full SSP - it depends on the on the product selected. Please refer to the documentation on the specific card engine to determine whether or not it will support the synchronous serial mode required by the design.

3.1.5 Dedicated Interrupts

The dedicated interrupt signals includes four interrupts (uP_nIRQA through uP_nIRQD), and in some cases an additional Non-Maskable Interrupt (nNMI) on the card engine SODIMM interface. Logic attempts to provide four separate interrupts and an nNMI signal for all processors.

In some cases the processor does not support dedicated external interrupts for all four IRQ signals. In those cases, either the onboard CPLD multiplexes multiple external card engine interrupts to a single interrupt that returns to the processor or an interruptable GPIO pin may be used.

Some interrupt signals require a specific level or edge signal to create the interrupt condition. For example, one card engine may require a low level interrupt condition on uP_IRQD, while another will require a falling edge. Please consult the specific card engine documentation.

To design for the greatest degree of compatibility, use the lowest order interrupts first. For example, use uP_nIRQA before using uP_nIRQB.

3.1.6 Mode Pins

The SODIMM has 4 mode pins on every card engine.

To design for multiple card engine compatibility, leave the Mode signals unconnected on the base board if the default software and hardware configuration used on the card engine. If your product requires an external boot device or an Endian setting change, ensure that all the card engines you are designing for support the settings desired.

Mode pins 0 and 1 are used to select the width of the boot device. Mode 0 and Mode 1 have pull ups and pull downs on the card engine to automatically boot from onboard flash.

One item that can easily cause problems is an external boot source. If an external boot source is used, you may have to change Mode pins 0 and 1 for the boot device. If two different card engines are designed in, their Mode 0 and Mode 1 settings may require different pull up or pull down requirements to correctly setup the boot width of the external device. To design for multiple card engines, design the product so that the Mode 0 and Mode 1 pins can be tied to ground or to 3.3V by a different configuration resistor population / build of material configuration.

For prototype designs it may be desirable to put down a strong pull up and a dip switch to ground for ease of configuring these Mode pins. Refer to the IDK design for an implementation of multiple Mode pin settings.

Mode pin 2 selects little or big endian memory architecture and has a pull up on the card engine. Not all card engines support little or big endian selection. Logic's standard is to implement little endian architecture by default.

Mode pin 3 selects on-board or off-board boot device selection. The on-board CPLD reads uP_MODE3 to determine whether to assert the onboard flash chip select FLASH_nCS or the external BOOT_nCS signal. There is a pull-up on the uP_MODE3 signal on the card engine so the device will boot from onboard flash.

3.1.7 Power-on Reset State

Some signals are read by the card engine processor at the end of a power-on reset cycle to define the state of the processor at power-on reset.

Two signals defined on the SODIMM connector that set the processor state upon power-on reset are uP_TEST1 and uP_TEST2. The TEST1 and TEST2 signals are tied directly to the processor and their state at power on reset determines if the processor runs in Normal operation or JTAG/Test mode.

All card engines includes pull-ups on the board to put every processor in Normal operation mode. It is possible to override these signals with jumpers to ground or power on a baseboard to put the processors in JTAG/Test mode. If your design will include a JTAG interface that will be used for development, the uP_TEST1 and uP_TEST2 signals should be connected to configurable jumpers that allow for tying the signal directly to 3.3V power or ground.

Each processor will have a different defined state for the TEST1 and TEST2 pins determining Normal operation and JTAG/Test modes. It is important to have a configuration jumper available for each card engine that will be used on the baseboard. Refer to the SDK or IDK kit documentation for further information on JTAG jumper settings for various card engines and example designs for configuration jumper versatility.

3.1.8 UARTA

The SODIMM connector has a dedicated location for a single UART designated UARTA. UARTA is setup as the debug serial port in Logic software offerings.

The UARTA peripheral has interface support for TX, RX, CTS, RTS, DTR, and DSR hardware signals. However, not every processor supports CTS, RTS, DTR, and DSR UART signals. If these signals are required for your product application, ensure that the card engines you choose to design for have the required control signals on the UARTA port.

The UARTA peripheral should be used as a dedicated manufacturing, field, and debug support serial port.

3.1.9 Local Bus Control

The processor local bus control signals reside at designated locations on the SODIMM connector. Some of the supported signals are nWR, nRD, nCAS, nRAS, nBREQ, nBACK, nWAIT, DREQ, DRAK, DACK, nWE0, nWE1, nWE2, and nWE3. Each of these signals can be used to implement asynchronous or synchronous components on the bus.

From a control signal perspective, not all card engines support external wait states (nWAIT), bus requests(nBREQ, nBACK), or DMA requests (DREQ, DRAK, DACK). Each card engine's

documentation should be consulted before implementing to parts that require asserting external wait states, bus requests, or DMA requests.

There are also four available external memory chip selects for expanded base board devices: FAST_nMCS, SLOW_nMCS, VIDEO_nMCS and BOOT_nMCS. These chip selects are activated when designated areas of the processor's memory are accessed. For example, every card engine's on-board CPLD will have internal registers accessible in the designated FAST_nMCS area. Please consult the individual card engine's hardware specification documents for the specific memory map and usage information on these chip select signals.

3.1.10 Clocks

The SODIMM connector has two clock signals: uP_BUS_CLK and uP_AUX_CLK. On most card engines, these signals are derived from the processor's bus clock.

The uP_BUS_CLK is the clock used on the card engine to clock in bus transactions to the onboard SDRAM and CPLD. uP_AUX_CLK comes from the processor, but is not used on the card engine.

The frequency of uP_BUS_CLK is different for each card engine. The uP_AUX_CLK is controlled in the processor and in some cases has internal dividers and multipliers to get desired output frequencies.

The uP_AUX_CLK signal should be the primary clock used on the base board for bus synchronization. The use of uP_BUS_CLK is discouraged on a baseboard design except as a debugging reference.

When designing for multiple card engine compatibility, note that the uP_BUS_CLK and uP_AUX_CLK frequencies may be different for each card engine.

3.1.11 JTAG

The card engine SODIMM connector has a JTAG interface that consists of TMS, TDO, TDI, TCK, and nTRST signals.

Most processors implement all of these signals for a test/debug JTAG interface. In some cases a processor may have additional test signals required for example RTCK on ARM7 processors. The RTCK signal and any other JTAG signals not included in the above list can be found on the J1B expansion connector on processors that require those signals for proper JTAG operation.

Another item to consider is that different processors may have different JTAG debug devices. The different devices may require different connectors on the baseboard. To save space and cost, designers may opt to put a single connector down that has all available JTAG signals and create different custom cables to connect to each processor specific JTAG device.

3.2 80 pin Expansion Connector J1A Signals

3.2.1 Voltage Sense Resistors

The 80 pin expansion connector J1A has 2 signals designated for a voltage sense resistor on the card engine: POWER_SENSE1 and POWER_SENSE2.

The sense resistor is used as part of a feedback network on the SDK and IDK development kits to determine the required VCORE voltage to supply to the card engine.

Refer to the SDK kit documentation for an example circuit showing a LDO voltage regulator or the IDK kit documentation for an example of a switching supply circuit to create VCORE dynamically for each card engine.

Using the onboard sense resistor, a single VCORE voltage supply design is possible. If the onboard sense resistor is not used, the voltage supply must be able to change the VCORE voltage from 1.4V to 2V depending on the card engines to be used in the product.

Correct implementation of a core voltage control by using these signals or some other mechanism is absolutely essential for successful multi-card engine design.

3.2.2 USB

The J1A expansion connecter holds the 2 dedicated USB signal sets. The USB signals are generically named uP_USBx_M, uP_USBx_P, uP_USBx_nOVR_CRNT, and uP_USBx_PWR_EN. Where x is either 1 or 2. Not all processors have USB support.

When a processor supports USB function/client/device the data signals are connected to the uP_USB1 positions on the J1A expansion connector.

The uP_USB2 J1A expansion connector is used for USB host interface connections.

Some processors have USB client and host interfaces muxed on the same signals which is software selectable. For USB peripherals that have muxed client/host interfaces they muxed USB connection is connected to the up_USB1 signal set.

For processors that support two host and no client connections, the uP_USB1 and uP_USB2 signal sets are used-- one for each host interface.

For processors that support two host and one client connections, uP_USB1 is used for the single client interface, uP_USB2 is used for one host interface, and the second host interface is connected to available MFP pins.

To design a multi-card engine product that utilizes the card engine USB connections, ensure that all card engines intended to be used in the design support the desired USB host/client interfaces.

3.2.3 ADC and DAC

The J1A expansion connector has 4 signals that may support multiple Analog to Digital Converter (ADC) or Digtal to Analog Converter (DAC) signals if the card engine specific processor supports either of these devices.

Some devices may have two ADC’s made available from an onboard Touch Screen Controller. Care must be taken to choose multiple card engines that support the desired functionality if ADC’s or DAC’s are required for the base board design.

3.2.4 Analog Touch

The 4 wire analog touch signals reside on the J1A expansion connector. Depending on the processor, these signals are both driven and sensed by a stand alone touch screen controller IC or are controlled and sensed directly by the processor.

From a software perspective, if using any of Logic's BSPs, the touch software is a seamless interface between card engine products.

Some card engine product processors support a 5 wire touch interface. If your application requires 5 wire touch functionality, the 5th wire in the touch system is made available through the MFP pins on expansion connector J1B. When considering a 5 wire touch design, ensure that all desired card engine products support a 5 wire touch interface before attempting to design the base board.

3.2.5 Audio Out

The card engine CODEC right and left inputs and outputs are available from the J1A expansion connector.

These signals are line level inputs/outputs; however, exact line level voltages may vary between card engine products based on the CODEC used on different card engines.

3.2.6 LCD

Each card engine has a dedicated LCD interface. Each processor supports multiple types of LCD types including Color/Monochrome, STN, DSTN, TFT, HR-TFT, and others.

If the card engine LCD peripheral is required to support a specific display or multiple displays, it is important to verify that each card engine that will be used in the final product can support the desired LCD display.

Each processor may support a different number of LCD resolution bits, the card engine standard supports a 5-6-5 R-G-B format. The LCD connector has been pinned out so that a less than 18bit data bus can still drive all the bits of an 18 bit display.

The processor speed, LCD bandwidth, screen size, and color depth will all affect the LCD performance.

3.2.7 Status Pins

The uP_STATUS_1, uP_STATUS_2, and CPLD_GPIO_1 signals are available on the J1A expansion connector and are used by Logic BSP's to indicate the device is operating.

Most baseboard designs should connect these signals to LED's that are connected through a resistor to a power rail.

Some processors allow the status signals to be used as general purpose I/O pins which can be reconfigured in customer specific software applications. Not all processors support this functionality, and in some cases the processor's status pins only indicate the current operating state of the processor.

3.2.8 AC97 and I2S CODEC

The card engine interface has dedicated pins for an AC97 CODEC interface.

Most processors only have a single AC97 interface, so it is used to drive the onboard CODEC. The AC97 signals are made available on the J1A expansion connector for flexibility in CODEC

selection. The customer can opt to not have the card engine CODEC populated and use their own CODEC on their baseboard driven by the processor's AC97 link.

Some processors have duplicate AC97 interfaces; in these cases the first AC97 link is used for the onboard CODEC and the second link is provided at the J1A expansion connector.

I2S interfaces are sometimes muxed with the processor's AC97 link and can be used by the customer through the AC97 dedicated card engine interface.

In the case of an I2S interface, the SD_IN is connected to the DATAOUT of the baseboard I2S CODEC and the SD_OUT is connected to the DATAIN of the baseboard I2S CODEC. For a baseboard AC97 CODEC, SD_OUT is connected to the CODEC DATAOUT pin; the SD_IN is connected to the CODEC DATAIN pin.

3.3 80 pin Expansion Connector J1B Signals

3.3.1 UARTB and UARTC

The 80 pin expansion connector J1B has the dedicated locations for UARTB and UARTC serial ports.

UARTB and UARTC typically are processor specific serial ports and are generally available on all processors that support three serial ports.

In some cases, there are other peripheral chips on the card engine that have serial ports that can be used as UART's. The card engine may have one of these extra serial devices at a UARTB or UARTC location if the processor does not support multiple serial ports.

Please note that the UART flow control signal implementations may vary between card engine implementations.

3.3.2 Infra-Red Serial Port

The J1B expansion connector also has two pins dedicated to an Infra Red serial port.

Most processors support IR ports and in some cases the IR port may be muxed with a UART. In muxed serial port cases, UARTB/C is mutually exclusive with the IR port.

For base boards that implement IR devices, ensure that all processors that will be used in the product support IR before relying on the IR port of a single product.

3.3.3 PCMCIA

The J1B expansion connector has signals dedicated to the card engine PCMCIA interface.

The PCMCIA interface has multiple control signals for accessing different types of PC cards. For multi-card engine designs that will be using the PCMCIA/ PC Card interface, reference the IDK kit design documentation for an example design that implements a PCMCIA / PC Card interface that is compatible with all card engine PCMCIA / PC Card enabled products.

Before designing a product based around the card engine PCMCIA interface, ensure that the desired card engines that will be targeted for the end product have PCMCIA capability.

3.3.4 Multi-Function Pins

The remaining signals on the J1B expansion connector are dedicated as Multi Function Pins or MFP's.

MFP's are signals that are not designated from a card engine level, but are based around the peripherals of the processor. The MFP signals allow Logic to maximize the feature sets of the chosen processor for a specific card engine. Different processors support different peripherals, and that is why Logic makes different card engines.

The MFP's are intelligently mapped out so that card engines with similar MFP peripherals line up exactly across multiple card engine products. This ensures that if two card engines support I2C interfaces, a customer can design a product with an I2C device and switch between the two different card engines and still be able to support the I2C device without changing any hardware.

The following is a list of some of the features that can be found on current card engine products: I2C, battery monitoring, additional serial ports, PWM signals, buzzer outputs, specific clock inputs, expanded chip selects, keypad interfaces, PS2 keyboard/mouse inputs, Smart Card Interfaces, MMC interfaces, additional LCD signals not defined in the dedicated LCD interface,

CPLD GPIO, additional CODEC inputs/outputs, additional external DMA signals, and additional USB host or client interfaces.

4 Card Engine Pin-Out Chart

The chart below presents a general card engine pin-out for Logic's card engines. *Please refer to respective card engine hardware specification, such as the "LH7A400-10 Card Engine Hardware Specification," for specific pin-out similarities and differences.*

PIN #	GROUP	SIGNAL NAME	MUX	I/O	Description
J1A.01	LCD	LCD_VSYNC		O	LCD Vsync/ Frame line marker (active state selectable) || General purpose I/O PTE3.
J1A.02	LCD	LCD_HSYNC		O	LCD Hsync/ Line clock (active state selectable) || General purpose I/O PTD5.
J1A.03	LCD	LCD_DCLK		O	LCD data clock || General purpose I/O PTH7.
J1A.04	LCD	LCD_DON		O	Active high. LCD display on signal || General purpose I/O PTD7.
J1A.05	LCD	LCD_MDISP		O	LCD current alternating signal/LCD enable signal || General purpose I/O PTE6.
J1A.06	LCD	LCD_VEEEN		O	Active high. LCD panel Vee enable.
J1A.07	LCD	LCD_VDDEN		O	Active high. LCD panel Vcc enable.
J1A.08	LCD	LCD_CLK_RETURN		I	LCD clock input signal
J1A.09	PWR	DGND		I	Digital Ground (0V)
J1A.10	LCD	LCD_CLS		O	LCD signal
J1A.11	LCD	LCD_SPS		O	LCD signal
J1A.12	LCD	LCD_PSAVE		O	LCD signal
J1A.13	LCD	LCD_SPL		O	LCD signal
J1A.14	LCD	LCD_HRLP		O	LCD signal
J1A.15	LCD	LCD_MOD		O	LCD signal
J1A.16	LCD	LCD_REV		O	LCD signal
J1A.17	DEBUG	uP_STATUS_1		O	Processor status pin. uP_STATUS_2/uP_STATUS_1 -> 0/0 = Running, 0/1= Standby, 1/0 = Sleep,
J1A.18	DEBUG	uP_STATUS_2		O	Processor status pin. uP_STATUS_2/uP_STATUS_1 -> 0/0 = Running, 0/1 = Standby, 1/0 = Sleep,
J1A.19	CODEC	uP_AC97_BITCLK0		O	AC97 Clock signal
J1A.20	CODEC	uP_AC97_nRESET		I	Active Low. AC97 reset signal
J1A.21	CODEC	uP_AC97_SYNC0		O	AC97 signal
J1A.22	CODEC	uP_AC97_SD_IN0		I	AC97 signal
J1A.23	CODEC	uP_AC97_SD_OUT0		O	AC97 signal
J1A.24	PWR	DGND		I	Digital Ground (0V)
J1A.25	AFE	A/D1		I	Analog input (pin ANx) : 0 to 3.3V swing possible.
J1A.26	AFE	A/D2		I	Analog input (pin AN4) : 0 to 3.3V swing possible.
J1A.27	PWR	AGND		I	Analog Ground (0V)
J1A.28	MFP	MFP39 (A/D4 - HP_OUTL)	Y	I || O	Analog input (pin AN7) : 0 to 3.3V swing possible || Analog output (SH7727 pin DA0)
J1A.29	MFP	MFP40 (A/D4 - HP_OUTL)		I/O	MFP bit 40
J1A.30	PWR	3.3VA		I	Analog Power Supply (3.3V)
J1A.31	CODEC	CODEC_INL		I	Left channel stereo line-in input of the audio CODEC. 1V RMS typcial, 2V RMS max (if current
J1A.32	CODEC	CODEC_INR		I	Right channel stereo line-in input of the audio CODEC. 1V RMS typcial, 2V RMS max (if current
J1A.33	CODEC	CODEC_OUTL		O	Left stereo mixer-channel line output. Nominal output level is 1.0 Vrms.
J1A.34	CODEC	CODEC_OUTR		O	Right stereo mixer-channel line output. Nominal output level is 1.0 Vrms.
J1A.35	PWR	AGND		I	Analog Ground (0V)
J1A.36	TOUCH	TOUCH_LEFT		I	Four wire resistive touch X+ position connection.(LEFT)
J1A.37	TOUCH	TOUCH_RIGHT		I	Four wire resistive touch X- position connection. (RIGHT)
J1A.38	TOUCH	TOUCH_BOTTOM		I	Four wire resistive touch Y- position connection.(BOTTOM)
J1A.39	TOUCH	TOUCH_TOP		I	Four wire resistive touch Y+ position connection. (TOP)
J1A.40	PWR	3.3VA		I	Analog Power Supply (3.3V)
J1A.41	LCD	R0		O	The LCD data bus used to transmit data to the LCD module. RED 0 - internally shorted to R5 due to
J1A.42	LCD	R1		O	The LCD data bus used to transmit data to the LCD module. RED 1
J1A.43	LCD	R2		O	The LCD data bus used to transmit data to the LCD module. RED 2.
J1A.44	PWR	DGND		I	Digital Ground (0V)
J1A.45	LCD	R3		O	The LCD data bus used to transmit data to the LCD module. RED 3.
J1A.46	LCD	R4		O	The LCD data bus used to transmit data to the LCD module. RED 4.
J1A.47	LCD	R5		O	The LCD data bus used to transmit data to the LCD module. RED 5.
J1A.48	LCD	G0		O	The LCD data bus used to transmit data to the LCD module. GREEN 0
J1A.49	LCD	G1		O	The LCD data bus used to transmit data to the LCD module. GREEN 1.
J1A.50	LCD	G2		O	The LCD data bus used to transmit data to the LCD module. GREEN 2.
J1A.51	LCD	G3		O	The LCD data bus used to transmit data to the LCD module. GREEN 3.
J1A.52	LCD	G4		O	The LCD data bus used to transmit data to the LCD module. GREEN 4
J1A.53	LCD	G5		O	The LCD data bus used to transmit data to the LCD module. GREEN 5
J1A.54	LCD	B0		O	The LCD data bus used to transmit data to the LCD module. BLUE 0 - internally shorted to B5 due to
J1A.55	PWR	DGND		I	Digital Ground (0V)
J1A.56	LCD	B1		O	The LCD data bus used to transmit data to the LCD module. BLUE 1.
J1A.57	LCD	B2		O	The LCD data bus used to transmit data to the LCD module. BLUE 2.
J1A.58	LCD	B3		O	The LCD data bus used to transmit data to the LCD module. BLUE 3.
J1A.59	LCD	B4		O	The LCD data bus used to transmit data to the LCD module. BLUE 4.
J1A.60	LCD	B5		O	The LCD data bus used to transmit data to the LCD module. BLUE 5.
J1A.61	CF	CF_nCE		O	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word
J1A.62	CF	RSVD_1			
J1A.63	GPIO	CPLD_GPIO_1		I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1A.64	GPIO	CPLD_GPIO_2		I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1A.65	USB	uP_USB2_nOVR_CRNT		I	Active low. Signals an overcurrent condition on USB host port #2.
J1A.66	PWR	DGND		I	Digital Ground (0V)
J1A.67	USB	uP_USB1_nOVR_CRNT		I	Active low. Signals an overcurrent condition when USB port #1 is configured as host. Signals cable
J1A.68	USB	uP_USB2_PWR_EN		O	Active high. Enables power supply for USB host port #2.
J1A.69	USB	uP_USB1_PWR_EN		O	Active high. Enables power supply when USB port #1 is configured as host. Enables D+ pullup (TX
J1A.70	USB	uP_USB2_M		I/O	USB port #2 data I/O minus. Route as differential pair with uP_USB2_P.
J1A.71	USB	uP_USB2_P		I/O	USB port #2 data I/O plus. Route as differential pair with uP_USB2_M.
J1A.72	USB	uP_USB1_M		I/O	USB port #1 data I/O minus. Route as differential pair with uP_USB1_P.
J1A.73	USB	uP_USB1_P		I/O	USB port #1 data I/O plus. Route as differential pair with uP_USB1_M.
J1A.74	BUS	BUFF_nOE		I/O	Active low. Controls the outputs of the buffers on the card engine. When low, the buffers are active,
J1A.75	BUS	BUFF_DIR_ADDRESS		O	Active high/low. Controls the direction of the address lines through the buffers. When low, the
J1A.76	BUS	BUFF_DIR_DATA		I/O	Active high/low. Controls the direction of the data lines through the buffers. When low, the data lines
J1A.77	PWR	DGND		I	Digital Ground (0V)
J1A.78	CODEC	MIC_IN		I	Microphone input
J1A.79	OTHER	POWER_SENSE1		I	These two pins are used to set the core voltage of the card engine. For use with Logic Application
J1A.80	OTHER	POWER_SENSE2		I	These two pins are used to set the core voltage of the card engine. For use with Logic Application

J1B.01	DEBUG	CPLD_TCK		I	This is the test clock input for the CPLD JTAG port.
J1B.02	DEBUG	CPLD_TDO		O	This input transmits data out of the CPLD JTAG port.
J1B.03	DEBUG	CPLD_TMS		O	This input indicates the mode of CPLD JTAG port.
J1B.04	DEBUG	CPLD_TDI		I	This input receives data on the CPLD JTAB port.
J1B.05	PCMCIA	uP_PCC_nOE	Y	O	Active low. This bufferred signal is the read strobe that latches data output from external peripherals.
J1B.06	PCMCIA	uP_PCC_nWE	Y	O	Active low. Bufferred write enable for buffered data bus bits 15->8 - PCMCIA WE - DQM1
J1B.07	PCMCIA	uP_PCC_nIORD	Y	O	Active low. Buffered write enable for buffered data bus bits 23->16 - PCMCIA IORD - DQM2
J1B.08	PCMCIA	uP_PCC_nIOWR	Y	O	Active low. Buffered write enable for buffered data bus bits 31->24 - PCMCIA IOWR - DQM3
J1B.09	PWR	DGND		I	Digital Ground (0V)
J1B.10	PCMCIA	uP_PCC_RESET	Y	O	DMA channel 0 external request acknowledge (active state selectable) || Active high. PCMCIA reset.
J1B.11	PCMCIA	uP_PCC_nCE1B		O	Active low. Chip/card enable signal for PCMCIA area 6 accesses signifying data bits 0..7 are valid.
J1B.12	PCMCIA	uP_PCC_nCE2B		O	Active low. Chip/card enable signal for PCMCIA area 6 accesses signifying data bits 15..8 are valid.
J1B.13	PCMCIA	uP_PCC_nIOIS16		I	Active low. PCMCIA IOIS16 signal. When low, specifies 16 bit IO card or write protected memory
J1B.14	PCMCIA	uP_PCC_RDY		I	Active high. PCMCIA RDY signal. PCMCIA/CF card will hold this signal low until ready to be
J1B.15	PCMCIA	uP_PCC_nWAIT		I	Active low. PCMCIA WAIT signal. Has same effect of holding the current bus cycle that uP_WAIT#
J1B.16	PCMCIA	uP_PCC_BVD2		I	PCMCIA BVD2 signal.
J1B.17	PCMCIA	uP_PCC_BVD1		I	PCMCIA BVD1 singal.
J1B.18	PCMCIA	uP_PCC_nCD2		I	Active low. PCMCIA CD2 signal. Signals that one side of the PCMCIA/CF card is connected.
J1B.19	PCMCIA	uP_PCC_nCD1		I	Active low. PCMCIA CD1 signal. Signals that one side of the PCMCIA/CF card is connected.
J1B.20	PCMCIA	uP_PCC_nREG		O	Active low. PCMCIA REG signal. When asserted, this signal specifies accesses to card attribute
J1B.21	PWR	DGND		I	Digital Ground (0V)
J1B.22	PCMCIA	uP_PCC_VS1		I	PCMCIA VS1 signal. Voltage sense.
J1B.23	PCMCIA	uP_PCC_VS2		I	PCMCIA VS2 signal. Voltage sense.
J1B.24	PCMCIA	uP_PCC_nDRV	Y	O	DMA channel 0 acknowledge (active state selectable) || Active low. PCMCIA drive enable (can use
J1B.25	PCMCIA	uP_PCC_DIR		O	PCMCIA Data Direction
J1B.26	SDRAM	uP_nDQM3	Y	O	Active low. Buffered write enable for buffered data bus bits 31->24 - PCMCIA IOWR - DQM3
J1B.27	SDRAM	uP_nDQM2	Y	O	Active low. Buffered write enable for buffered data bus bits 23->16 - PCMCIA IORD - DQM2
J1B.28	SDRAM	uP_nDQM1	Y	O	Active low. Bufferred write enable for buffered data bus bits 15->8 - PCMCIA WE - DQM1
J1B.29	SDRAM	uP_nDQM0	Y	O	Active low. Buffered write enable for buffered data bus bits 7->0 - DQM0 SDRAM signal from the
J1B.30	IRDA	uP_IRTX		O	IRDA Transmit data
J1B.31	IRDA	uP_IRRX		I	IRDA Receive data
J1B.32	PWR	DGND		I	Digital Ground (0V)
J1B.33	MFP	MFP1		I/O	MFP bit 1
J1B.34	MFP	MFP2		I/O	MFP bit 2
J1B.35	MFP	MFP3		I/O	MFP bit 3
J1B.36	MFP	MFP4		I/O	MFP bit 4
J1B.37	MFP	MFP5		I/O	MFP bit 5
J1B.38	MFP	MFP6		I/O	MFP bit 6
J1B.39	MFP	MFP7		I/O	MFP bit 7
J1B.40	MFP	MFP8		I/O	MFP bit 8
J1B.41	UART	uP_UARTB_TX		O	UARTB Transmit data
J1B.42	UART	uP_UARTB_RX		I	UARTB Receive data
J1B.43	UART	uP_UARTB_CTS		I	UARTB Clear to Send
J1B.44	PWR	DGND		I	Digital Ground (0V)
J1B.45	UART	uP_UARTB_DSR		O	UARTB Data Set Ready
J1B.46	UART	uP_UARTC_TX		O	UARTC Transmit data
J1B.47	UART	uP_UARTC_RX		I	UARTC Receive data
J1B.48	MFP	MFP9	Y	O	MFP bit 9
J1B.49	MFP	MFP10	Y	I	MFP bit 10
J1B.50	MFP	MFP11	Y	I	MFP bit 11
J1B.51	MFP	MFP12	Y	I || I	MFP bit 12
J1B.52	MFP	MFP13	Y	I	MFP bit 13
J1B.53	MFP	MFP14	Y	O	MFP bit 14
J1B.54	MFP	MFP15	Y	O	MFP bit 15
J1B.56	MFP	MFP16	Y	I	MFP bit 16
J1B.57	MFP	MFP17		I/O	MFP bit 17
J1B.58	MFP	MFP18	Y	O	SIOF serial transmit data. This signal is attached to the on-board CODEC, but may be used to
J1B.59	MFP	MFP19	Y	I	SIOF serial receive data. This signal is attached to the on-board CODEC, but may be used to
J1B.60	MFP	MFP20	Y	I/O	SIOF serial frame sync signal. This signal is output in master mode and input in slave mode. This
J1B.61	MFP	MFP21	Y	I/O	SIOF serial communications clock. This signal is output in master mode and input in slave mode.
J1B.62	MFP	MFP22	Y	I/O	This signal is the master CODEC clock frequency and is typically output from the card engine. If the
J1B.63	MFP	MFP23	Y	O || I	Active high. Signals that the output of the CODEC is within 1dB of the rails. || If the on-board
J1B.65	MFP	MFP25	Y	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1B.66	PWR	DGND		I	Digital Ground (0V)
J1B.67	MFP	MFP26	Y	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1B.68	MFP	MFP27	Y	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1B.69	MFP	MFP28	Y	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1B.70	MFP	MFP29	Y	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1B.71	MFP	MFP30	Y	I/O	Active low. Chip/card enable signal for PCMCIA area 5 accesses signifying data bits 15..8 are valid.
J1B.72	MFP	MFP31	Y	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD.
J1B.73	MFP	MFP32		I/O	MFP bit 32
J1B.74	MFP	MFP33		I/O	MFP bit 33
J1B.75	MFP	MFP34		I/O	MFP bit 34
J1B.76	MFP	MFP35		I/O	MFP bit 35
J1B.77	PWR	DGND		I	Digital Ground (0V)
J1B.78	MFP	MFP36		I/O	MFP bit 36
J1B.79	MFP	MFP37		I/O	MFP bit 37
J1B.80	MFP	MFP38		I/O	MFP bit 38

J1C.001	ETH	ETHER_RX(-)		I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive
J1C.002	RESET	MSTR_nRST		I/O	Active Low. This signal initiates a hard reset (power on) – external memory contents are lost during
J1C.003	ETH	ETHER_RX(+)		I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive
J1C.004	RESET	uP_SW_nRESET		I	Active Low. This signal initiates a soft reset (manual reset) – external memory contents are retained
J1C.005	ETH	ETHER_TX(-)		O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines.
J1C.006	CS	FAST_nMCS		O	Active Low. Buffered chip select for area 4 of SH7727-20 memory. This is the "fast" peripheral chip
J1C.007	ETH	ETHER_TX(+)		O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines.
J1C.008	CS	SLOW_nMCS		O	Active Low. Buffered chip select for area 5 of SH7727-20 memory. This is the "slow" peripheral chip
J1C.009	PWR	DGND		I	Digital Ground (0V)
J1C.010	CS	VIDEO_nMCS		O	Active Low. Buffered chip select for area 2 of SH7727-20 memory. This is the "video" chip select
J1C.011	ETH	ETHER_nACT_LED		O	Active Low open drain output. 24mA sink. This output indicates transmission or reception of frames
J1C.012	CS	BOOT_nMCS		O	Active Low. This signal is the buffered chip select for boot ROM and is connected to area 0 of
J1C.013	ETH	ETHER_nLNK_LED		O	Active Low open drain output. 24mA sink. This output indicates valid link pulses. May be connected
J1C.014	BUS	nIOWR		O	Active Low. This signal is driven by the ISA bus master or DMA controller to signal valid write data
J1C.015	RESET	nSTANDBY		I	Active Low. CPU power mode signal. When low during an NMI interrupt, Card Engine will enter
J1C.016	BUS	nIORD		O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O
J1C.017	PWR	DGND		I	Digital Ground (0V)
J1C.018	PWR	3.3V_WRLAN		O	Power Supply (3.3V) from the 10/100 wired LAN circuit. This pin is used to power the impedance
J1C.019	PWR	VDD3.3V		I	Power Supply (3.3V)
J1C.020	BUS	BALE		O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid.
J1C.021	IRQ	uP_NMI		I	Active Low. The non-maskable interrupt – highest priority - for the CPU. Used to signal power
J1C.022	BUS	nCHRDY		I	Active Low. The I/O channel ready signal line allows the resources to indicate to the ISA bus master
J1C.023	IRQ	uP_IRQD		I	Active Low. Port interrupt on SH7727-20 (SH7727 pin PINT11). May also be configured as a general
J1C.024	OTHER	uP_TEST1		I	Reserved for Production Test. Leave unconnected or tie high for normal operation. This is the
J1C.025	IRQ	uP_IRQC		I	Active Low. Dedicated hardware interrupt on SH7727-20 (SH7727 pin IRQ4). May also be
J1C.026	OTHER	uP_TEST2		I	Reserved for Production Test. Leave unconnected.
J1C.027	IRQ	uP_IRQB		I	Active Low. Dedicated hardware interrupt on SH7727-20 (SH7727 pin IRQ3). May also be
J1C.028	DEBUG	uP_TRST		I	JTAG Test Reset Input. May leave unconnected if not using the JTAG port.
J1C.029	IRQ	uP_IRQA		I	Active Low. Dedicated hardware interrupt on SH7727-20 (SH7727 pin IRQ0). May also be
J1C.030	DEBUG	uP_TMS		I	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port.
J1C.031	BUS	uP_nBS		O	Active Low. This buffered signal signifies the start of an external bus cycle from the processor.
J1C.032	DEBUG	uP_TDO		O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use.
J1C.033	BUS	uP_nBACK		O	Active Low. Acknowledge signal in response to uP_BREQ signifying that CPU is releasing bus
J1C.034	DEBUG	uP_TDI		I	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port.
J1C.035	BUS	uP_nBREQ		I	Active Low. Request for CPU to release bus control.
J1C.036	DEBUG	uP_TCK		I	JTAG Test Clock Input. May leave unconnected if not using the JTAG port.
J1C.037	BUS	uP_nWAIT		I	Active low. The WAIT signal requests the current bus cycle be extended until this signal is de-
J1C.038	CONFIG	uP_MODE3		I	Boot select signal (0 = external boot device, 1 = onboard flash). This defaults to high (onboard flash)
J1C.039	UART	uP_UARTA_RTS		O	Active low. Request to send for SCIF port (UARTA).
J1C.040	CONFIG	uP_MODE2		I	Endian setting (0 = big endian, 1 = little endian). This defaults to high (little endian) if left
J1C.041	UART	uP_UARTA_CTS		I	Active low. Clear to send for SCIF port (UARTA).
J1C.042	CONFIG	uP_MODE1		I	Bus width setting. uP_MODE1/uP_MODE0 - 0/0 = INVALID , 0/1 = 8 bit, 1/0 = 16 bit, 1/1 = 32 bit.
J1C.043	UART	uP_UARTA_TX		O	SCIF port (UARTA) transmit data output.
J1C.044	CONFIG	uP_MODE0		I	Bus width setting. uP_MODE1/uP_MODE0 - 0/0 = INVALID , 0/1 = 8 bit, 1/0 = 16 bit, 1/1 = 32 bit.
J1C.045	UART	uP_UARTA_RX		I	SCIF port (UARTA) receive data input.
J1C.046	DMA	uP_DREQ1		I	DMA Channel 1 Request
J1C.047	UART	uP_UARTA_DTR		I	UARTA Data Terminal Ready Signal
J1C.048	DMA	uP_DREQ0		I	Active low. DMA channel 0 external request (low level or falling edge selectable). This may also be
J1C.049	UART	uP_UARTA_DSR		O	UARTA Data Set Ready Signal
J1C.050	DMA	uP_DRAK1		I	DMA channel 1 external request acknowledge (active state selectable)
J1C.051	RESET	nSUSPEND		I	Active low. CPU power mode signal. When low during an NMI interrupt, Card Engine will enter
J1C.052	PCMCIA	uP_DRAK0	Y	O	DMA channel 0 external request acknowledge (active state selectable) || Active high. PCMCIA reset.
J1C.053	CLK	uP_AUX_CLK		O	This auxiliary clock is controlled in the CPU and can be used by the peripherals. It is the same
J1C.054	DMA	uP_DACK1		O	DMA channel 1 acknowledge (active state selectable)
J1C.055	PWR	DGND		I	Digital Ground (0V)
J1C.056	DMA	uP_DACK0	Y	O	DMA channel 0 acknowledge (active state selectable)
J1C.056	PCMCIA	uP_PCC_nDRV	Y	O	Active low. PCMCIA drive enable.
J1C.057	PWR	VCORE		I	CPU core voltage supply (on during low power, SW_Reset).
J1C.058	PWR	VCORE		I	CPU core voltage supply (on during low power, SW_Reset).
J1C.059	PWR	VCORE		I	CPU core voltage supply (on during low power, SW_Reset).
J1C.060	PWR	VCORE		I	CPU core voltage supply (on during low power, SW_Reset).
J1C.061	SDRAM	3.3V_uP_SDRAM		I	uP and SDRAM Power Supply (3.3 V) (on during low power, SW_Reset). Recommend leaving this
J1C.062	SDRAM	3.3V_uP_SDRAM		I	uP and SDRAM Power Supply (3.3 V) (on during low power,SW_Reset). Recommend leaving this
J1C.063	SDRAM	3.3V_uP_SDRAM		I	uP and SDRAM Power Supply (3.3 V) (on during low power, SW_Reset). Recommend leaving this
J1C.064	SDRAM	3.3V_uP_SDRAM		I	uP and SDRAM Power Supply (3.3 V) (on during low power, SW_Reset). Recommend leaving this
J1C.065	SPI	uP_SPI_FRM		O	Software controlled SPI framing signal. This signal may be used by application software to frame SPI
J1C.066	CLK	uP_BUS_CLK		O	Bus clock. Operates at 51.6MHz. Do not connect to any loads unless first buffered for extended
J1C.067	SPI	uP_SPI_MOSI_TX		O	This output transmits synchronous SPI data.
J1C.068	PWR	DGND		I	Digital Ground (0V)
J1C.069	SPI	uP_SPI_MISO_RX		I	This input receives synchronous SPI data.
J1C.070	SDRAM	uP_nRAS		O	Active low. This signal is sent to a random access memory to tell that an associated address is a row
J1C.071	SPI	uP_SPI_SCK		O	SPI clock signal. SPI transmit/receive data is valid on the rising edge of this clock (data is output
J1C.072	SDRAM	uP_nCAS		O	Active low. This signal is sent to a random access memory to tell that an associated address is a
J1C.073	DATA	uP_MD00		I/O	Buffered Data Bus bit 0.
J1C.074	BUS	uP_nMWE3	Y	O	Active low. Buffered write enable for buffered data bus bits 31->24 - PCMCIA IOWR - DQM3
J1C.075	DATA	uP_MD01		I/O	Buffered Data Bus bit 1.
J1C.076	BUS	uP_nMWE2	Y	O	Active low. Buffered write enable for buffered data bus bits 23->16 - PCMCIA IORD - DQM2
J1C.077	DATA	uP_MD02		I/O	Buffered Data Bus bit 2.
J1C.078	BUS	uP_nMWE1	Y	O	Active low. Buffered write enable for buffered data bus bits 15->8 - PCMCIA WE - DQM1 SDRAM
J1C.079	DATA	uP_MD03		I/O	Buffered Data Bus bit 3.
J1C.080	BUS	uP_nMWE0	Y	O	Active low. Buffered write enable for buffered data bus bits 7->0 - DQM0 SDRAM signal from the

J1C.081	DATA	uP_MD04		I/O	Buffered Data Bus bit 4.
J1C.082	BUS	uP_nMWR		O	Active low. When low, this bufferred signal signifies a write cycle on the bus. When high, this signal
J1C.083	DATA	uP_MD05		I/O	Buffered Data Bus bit 5.
J1C.084	BUS	uP_nMRD	Y	O	Active low. This buffered signal is the read strobe that latches data output from external peripherals.
J1C.085	DATA	uP_MD06		I/O	Buffered Data Bus bit 6.
J1C.086	ADDR	uP_A26		O	Buffered Address Bus bit 26
J1C.087	DATA	uP_MD07		I/O	Buffered Data Bus bit 7.
J1C.088	ADDR	uP_A27		O	Buffered Address Bus bit 27
J1C.089	PWR	DGND		I	Digital Ground (0V)
J1C.090	ADDR	uP_MA00		I/O	Buffered Address Bus bit 0.
J1C.091	DATA	uP_MD08		I/O	Buffered Data Bus bit 8.
J1C.092	ADDR	uP_MA01		I/O	Buffered Address Bus bit 1.
J1C.093	DATA	uP_MD09		I/O	Buffered Data Bus bit 9.
J1C.094	ADDR	uP_MA02		I/O	Buffered Address Bus bit 2.
J1C.095	DATA	uP_MD10		I/O	Buffered Data Bus bit 10.
J1C.096	ADDR	uP_MA03		I/O	Buffered Address Bus bit 3.
J1C.097	DATA	uP_MD11		I/O	Buffered Data Bus bit 11.
J1C.098	ADDR	uP_MA04		I/O	Buffered Address Bus bit 4.
J1C.099	DATA	uP_MD12		I/O	Buffered Data Bus bit 12.
J1C.100	ADDR	uP_MA05		I/O	Buffered Address Bus bit 5.
J1C.101	DATA	uP_MD13		I/O	Buffered Data Bus bit 13.
J1C.102	ADDR	uP_MA06		I/O	Buffered Address Bus bit 6.
J1C.103	DATA	uP_MD14		I/O	Buffered Data Bus bit 14.
J1C.104	ADDR	uP_MA07		I/O	Buffered Address Bus bit 7.
J1C.105	DATA	uP_MD15		I/O	Buffered Data Bus bit 15.
J1C.106	ADDR	uP_MA08		I/O	Buffered Address Bus bit 8.
J1C.107	PWR	VDD3.3V		I	Power Supply (3.3V)
J1C.108	ADDR	uP_MA09		I/O	Buffered Address Bus bit 9.
J1C.109	PWR	DGND		I	Digital Ground (0V)
J1C.110	ADDR	uP_MA10		I/O	Buffered Address Bus bit 10.
J1C.111	DATA	uP_MD16		I/O	Buffered Data Bus bit 16.
J1C.112	ADDR	uP_MA11		I/O	Buffered Address Bus bit 11.
J1C.113	DATA	uP_MD17		I/O	Buffered Data Bus bit 17.
J1C.114	ADDR	uP_MA12		I/O	Buffered Address Bus bit 12.
J1C.115	DATA	uP_MD18		I/O	Buffered Data Bus bit 18.
J1C.116	ADDR	uP_MA13		I/O	Buffered Address Bus bit 13.
J1C.117	DATA	uP_MD19		I/O	Buffered Data Bus bit 19.
J1C.118	ADDR	uP_MA14		I/O	Buffered Address Bus bit 14.
J1C.119	DATA	uP_MD20		I/O	Buffered Data Bus bit 20.
J1C.120	ADDR	uP_MA15		I/O	Buffered Address Bus bit 15.
J1C.121	DATA	uP_MD21		I/O	Buffered Data Bus bit 21.
J1C.122	ADDR	uP_MA16		I/O	Buffered Address Bus bit 16.
J1C.123	DATA	uP_MD22		I/O	Buffered Data Bus bit 22.
J1C.124	ADDR	uP_MA17		I/O	Buffered Address Bus bit 17.
J1C.125	DATA	uP_MD23		I/O	Buffered Data Bus bit 23.
J1C.126	ADDR	uP_MA18		I/O	Buffered Address Bus bit 18.
J1C.127	PWR	DGND		I	Digital Ground (0V)
J1C.128	ADDR	uP_MA19		I/O	Buffered Address Bus bit 19.
J1C.129	DATA	uP_MD24		I/O	Buffered Data Bus bit 24.
J1C.130	ADDR	uP_MA20		I/O	Buffered Address Bus bit 20.
J1C.131	DATA	uP_MD25		I/O	Buffered Data Bus bit 25.
J1C.132	ADDR	uP_MA21		I/O	Buffered Address Bus bit 21.
J1C.133	DATA	uP_MD26		I/O	Buffered Data Bus bit 26.
J1C.134	ADDR	uP_MA22		I/O	Buffered Address Bus bit 22.
J1C.135	DATA	uP_MD27		I/O	Buffered Data Bus bit 27.
J1C.136	ADDR	uP_MA23		I/O	Buffered Address Bus bit 23.
J1C.137	DATA	uP_MD28		I/O	Buffered Data Bus bit 28.
J1C.138	ADDR	uP_MA24		I/O	Buffered Address Bus bit 24.
J1C.139	DATA	uP_MD29		I/O	Buffered Data Bus bit 29.
J1C.140	ADDR	uP_MA25		I/O	Buffered Address Bus bit 25.
J1C.141	DATA	uP_MD30		I/O	Buffered Data Bus bit 30.
J1C.142	BUS	nAEN		O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
J1C.143	DATA	uP_MD31		I/O	Buffered Data Bus bit 31.
J1C.144	PWR	VDD3.3V		I	Power Supply (3.3V)