PXA270-10 Power Application Note

Application Note 281

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Abstract

The PXA270 processor provides many opportunities for system-level power savings. This application note describes and compares recommended power supply design scenarios for the PXA270-10 Card Engine module.

REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	Kurt Larson	Release	HAR	1/13/2006
B	Michael Aanenson	-Updated Section 3 for proper 3.3V power plane use for external devices. This change is a reflection of the update to the PXA270 Card Engine HW Specification (PN 1001624 Rev F) and the update to the Zoom SDK Baseboard Schematic (PN 80000116 Revision J). Also see PXA270 Card Engine PCN 327 for more information. -Updated MSTR_nRST summary in Section 4 -Updated number of fixed voltages from two to three	MAA	5/22/06

1 Introduction

This document summarizes how power management is handled on the PXA270-10 Card Engine and outlines methods for implementing power management schemes for various custom applications.

2 PXA270 Power Plane Diversity

The Intel PXA270 processor is noted for its extensive power management capabilities. The number of independent power supplies that must be controlled increases the difficulty of working with the processor. The PXA270 has ten independent power supply groups, which allows its use in a wide range of applications dependant on fixed voltage interface requirements. The processor allows fixing the memory bus, liquid crystal display (LCD) bus, general purpose input/output (GPIO) pins, baseband pins, and USIM pins at different voltages to allow for different types of applications. The other power pins require fixed sources or, as in the case of VCORE, can be changed dynamically at runtime.

The Logic Product Development PXA270-10 Card Engine simplifies customer designs by implementing a single power scenario onboard the Card Engine that reduces the customer's design decisions to three basic product paths based on the product's power requirements.

The PXA270-10 Card Engine reduces the power voltage inputs from ten on the PXA270 to five on the Card Engine interface. Depending on the application, the inputs can be reduced to only three separate voltages that the customer must provide on their product. Each Card Engine power source will be discussed in more detail later in this document.

VCORE:	The VCORE power source can dynamically control voltage that directly drives the PXA270's CORE circuitry.
3.3V_IN:	The 3.3V_IN power source is the main power source for all onboard devices including the PXA270, Ethernet chip, touch chip, audio codec, NOR flash, NAND flash, and onboard power circuitry. This should be used for powering off-board devices connected directly to the Card Engine.
3.3VA_IN:	This signal is similar to 3.3V_IN, but it only supplies power to the analog portion of the onboard codec and touch chip.
3.3V_uP_SDRAM:	The 3.3V_uP_SDRAM signal provides power to the onboard SDRAM chips and should be maintained at all times in order to retain SDRAM data.
3.3V_uP_BATT:	The 3.3V_uP_BATT signal maintains the processor's real-time clock (RTC) contents and power controller states.

3 Recommended Power Management Paths

Most PXA270-10 Card Engine-based products fit into one of three main categories. Each category increases the design complexity and software support requirements of the product, which the Logic Product Development team can help with.

3.1 Minimal Requirements for Power Management

Products with minimal power restrictions belong to this group. The end product typically is connected directly to the power grid through an AC power cord and does not run on batteries for an extended period of time. The product may require only a few operating states, such as On and Off.

If your product fits into this group, the required baseboard design is relatively simple. The baseboard only needs to provide 3.3V, a switched 3.3V for external devices, and a fixed VCORE value to the Card Engine. The Starter Development Kit (SDK) baseboard that ships with the development kit is one example of how to power the Card Engine with the three fixed voltages. Figure 3.1 below graphically shows the power supply implementation of the SDK baseboard.

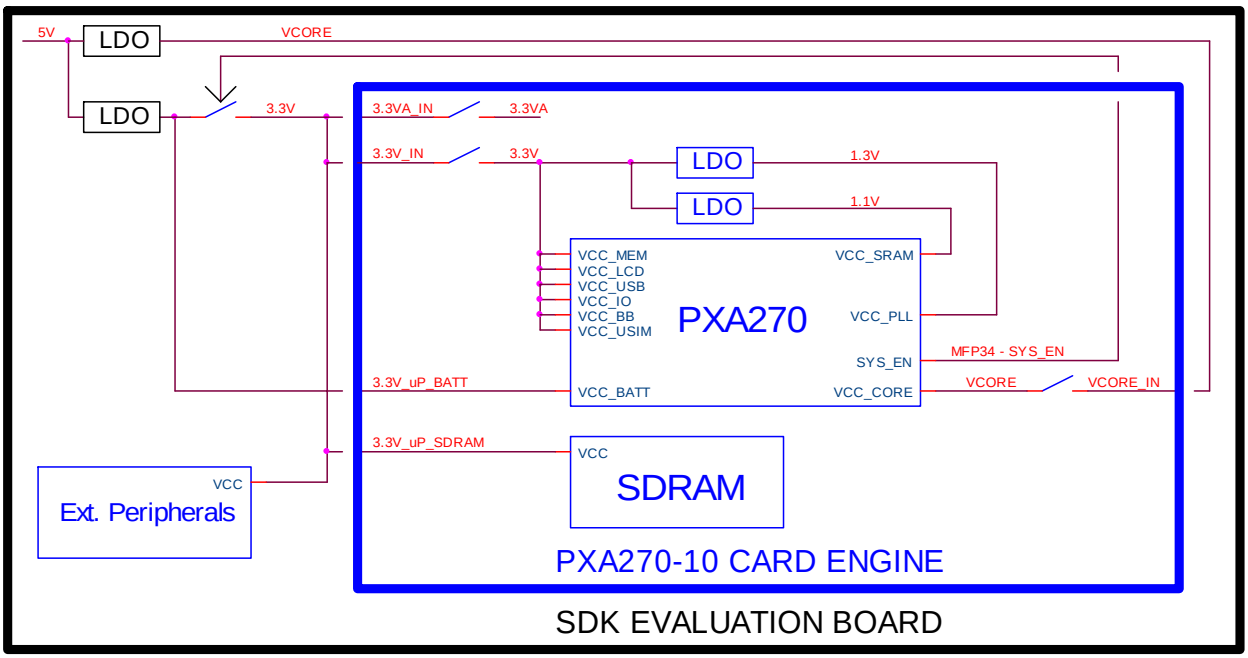

Figure 3.1: SDK Power Supply Implementation

The SDK baseboard is powered through a wall adapter that supplies the kit with a regulated 5V. The SDK baseboard uses two inexpensive Linear Drop Out (LDO) regulators to adjust the voltage from 5V to 3.3V and from 5V to the VCORE voltage for the PXA270. Since the SDK baseboard has several peripherals, including the Memory-Mapped CompactFlash interface, the 3.3V power plane must be split and controlled by the MFP34 – SYS_EN signal. This can be done with a simple P-FET and inverted MFP34 – SYS_EN signal. The 3.3V_uP_BATT signal must have 3.3V connected right away and the devices external to the Card Engine must be powered when the SYS_EN signal from the processor becomes active.

This is the simplest way to power the PXA270-10 Card Engine.

Pros: Simple to design and debug.
Low cost.
Less electrical noise when compared to switching supplies.

Cons: Least efficient method to reduce line voltage.
Not recommended for battery powered designs.
Power dissipated in the form of heat in the baseboard printed circuit board (PCB).
Only supports On/Off power states.

3.2 Medium Requirements for Power Management

Products that depend mainly on a portable power source belong in this group. Portable products typically use one (or more) of: Nickel Cadmium, Nickel Metal Hydride, Lithium Ion, Lithium Polymer, or consumer grade battery products as their main power source. They may be plugged-in to recharge the batteries or occasionally rely on alternate power sources, but using minimal power is the goal. The product may support multiple modes of operation to reduce total power consumption. Some common power states are On, Suspend, Standby, and Off.

For products in this category, the baseboard hardware design will be slightly more complex depending on the number of power states the product must support, as well as how much power is conserved in each power state. The baseboard will need to supply power to the Card Engine, as well as remove power from some power pins on the Card Engine to support further reduced power states.

The Card Engine still requires 3.3V applied to the 3.3V_IN, 3.3VA_IN, and 3.3V_uP_SDRAM terminals. A more efficient option than using LDO supplies is to use high efficiency switching regulators. Switching regulators can dynamically compensate for changing loads, which reduces overall regulator power consumption on the baseboard.

Pros: Less power lost in the form of heat.
Less heat transferred to PCB.
Longer battery life.
Greater control over power.

Cons: Strict routing requirements to minimize electrical noise.
More components on Bill of Materials (BOM).
Parts require larger surface area on PCB than LDO regulators.
More difficult design and debug.
Costs more than LDO option.
Only supports On/Off power states.

The 3.3V_uP_BATT signal powers the PXA270 internal power controller and RTC functions. Typically, this signal is powered with a coin-style battery that is diode OR'd with the main 3.3V power source so if the main power source fails, the RTC and processor power states are maintained by the backup battery.

Figure 3.2 shows a typical block diagram for a battery-powered device. The product's main power source is a discrete battery pack. The pack can be recharged by an external power source through a charge control circuit. The battery output is regulated by two different switchers in order to create the VCORE and 3.3V supplies the Card Engine requires. The 3.3V_uP_BATT signal is also backed up with a 3.3V coin style battery to maintain RTC data when the main battery or power source fails.

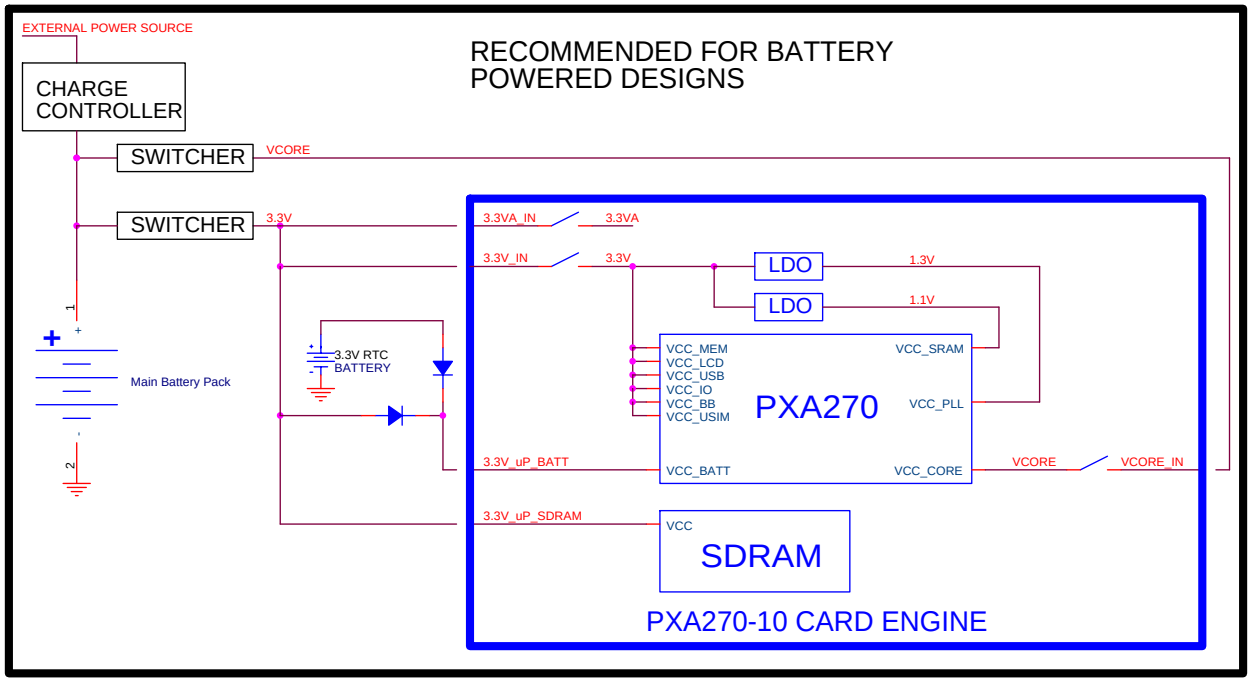

Figure 3.2: Typical Block Diagram for Battery Powered Device

A product designed like the diagram shown in Figure 3.2 will work well for most typical power consumption requirements including On, Standby, Suspend, and Off power states. Users that want additional power savings can use outputs from the Card Engine and PXA270 processor to further control their baseboard power circuitry. The two outputs that are easily implemented are the PWR_EN (net name MFP33 - PWR_EN) and SYS_EN (net name MFP32 – SYS_EN). The PWR_EN signal when high indicates the VCORE power should be applied. The SYS_EN signal when high indicates the 3.3V power supply should be turned on. These signals indicate when the PXA270 wants power supplies turned on or off before it transitions to a new power state. Either output when high indicates the particular power supply should be turned on. When either output is low, the corresponding power supply should be turned off for maximal power savings. Most Switching regulators have an Enable/Disable input that can be used with the PWR_EN and SYS_EN signals to easily control when each supply should be sequenced. The PXA270 has a fixed time during which the supplies must be turned on and stabilized for proper operation. Please refer to the “Intel® PXA270 Processor Electrical, Mechanical and Thermal Specification Data Sheet” for timing requirements and additional information on the PWR_EN and SYS_EN signals. Figure 3.3 shows a typical application of using PWR_EN and SYS_EN to control the switching regulators.

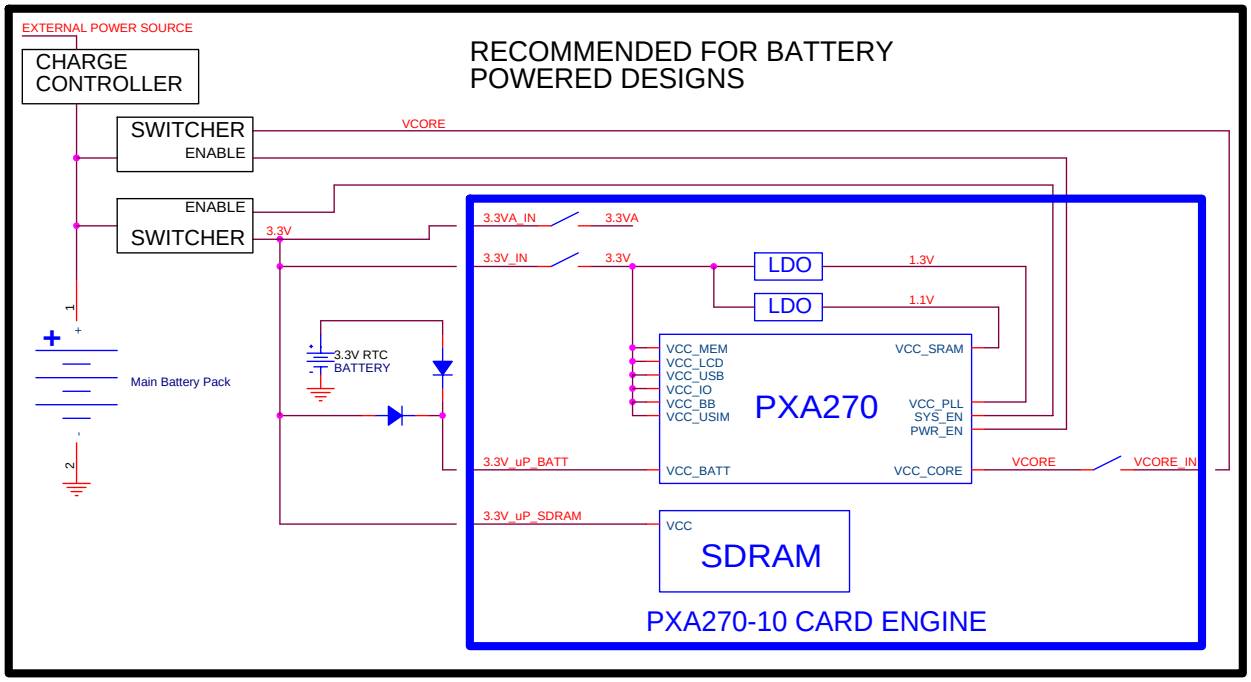

Figure 3.3: Using PWR_EN and SYS_EN to Control Switching Regulator

The only time the SYS_EN signal will go low is at power on and when the PXA270 processor transitions to the Deep Sleep state. In some designs it may be necessary to maintain the SDRAM contents in the Deep Sleep state, so the 3.3V_uP_SDRAM signal must remain powered. There are multiple solutions to this problem; a few are listed below as suggestions:

- Do not power down the 3.3V power supply when SYS_EN goes low. The Card Engine turns off power to the 3.3V_IN and 3.3VA_IN nets when SYS_EN goes low, so the external power supply would only be supplying power to the 3.3V_uP_BATT and 3.3V_uP_SDRAM power planes.

- Diode OR the 3.3V supply and the backup battery to the 3.3V_uP_SDRAM net. The SDRAM chips draw about 3–6mA each when in Self Refresh mode, which is minimal draw on the backup battery and may be acceptable in some designs.

Note: The three LDOs that are used on the Card Engine are also powered down based on the SYS_EN and PWR_EN signals to minimize onboard power consumption in all power states.

3.3 Numerous Requirements for Power Management

Products that depend solely on a portable power source belong in this group. These products typically use one (or more) of: Nickel Cadmium, Nickel Metal Hydride, Lithium Ion, Lithium Polymer, or consumer grade battery products as their main power source. They may be plugged in to recharge the batteries or occasionally rely on alternate power sources, but using minimal power is a requirement. The product may support multiple modes of operation to reduce total power consumption. Some common power states are On, Suspend, Standby, and Off, but may include more to reduce power consumption further.

For products in this category, the baseboard hardware design will be the most complex depending on the number of power states the product must support as well as how much power is conserved in each power state. The baseboard will need to supply power to the Card Engine, as well as remove power from some power pins on the Card Engine to support further reduced power states.

Products in this category will utilize an external power management integrated circuit (IC) that uses the PXA270 power management inter-integrated circuit (I2C) port to throttle the VCORE voltage applied to the processor as the operating frequency changes. As the CPU activity increases, the VCORE voltage can be raised followed by the CPU operating frequency to quickly complete the operations. As the CPU activity decreases, the operating frequency can be reduced followed by reducing VCORE voltage to conserve overall power consumption.

Users must ensure that the software being used on the Card Engine supports the required power states and drivers required to use with the external I2C controlled power supply. By default, Logic's Board Support Packages (BSPs) may not throttle CPU frequency or VCORE voltage external ICs. If the product is going to use these BSPs, please contact the Logic Product Development sales team for the latest information regarding supported, externally controllable, power management devices.

There are multiple ICs available that have various features to select for various design goals. Below are a few devices that could be used with the PXA270 for VCORE dynamic regulation and better power management control than the suggested solutions listed in Section 3.2.

National	LP3970
Linear Tech	LTC3445
Linear Tech	LTC3447

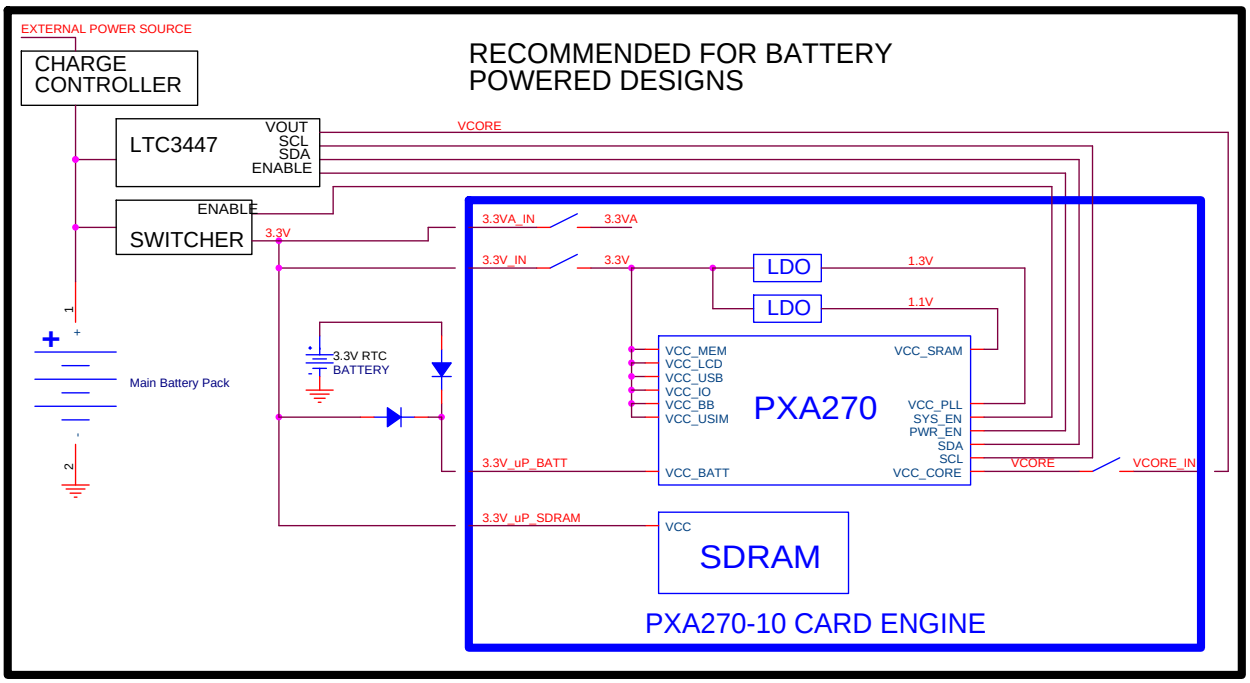

Figure 3.4: Using IC Devices to Control Switching Regulation

Pros: Least power lost in the form of heat.
Less heat transferred to PCB.
Longer battery life.
Greatest control over power.

Cons: Strict routing requirements to minimize electrical noise.
Most components on BOM.
More difficult design and debug.
Requires software development to support many power states.
Most costly baseboard IC solution.

4 Power Transition Inputs

The PXA270-10 Card Engine supports various external, power-transitioning signals. This section summarizes each.

MSTR_nRST – This signal acts as the main reset to the entire product. If this signal is asserted low, the CPU resets including the RTC count and power state controller. All 3.3V and VCORE power will be removed from the CPU except 3.3V_uP_BATT. This signal is typically implemented as a pin-hole style reset on an end product. When the processor receives the MSTR_nRST transition, it will send a reset out of nRESET. This signal is labeled as uP_nRESET_OUT on the Card Engine. The uP_nRESET_OUT signal should be used to reset all external devices to meet proper power sequence design.

nSUSPEND – When implemented in software, this signal will cause the CPU to enter the Sleep state. CPU context will be lost. Return to RUN state requires an assertion of uP_nWAKEUP/nRESET or MSTR_nRST. The program counter restarts at the reset vector. VCC_CORE, VCC_PLL, and VCC_SRAM are disabled by the PWR_EN output while in this state.

nSTANDBY – When implemented in software this signal will cause the CPU to enter the Deep Idle state. CPU context will be lost. Return to RUN state requires an assertion of uP_nWAKEUP/nRESET or MSTR_nRST. The program counter restarts at the reset vector. VCC_CORE, VCC_PLL, and VCC_SRAM are disabled by the PWR_EN output. VCC_IO, VCC_MEM, VCC_LCD, VCC_BB, and VCC_USIM are disabled by the SYS_EN output.

nWAKEUP/nRESET – When implemented in software, this signal serves two purposes. In RUN mode, this signal acts as a product reset signal and causes the CPU to restart at the reset vector. It will also cause the hardware reset of all other hardware devices on the board, as well as return some CPU registers to their reset state. Refer to PXA270 Developer's Manual for more information on which registers are affected by GPIO Resets. When the CPU is in a low power state, like Sleep or Deep Idle, this signal acts as an external wakeup source causing the CPU to return to RUN mode. The exact function of this signal in end applications can vary depending on how the software is implemented.

For information on Logic Product Development's BSP implementation of these signals, please refer to specific BSP documentation.

5 Summary

The PXA270 processor is a highly configurable device. This application note recommends power management options end customers should consider when implementing their specific designs. If further application-specific information is required, please contact product.sales@logicpd.com for assistance.