PXA270 Card Engine IO Controller Specification

Hardware Documentation

Logic PD // Products
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Revision History

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	NK	Release	KTL	04/19/05
B	JW NK	- Section 3.1.2 Peripheral Register0 Description of USB_SOFT_CONNECT correction: 0 = USB Device disabled; 1 = USB Device enabled; USB_SOFT_CONNECT reset value changed from 1 to 0. - Section 3.1.11 Interrupt Register: bits 4 & 3 corrected to be "R" only; corrected definition of UCB1400_INT and WRLAN_INT.	KTL	06/23/05
C	JCA	- Added CPLD Version column to Rev History - General formatting and design changes - Updated Product Brief - Section 1.2: updated list for acronyms used in document - Section 1.3: updated Xilinx CPLD part number	JCA	07/11/07
D	SMC	-Updated document for current style and for the PXA270-11 release; no content changes	JCA	05/03/11

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1 Introduction

1.1 Overview

Logic PD offers production-ready IO controller devices and design packages for customers creating custom Card Engine designs and CPLD code for Logic PD's Card Engines. Logic PD has optimized the VHDL code to fit in the smallest possible programmable logic device. This helps you stay focused on your high-value core technologies and fast forwards your embedded designs.

1.2 Acronyms

BALE	Buffered Address Latch Enable
CF	CompactFlash
CPLD	Complex Programmable Logic Device
CS	Chip Select
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
IO	Input Output
IRQ	Interrupt Request
ISA	Industry Standard Architecture
LAN	Local Area Network
SPI	Serial Peripheral Interface

1.3 Technical Specifications

Please refer to the following component specifications and data sheets.

- Xilinx CoolRunner-II CPLD data sheet (XC2C64-7VQG100C)
- Xilinx Device Package Information data sheet
- Xilinx Ordering Information

1.4 IO Controller Advantages

Some of the key features in the IO Controller include:

- Chip Select Decoder
- Interrupt Encoder
- CompactFlash Interface
- ISA-Like Bus Interface
- Bus Control Logic
- Programmable Register Control
- GPIO Interface
- In-System Programmability via JAM Player

The IO Controller VHDL source code is available for purchase. Contact Logic PD for more information.

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2 IO Controller Block Diagram

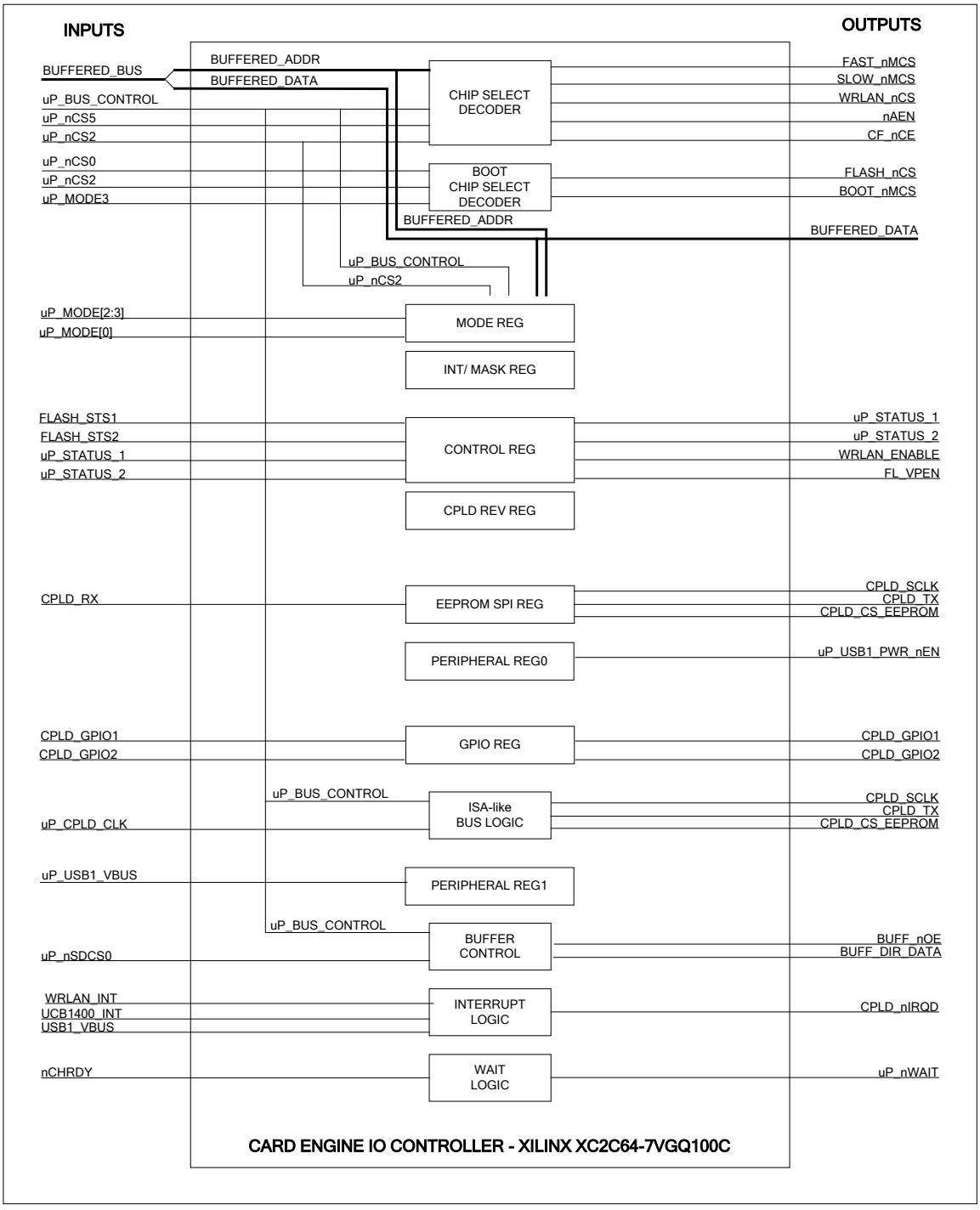

Figure 2.1: IO Controller Block Diagram

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3 IO Controller Address and Register Definitions

Address Range	Memory Block Description	Area Size
0x0800 0000 – 0x0BFF FFFF	Fast Peripherals Chip Select 2 (CS2)	64MB
0x1400 0000 – 0x17FF FFFF	Slow Peripherals Chip Select 5 (CS5)	64MB

3.1 Fast Peripherals Chip Select 2 (CS2)

Address Range	Memory Block Description	Area Size
0x0800 0000 – 0x0800 0003	Card Engine Control Reg	4Byte
0x0800 0004 – 0x0800 000F	Peripheral Reg0	12Byte
0x0800 0010 – 0x0800 0013	Peripheral Reg1	4Byte
0x0800 0014 – 0x0800 001F	IO Controller Code Revision Reg	12Byte
0x0800 0020 – 0x0800 0023	EEPROM SPI Reg	4Byte
0x0800 0024 – 0x0800 002F	Mode Reg	12Byte
0x0800 0030 – 0x0800 0033	GPIO Reg	4Byte
0x0800 0034 – 0x0800 003F	Reserved	12Byte
0x0800 0040 – 0x0800 0043	Interrupt Mask Reg	4Byte
0x0800 0044 – 0x0800 004F	Reserved	12Byte
0x0800 0050 – 0x0800 0053	Interrupt Reg	4Byte
0x0800 0054 – 0x0800 005F	Reserved	12Byte
0x0800 0060 – 0x0800 0063	BSP1 Support Reg	4Byte
0x0800 0064 – 0x0800 006F	BSP2 Support Reg	12Byte
0x0800 0070 – 0x0800 0073	Reserved	4Byte
0x0800 0074 – 0x08FF FFFF	Reserved	16MByte – 102Byte
0x0900 0000 – 0x09FF FFFF	Wired LAN Chip Select	16MByte
0x0A00 0000 – 0x0AFF FFFF	External Fast_nCS	16MByte
0x0B00 0000 – 0x0BFF FFFF	Flash_nCS when uP_MODE3 = 0 Boot_nCS when uP_MODE3 = 1	16MByte

To access the CPLD registers, chip select 2 should be defined on GPIO78 and should be setup as a 16 bit VLIO area. The CPLD register data is presented on the lowest 8 bits of the data bus.

Each memory block for chip select 2 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.1.1 Card Engine Control Register

Address Range: 0x0800 0000

- This register holds control bits for the card engine.

7	6	5	4	
-	FLASH_POPULATED	STATUS_2	STATUS_1	
-	0	1	1	reset
-	R/W	R/W	R/W	R/W

3	2	1	0	
FL_VPEN	STS2	STS1	WRLAN_nENABLE	
0	x	x	0	reset
R/W	R	R	R/W	R/W

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FLASH_POPULATED: Flash populated bit. This bit is used to generate the FLASH_nCS signal. See Section 4.2 for a detailed description.
0 = no affect
1 = when uP_MODE3 is low FLASH_nCS assertion is prevented

STATUS_2: STATUS_2 bit, configured as an input on reset, direction controlled by GPIO_REG(3). Asserted by an open drain output.
0 = Set pin low if configured as output, read pin state low if configured as input
1 = Set pin high if configured as output, read pin state high if configured as input

STATUS_1: STATUS_1 bit, configured as an input on reset, direction controlled by GPIO_REG(2). Asserted by an open drain output.
0 = Set pin low if configured as output, read pin state low if configured as input
1 = Set pin high if configured as output, read pin state high if configured as input

FL_VPEN: Flash write enable bit. Prevents writes to onboard NOR FLASH chips.
0 = flash write protected
1 = flash write not protected

STS2: Flash Status2 bit. This bit shows the status for flash chip 2.
0 = flash busy
1 = flash ready

STS1: Flash Status1 bit. This bit shows the status for flash chip 1.
0 = flash busy
1 = flash ready

WRLAN_ENABLE: wired LAN power enable signal. This bit enables/disables power to the on-board wired LAN chip.
0 = Wired LAN enabled
1 = Wired LAN disabled

3.1.2 Peripheral Register0

Address Range: 0x0800 0004

- This register contains control bits for USB Device enable.

7	6	5	4	3	2	1	0	
-	-	-	USB_SOFT_CONNECT	-	-	-	-	
-	-	-	0	-	-	-	-	reset
-	-	-	R/W	-	-	-	-	R/W

USB_SOFT_CONNECT: USB enable bit. Enables or disables USB Device interface.
0 = USB Device disabled
1 = USB Device enabled

3.1.3 Peripheral Register1

Address Range: 0x0800 0010

- This register tells if a USB device is attached and creates an interrupt upon connection/disconnection.

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7	6	5	4	3	2	1	0	
-	-	USB_DEVICE_ATTACHED	-	-	-	-	-	
-	-	x	-	-	-	-	-	reset
-	-	R	-	-	-	-	-	R/W

USB_DEVICE_ATTACHED: USB attached bit. This bit tells if a USB device is attached. An interrupt is created, VBUS_INT in the Interrupt register each time the device is connected or disconnected.

0 = USB device not attached
1 = USB device attached

3.1.4 IO Controller Code Revision Register

Address Range: 0x0800 0014

- This register holds the IO Controller code revision number.

7	6	5	4	3	2	1	0	
8-bit revision number								
8-bit revision number								reset
R								R/W

3.1.5 EEPROM SPI Interface Register

Address Range: 0x0800 0020

- This register holds SPI data during a read/write between the processor and on-board EEPROM. The SPI interface used for the EEPROM must be implemented in software and implemented by the processor, not the IO Controller.

7	6	5	4	3	2	1	0	
-	-	-	-	EECS	EECK	EETX	EERX	
-	-	-	-	0	0	0	x	reset
-	-	-	-	R/W	R/W	R/W	R	R/W

EECS: EEPROM chip select.

0 = not selected (CPLD_CS_EEPROM driven low)
1 = EEPROM chip selected (CPLD_CS_EEPROM driven high)

EECK: EEPROM SPI clock.

0 = output CPLD_CLK signal driven low
1 = output CPLD_CLK signal driven high

EETX: EEPROM SPI data transmit.

0 = output CPLD_TX driven low
1 = output CPLD_TX driven high

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EERX: EEPROM SPI data receive.

0 = input CPLD_RX reads low
1 = input CPLD_RX reads high

3.1.6 Mode Register

Address Range: 0x0800 0024

- This register holds the values of the mode pins.

7	6	5	4	3	2	1	0	
-	-	-	-	uP_MODE3	uP_MODE2	-	uP_MODE0	
-	-	-	-	x	x	-	x	reset
-	-	-	-	R	R	-	R	R/W

uP_MODE3: Mode pin 3. Mode pin 3 selects between on-board and off-board boot device. See Section 4.2 for detailed information on mode pin 3.

0 = off-board boot device
1 = on-board boot device

uP_MODE2: Mode pin 2. Mode pin 2 controls running scripts from LoLo.

0 = scripts are not run at LoLo boot time
1 = scripts are run at LoLo boot time

uP_MODE0: Mode pin 0. This mode pin represents the bus width at boot.

0 = Asynchronous 32-bit ROM/flash memory
1 = Asynchronous 16-bit ROM/flash memory

3.1.7 GPIO Register

Address Range: 0x0800 0030

- This register controls extended general-purpose signals.

7	6	5	4	3	2	1	0	
GPIO2_ DDR	GPIO1_ DDR	GPIO2	GPIO1	STS2_ DDR	STS1_ DDR	IGNORE_PCMCIA	-	
1	1	1	1	1	1	1	-	reset
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W

GPIO2_DDR: GPIO2 direction bit.

0 = external CPLD signal CPLD_GPIO_2 is an output
1 = external CPLD signal CPLD_GPIO_2 is an input

GPIO1_DDR: GPIO1 direction bit.

0 = external CPLD signal CPLD_GPIO_1 is an output
1 = external CPLD signal CPLD_GPIO_1 is an input

GPIO2: Controls the state of general purpose I/O bit CPLD_GPIO_2 when configured as an output; reads pin state when configured as an input.

0 = Set pin low if configured as output, read pin state low if configured as input
1 = Set pin high if configured as output, read pin state high if configured as input

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GPIO1: Controls the state of general purpose I/O bit CPLD_GPIO_1 when configured as an output; reads pin state when configured as an input.
0 = Set pin low if configured as output, read pin state low if configured as input
1 = Set pin high if configured as output, read pin state high if configured as input

STS2_DDR: STATUS_2 direction bit.
0 = external CPLD signal STATUS_2 is an output
1 = external CPLD signal STATUS_2 is an input

STS1_DDR: STATUS_1 direction bit.
0 = external CPLD signal STATUS_1 is an output
1 = external CPLD signal STATUS_1 is an input

IGNORE_PCMCIA: PCMCIA ignore bit. Determines if PCMCIA reads should be accounted for when creating the BUFF_DIR_DATA signal.
0 = use PCMCIA_nRD signal for determining BUFF_DIR_DATA
1 = ignore PCMCIA_nRD signal for determining BUFF_DIR_DATA

3.1.8 Reserved

Address Range: 0x0800 0034 – 0x0800 003F

- These memory blocks are reserved for future use.

3.1.9 Interrupt Mask Register

Address Range: 0x0800 0040

- This register contains the information used by the IO Controller to mask an interrupt to the processor on signal CPLD_nIRQ.

7	6	5	4	3	2	1	0	
-	-	-	MSK_UCB1400	MSK_WRLAN	MSK_VBUS	-	-	
-	-	-	0	0	0	-	-	reset
-	-	-	R/W	R/W	R/W	-	-	R/W

MSK_UCB1400: UCB1400 touch/codec chip interrupt mask.
0 = interrupt masked
1 = interrupt not masked

MSK_WRLAN: Wired LAN chip interrupt mask.
0 = interrupt masked
1 = interrupt not masked

MSK_VBUS: USB_VBUS interrupt mask.
0 = interrupt masked
1 = interrupt not masked

3.1.10 Reserved

Address Range: 0x0800 0044 – 0x0800 004F

- These memory blocks are reserved for future use.

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3.1.11 Interrupt Register

Address Range: 0x0800 0050

- This register contains the information used by the IO Controller to generate an interrupt to the processor on signal CPLD_nIRQ.

7	6	5	4	3	2	1	0	
-	-	-	UCB1400_INT	WRLAN_INT	VBUS_INT	-	-	
-	-	-	0	0	0	-	-	reset
-	-	-	R	R	R/W	-	-	R/W

UCB1400_INT: UCB1400 touch/CODEC chip interrupt request (IRQ). Reading this bit returns external signal state of CODEC chip U13's interrupt line. Interrupt can only be cleared at source chip U13.

0 = no interrupt
1 = interrupt

WRLAN_INT: Wired LAN chip interrupt request (IRQ). Reading this bit returns external signal state of wired LAN chip U10's interrupt line. Interrupt can only be cleared at source chip U10.

0 = no interrupt
1 = interrupt

VBUS_INT: USB_VBUS interrupt request (IRQ). Set when a USB Device cable is inserted or removed. Cleared by writing a 0 to this bit until another cable transition occurs.

0 = no interrupt
1 = interrupt

3.1.12 Reserved

Address Range: 0x0800 0054 – 0x0800 005F

- These memory blocks are reserved for future use.

3.1.13 BSP1 Support Register

Address Range: 0x0800 0060

- This register is for BSP support.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	-	
-	-	1	-	-	-	-	-	reset
-	-	R	-	-	-	-	-	R/W

3.1.14 BSP2 Support Register

Address Range: 0x0800 0064

- This register is for BSP support.

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7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	-	
-	-	1	-	-	-	-	-	reset
-	-	R	-	-	-	-	-	R/W

3.1.15 Reserved

Address Range: 0x0800 0070 – 0x0800 0073

- These memory blocks are reserved for future use.

3.1.16 Reserved

Address Range: 0x0800 0074 – 0x08FF FFFF

- These memory blocks are reserved.

3.1.17 Wired LAN Chip Select

Address Range: 0x0900 0000 – 0x09FF FFFF

- This area of memory is used when accessing the wired LAN chip (internal registers/memory).

3.1.18 Reserved On-Board Memory Blocks

Address Range: 0x0A00 0000 – 0x0AFF FFFF

- This memory block is reserved for off-board IO controller expansion. FAST_nCS chipselect is asserted in this area.

3.1.19 Available Off-Board Memory Blocks

Address Range: 0x0B00 0000 – 0x0BFF FFFF

- This memory block is open and available for the user to utilize. BOOT_nCS chipselect is asserted in this area when uP_MODE3 is high. FLASH_nCS is asserted when uP_MODE3 is low and FLASH_POPULATED is also low.

3.2 Slow Peripherals Chip Select 5 (CS5)

Address Range	Memory Block Description	Size
0x1400 0000 – 0x14FF FFFF	CF Chip Select	16MB
0x1500 0000 – 0x15FF FFFF	ISA-like Bus Chip Select	16MB
0x1600 0000 – 0x16FF FFFF	Reserved	16MB
0x1700 0000 – 0x17FF FFFF	Open	16MB

Each memory block for Chip Select 5 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.2.1 CompactFlash (CF) Chip Select

Address Range: 0x1400 0000 – 0x14FF FFFF

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- This area of memory is used when accessing the off-board memory mapped CompactFlash Type 1 Memory Only slot.

3.2.2 ISA-like Bus Chip Select

Address Range: 0x1500 0000 – 0x15FF FFFF

- The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This area of memory is used when accessing off-board components on the “ISA-like” bus. See Section 4 for read and write timing diagrams.

3.2.3 Reserved On/Off-Board Memory Block

Address Range: 0x1600 0000 – 0x16FF FFFF

- This memory block is reserved for future on-board expansion. SLOW_nCS chipselect is asserted in this area.

3.2.4 Open Memory Block

- This memory block is available for customer use. SLOW_nCS chipselect is asserted in this area.

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4 IO Controller Functions

This section describes in detail the different IO Controller function blocks. See Section 2 for the IO Controller block diagram.

4.1 Chip Select Decoder Logic

This logic decodes processor memory areas 2 and 5 into smaller segments of memory. See Section 3.1 for the chip select 2 memory map, and Section 3.2 for the chip select 5 memory map.

CPLD signal FAST_nCS is output when uP_nCS2 is low, uP_MA25 is high, and uP_MA24 is low. CPLD signal SLOW_nCS is output when uP_nCS5 is low and uP_MA25 is high. Signals FAST_nCS and SLOW_nCS are brought off the card engine through the expansion bus connectors.

4.2 Boot Chip Select Decoder Logic

Note: Mode pin 3 selects between on-board and off-board boot device. Mode pin 0 selects between 16 and 32-bit memory device.

The card engine can boot from the 32-bit on-board flash or a 16 or 32-bit off-board memory device. The boot device is determined by a jumper setting (mode pin 3) on the application board. The boot device is always located in area 0 (CS0). When mode pin 3 is high, the on-board flash is selected for boot, and when mode pin 3 is low, the off-board memory device is selected for boot. The logic is shown in the following table. The size is determined by a jumper setting (mode pin 0) on the application board. When mode pin 0 is low, a 32-bit memory device is specified for boot, and when mode pin 0 is high, a 16-bit memory device is specified for boot.

Card Engine Control register bit (6) is used to prevent the flash chip select, when mode pin 3 is low. The bit is ignored when mode pin 3 is high. See Section 3.1.1 for more information on the Card Engine Control register.

Flash (on-board)	Off-board memory	Mode Pin 3	Control Reg (6)	Function
CS0 (area 0)	CS2 (area 2)	1	ignored	boot from flash in area 0, off-board memory device is in area 2
CS2 (area 2)	CS0 (area 0)	0	0	boot from off-board memory device in area 0, flash is in area 2
1	CS0 (area 0)	0	1	boot from off-board memory device in area 0, (flash not populated) area 2 is open

The chip selects for area 0 and 2 are routed externally to the flash and off-board memory device by signals FLASH_nCS and BOOT_nMCS.

4.3 ISA-like Bus Logic and CompactFlash Support in area 5

The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This logic outputs the ISA chip select and BALE signals. It also creates one timing delay in the ISA-like bus timing: the delay between the rising edge of the read or write signal and rising edge of the chip select.

The ISA device chip select is output by the CPLD when an access to address range 0x1500 0000 – 0x15FF FFFF is made, and the CompactFlash chip select is output when an access to address range 0x1400 0000 – 0x14FF FFFF is made. To create a timing delay between the rising edge of the read or write signal and the rising edge of the chip select, the chip select rising edge is delayed from the processor's area 5 chip select by two bus clock cycles. See Section 5 for sample read and write ISA-like timing diagrams.

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The ISA-like bus timing is shown with internal wait states programmed for the processor. This is shown in order to meet CompactFlash timing. The VLIO interface of the PXA270 is used to create these timings. The user can verify/change these values by modifying the MSC5[RDN], MSC5[RRR], and MSC5[RDF] fields in the processor's Static Memory Control Register, for area 5. Recommended values are MSC5[RDN] = 0x3, MSC5[RRR] = 0x1, and MSC5[RDF] = 0xC to meet CompactFlash timing. For ISA timing, MSC5[RDF] should be 0xF to allow maximum wait states and if the device requires longer bus cycles, the uP_nWAIT signal should be asserted until the cycle is complete.

The nCHRDY input signal to the CPLD is shown in the ISA-like bus timing diagrams. It can be asserted by a Compact Flash or an ISA device. When pulled low, the nCHRDY signal generates a low on the uP_nWAIT signal to the processor, extending the length of the current cycle beyond the programmed internal wait states. The nCHRDY low pulse width for CompactFlash is a maximum of 350ns, and an example of this signal is shown in the timing diagrams. Not all CompactFlash cards or ISA devices will assert the nCHRDY signal. Therefore, the other signals in the read and write timing diagrams are shown assuming the nCHRDY signal was not pulled low.

4.4 Wired LAN Bus Logic

An interrupt to the processor is generated on the CPLD_nIRQ line when an interrupt from the wired LAN is seen at the CPLD.

The WIREDLAN_nENABLE bit enables or disables power to the Ethernet power plane. Low = enabled, High = disabled.

The Ethernet chip can be accessed within this memory window 0x0900 0000 – 0x09FF FFFF.

4.5 Buffer Control Logic

This logic controls the output enable and direction of the on-board buffers.

If PCMCIA is used, the IGNORE_PCMCIA bit in the GPIO register should be set to 0 so the buffers direction changes correctly during PCMCIA reads.

4.6 Interrupt Logic

This logic generates the processor's CPLD_nIRQ, from information in the Interrupt Mask register, Section 3.1.9, and the Interrupt register, Section 3.1.11.

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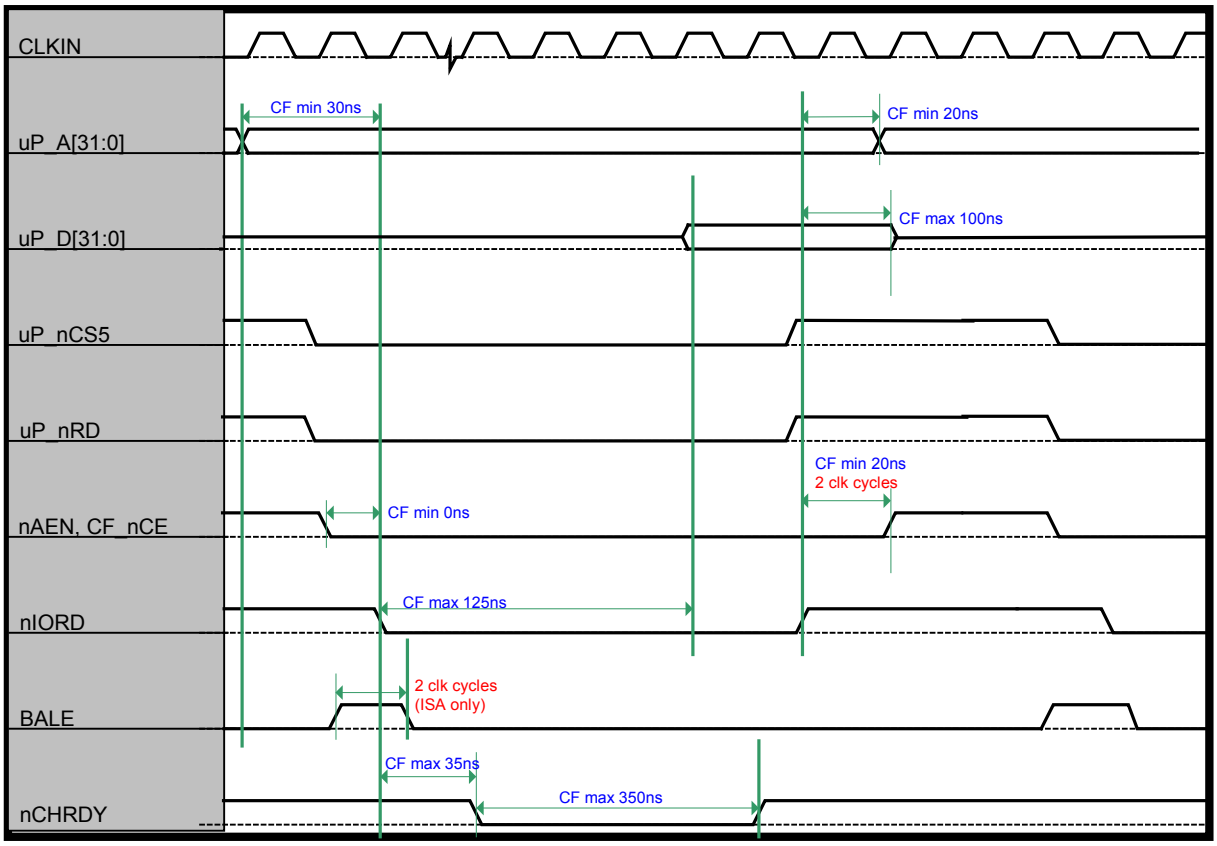
5 ISA and CompactFlash Timing Diagrams

nAEN and BALE only asserted during ISA accesses.

CF_nCE only asserted during CompactFlash accesses.

5.1 ISA-like Bus and CompactFlash Read Cycle Timing Diagram



Note: All timing parameters shown in nanoseconds (ns).

Figure 5.1: ISA-like Bus and CompactFlash Read Cycle Timing

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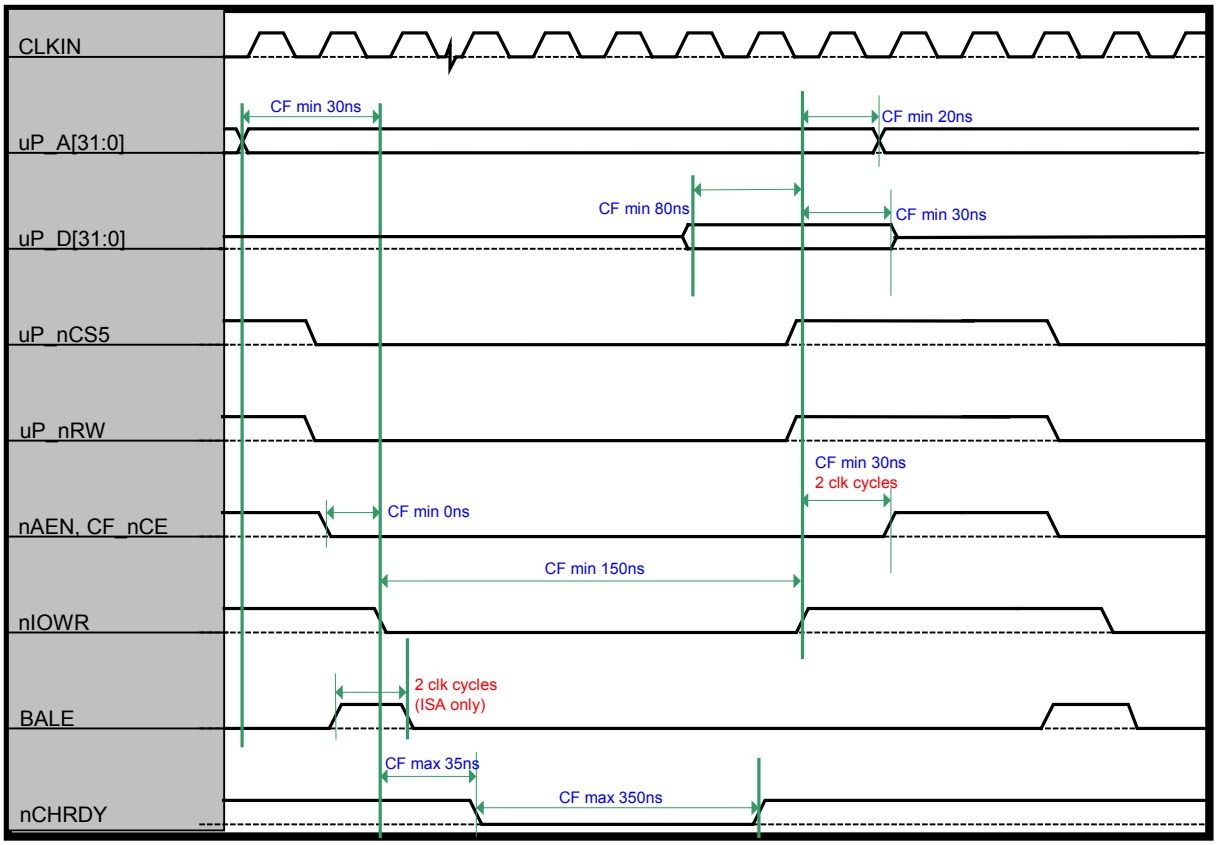
5.2 ISA-like Bus and CompactFlash Write Cycle Timing Diagram



Note: All timing parameters shown in nanoseconds (ns).

Figure 5.2: ISA-like Bus and CompactFlash Write Cycle Timing Diagram

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6 IO Controller Pin Information

Pin	Signal Name	Input/Output
30	CPLD_RX	Input
32	FLASH_STS1	Input
4	FLASH_STS2	Input
99	MSTR_nRST	Input
70	PCC_SLOT_SELECT_A_nB	Input
92	UCB1400_INT	Input
68	WRLAN_INT	Input
23	uP_BUS_CLK	Input
33	uP_MA0	Input
34	uP_MA1	Input
35	uP_MA2	Input
36	uP_MA3	Input
37	uP_MA4	Input
39	uP_MA5	Input
40	uP_MODE0	Input
41	PCMCIA_nRD	Input
42	uP_MODE2	Input
67	uP_MODE3	Input
64	uP_PCC_nCE1	Input
61	uP_PCC_nCE2	Input
7	uP_USB1_VBUS	Input
50	uP_USB2_PWR_nEN	Input
52	uP_nCS0	Input
53	uP_nCS2	Input
8	uP_nCS5	Input
56	uP_nRD	Input
58	uP_nSDCS0	Input
22	nIOWR	Input
14	BALE	Output
79	BOOT_nCS	Output
91	WRLAN_nCS	Output
90	BUFF_nOE	Output
28	CF_nCE	Output
2	CPLD_CLK	JTAG
1	CPLD_CS_EEPROM	Output
89	CPLD_GPIO_1	Input/Output
6	CPLD_GPIO_2	Input/Output

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Pin	Signal Name	Input/Output
94	CPLD_TX	Output
24	FAST_nCS	Output
78	FLASH_nCS	Output
97	FL_VPEN	Output
77	PCC_nCE1A	Output
76	PCC_nCE1B	Output
74	PCC_nCE2A	Output
72	PCC_nCE2B	Output
27	SLOW_nCS	Output
13	uP_MD6	Input/Output
12	uP_MD7	Input/Output
11	uP_MD4	Input/Output
10	uP_MD2	Input/Output
9	uP_MD3	Input/Output
29	nAEN	Output
71	CPLD_nIRQ	Output
17	uP_MD0	Input/Output
19	uP_MD1	Input/Output
18	uP_MD5	Input/Output
15	uP_STATUS_1	Input/Output
3	uP_STATUS_2	Input/Output
16	uP_USB1_PWR_nEN	Output
81	uP_USB2_PWR_EN	Output
49	WRLAN_ENABLE	Output
60	BUFF_DIR_DATA	Output
43	uP_nWAIT	Input/Output
55	nCHRDY	Input
48	CPLD_TCK	Input
45	CPLD_TDI	Input
83	CPLD_TDO	Output
47	CPLD_TMS	Input
20,38,51,88,98	3.3V	Vi/o
57,26,5	1.8V	Vcore
21,31,62,69,84,100,25,75	GND	GND
44,45,46,47,48,54,59,63, 65,66,73,80,82,83,85,86, 87,93,95,96	Unused	Unused

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