NCR

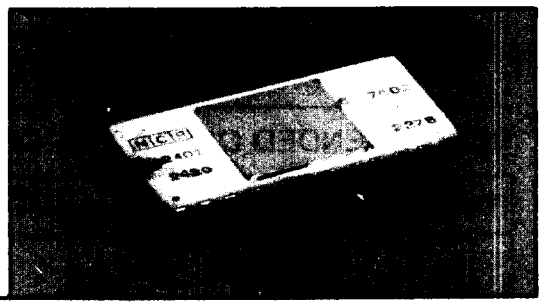
NCR CORPORATION

4096-BIT EAROM™ MEMORY

2401

MICROELECTRONICS DIVISION 8181 BYERS ROAD MIAMISBURG, OHIO 45342 | (513) 866-7471
TLX 28-8010 NCRMICRO, MSBG

Electrically alterable ROM MNOS P-channel technology



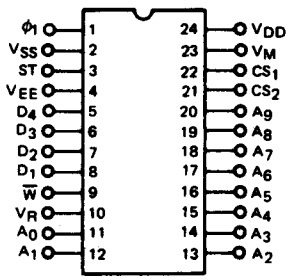
STANDARD 24 PIN SIDE BRAZE DIP
(1.2 x 0.6 IN.) .6" Rows

S-62 003506 ORIG

T-3504 NCR

- 1024 X 4 Organization
- 10-Bit Binary Addressing
- 2 Chip Select Inputs
- Electrically Reprogrammable
- 2.0 μs Access Time
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- ~~Minimum Data Retention~~—10^{11} Read Accesses/Word Between Refresh
- ~~Three State Outputs~~
- 24 Pin Ceramic DIP
- Unpowered, Nonvolatile Data Storage — 10 Years at 70° C
- Control, Address and Data Inputs TTL–Compatible with Pull-Up Resistors

PIN CONFIGURATION

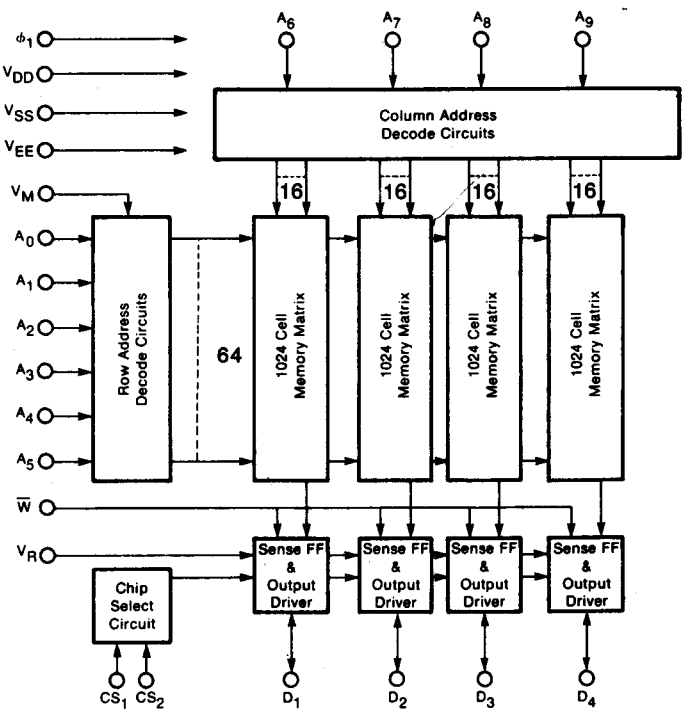


The NCR 2401 is a fully decoded, 1024 x 4-bit electrically erasable and reprogrammable ROM utilizing second-generation NCR MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 4096 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Stored data may be accessed a minimum of 10^{11} times without refresh and is nonvolatile in the unpowered state in excess of ten years. Data is erased by applying a −28 V pulse to the erase substrate of the device. Although the NCR 2401 is not intended for use as a read/write memory, data can be erased and rewritten up to a maximum of 10^4 times.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

All inputs or outputs relative to V_{SS} ..... +0.3V to −30V
Operating ambient temperature ..... 0°C to +70°C
Storage temperature ..... −65° C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

* Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS, T_A = 0°C TO 70°C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS} + 0.3V	V_{SS}−29	V_{SS}−28	V_{SS}−27	V_{SS}−20	V_{SS}−19	V_{SS}−18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage		V_{SS}		V_{SS}−29	V_{SS}−28	V_{SS}−27	V_{SS}−10.5	V_{SS}−10	V_{SS}−9.5	V
V_R	Reference voltage		V_{SS}		V_{SS}	V_{SS}	V_{SS}	V_{SS}−20	V_{SS}−19	V_{SS}−18	V
V_{EEH}	Erase substrate input high	V_{SS}−0.4	V_{SS}	V_{SS}+0.3	V_{SS}−0.4	V_{SS}	V_{SS}+0.3	V_{SS}−0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}−29	V_{SS}−28	V_{SS}−27	V_{SS}−0.4	V_{SS}	V_{SS}+0.3	V_{SS}−0.4	V_{SS}	V_{SS}+0.3	V
V_{WH}	Write control input high	V_{SS}−29	V_{SS}	V_{SS}+0.3	V_{SS}−1.5	V_{SS}	V_{SS}+0.3	V_{SS}−1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}−29		V_{SS}−4.4	V_{SS}−29		V_{SS}−4.4	V_{SS}−1.5	V_{SS}	V_{SS}+0.3	V
$V_{\phi H}$	ϕ_1 input high voltage		Don't Care		V_{SS}−0.8	V_{SS}	V_{SS}+0.3	V_{SS}−0.8	V_{SS}	V_{SS}+0.3	V
$V_{\phi L}$	ϕ_1 input low voltage		Don't Care		V_{SS}−29	V_{SS}−28	V_{SS}−27.0	V_{SS}−25	V_{SS}−19	V_{SS}−18	V
V_{IH}	Address and CS input high		Don't Care		V_{SS}−1.5	V_{SS}	V_{SS}+0.3	V_{SS}−1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low		Don't Care		V_{DD}		V_{SS}−4.4	V_{DD}		V_{SS}−4.4	V
V_{DH}	Data input high voltage		Don't Care		V_{SS}−1.5	V_{SS}	V_{SS}+0.3		Not Applicable		V
V_{DL}	Data input low voltage		Don't Care		V_{DD}		V_{SS}−4.4		Not Applicable		V

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C TO 70°C

NO EXTERNAL LOADS EXCEPT AS NOTED

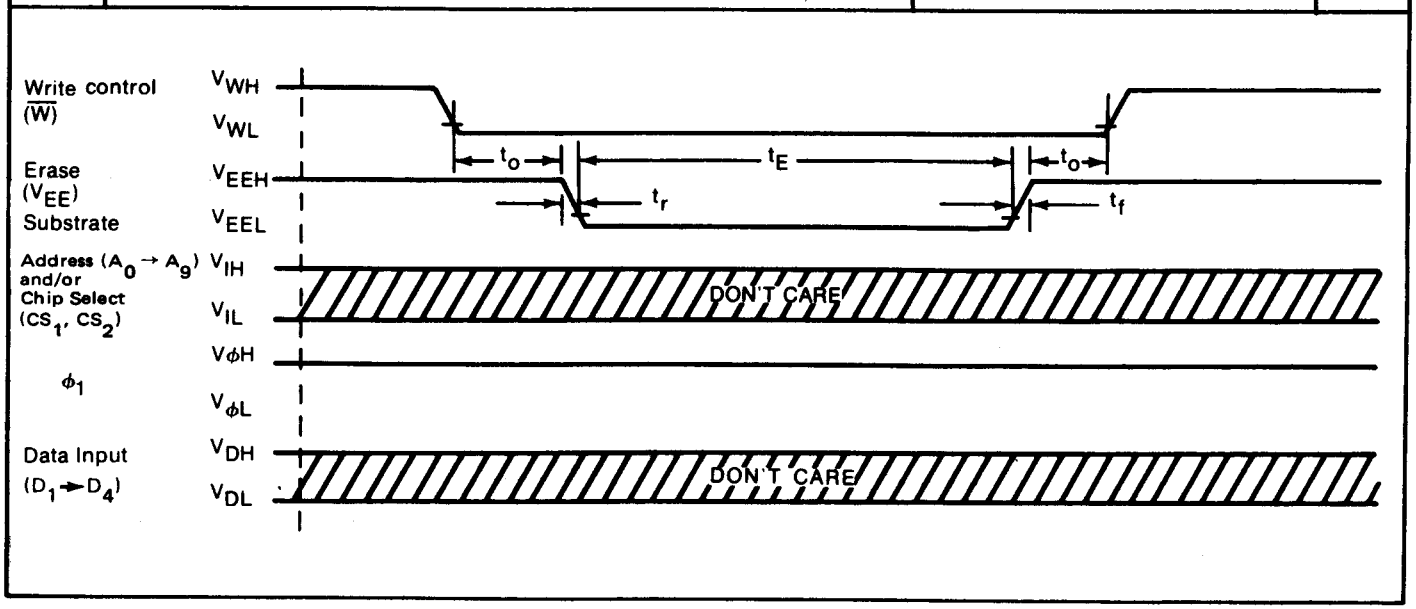
Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) @ V_{SS}−15V	$\phi 1 = V_{DD} = V_{SS}$−20			-2.0	μA
$I_{\phi 1}$	ϕ_1 Leakage current @ V_{SS}−29V	$V_{DD} = V_{SS}$−29, W = V_{SS}−25			-200	μA
I_0	Output leakage current @ V_{SS}−15V	Chip deselected			-10.0	μA
I_{EEL}	Erase substrate leakage current @ V_{SS}−28V	W = V_{SS}−25			-200	μA
I_{DD1}	V_{DD} supply current — read mode @ V_{SS}−19V	Outputs open See Figure 6		-8.5	-12	mA
I_{DD2}	V_{DD} supply current — write mode = V_{SS}−28V	Outputs open See Figure 5		-18	-25	mA
V_{OH}	Data output high voltage — TTL load	One Series 7400 TTL load with R_S = 1KΩ $V_{CC} = V_{SS}$	-2.0			mA
V_{OL}	Data output low voltage — TTL load	(See TTL Notes, Page 6)	+3.2			mA
V_{OH}	Data Output high voltage — MOS	C_L = 100pf	V_{SS}−1.5			V
V_{OL}	Data Output Low Voltage — MOS	C_L = 100pf			V_{SS} − 10	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	10			Years

CAPACITANCE AT $V_{IN} = V_{SS}$, ALL OTHER PINS GROUNDED (V_{SS}), f = 1 MHZ

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance		5	7	pf
C_W	Write control input capacitance		10	20	pf
$C_{\phi 1}$	ϕ_1 Input Capacitance		40	50	pf
C_{EE}	Erase substrate capacitance		600	700	pf
C_D	Data input/output capacitance		6	10	pf

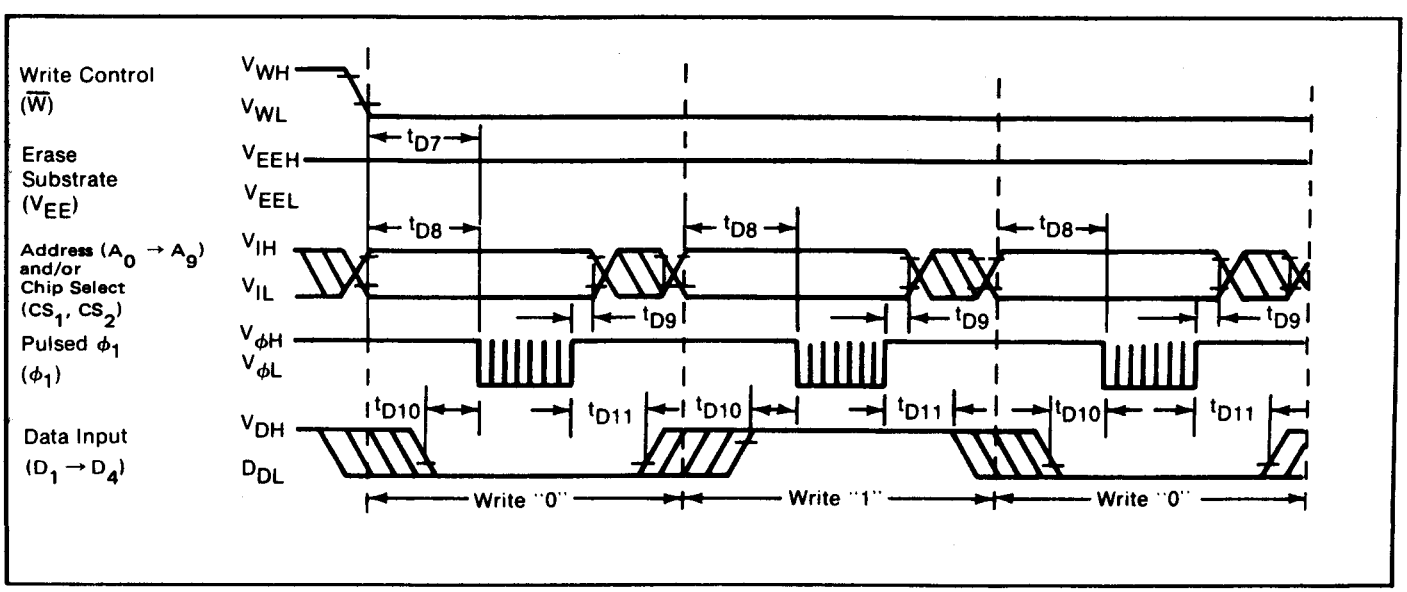
ERASE CYCLE CHARACTERISTICS, T_A = 0° C TO 70°C

Symbol	Parameter	Min	Typ	Max	Unit
t_E	V_{EE} erase pulse width	100		1000	mS
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01		1.0	mS
t_o	Write-erase overlap	10			μS



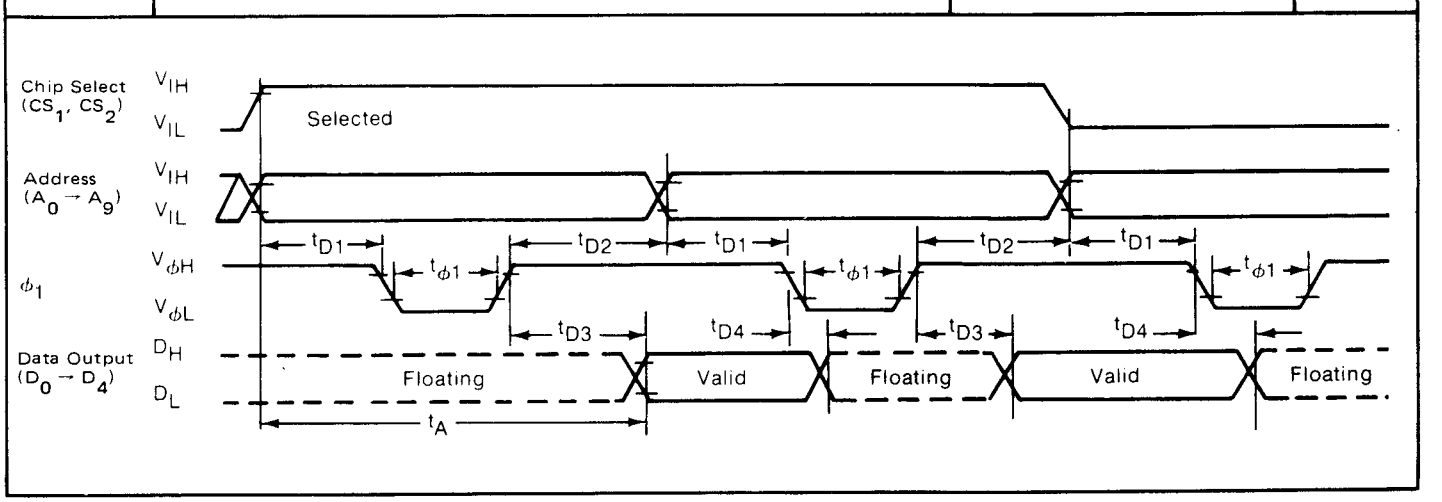
WRITE CYCLE CHARACTERISTICS, T_A = 0°C TO 70°C (SEE NOTE 3)

Symbol	Parameter	Min	Typ	Max	Unit
$N_{\phi W}$	Number of ϕ_1 write pulses (@ 100 μS ± 10%, 5 μS min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500			nS
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500			nS
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0			μS
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0			μS
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0			μS
N_W	Number of times word may be rewritten			10^4	



READ CYCLE CHARACTERISTICS T_A = 0°C to 70°C

Symbol	Parameter (See figures 1 through 4)	Min	Typ	Max	Unit
t_A	Access time			2.0	μS
$t_{\phi 1}$	ϕ_1 Pulse width (rise and fall times ≤ 50NS) (See Note 1)	850		2000	nS
t_{D1}	Address and chip select change to ϕ_1 rise delay	400			nS
t_{D2}	ϕ_1 Fall to address and chip select change delay	0			μS
t_{D3}	ϕ_1 Fall to data output valid delay (See Notes 1 and 2)			750	nS
t_{D4}	ϕ_1 Rise to floated output delay			300	nS
N_{RA}	Number of read accesses word between refresh	10^{11}			



FUNCTIONAL INFORMATION

ALL CONTROL, ADDRESS AND DATA INPUTS ARE TTL-COMPATIBLE WITH PULL-UP RESISTORS

Chip Select (CS_1, CS_2)

Both must be in the high state to enable the data output terminals or write data into the device.

Data Input/Output ($D_1 \rightarrow D_4$)

D_1 through D_4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

Write Control ($\overline{W}$)

The write control terminal must be in the low state in order to write data into the device.

Phase One (ϕ_1)

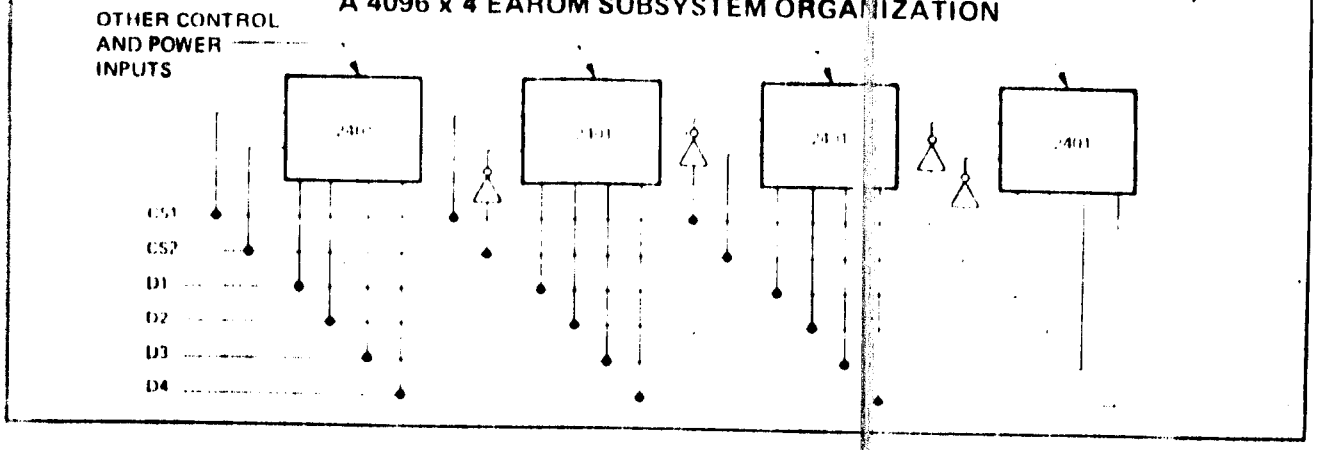
During the write operation, multiple 100 μs pulses must be applied to the ϕ_1 terminal to fully shift the memory transistor threshold voltage to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ_1 input is high-level and not TTL-compatible.

Note 1 — Due to the dynamic nature of the circuit, a "ϕ_1 NOT" time in excess of 40 μsec. may result in a floated output condition. Consequently, data must be resampled within a 40 μsec. time period following the fall of ϕ_1 to ensure its validity.

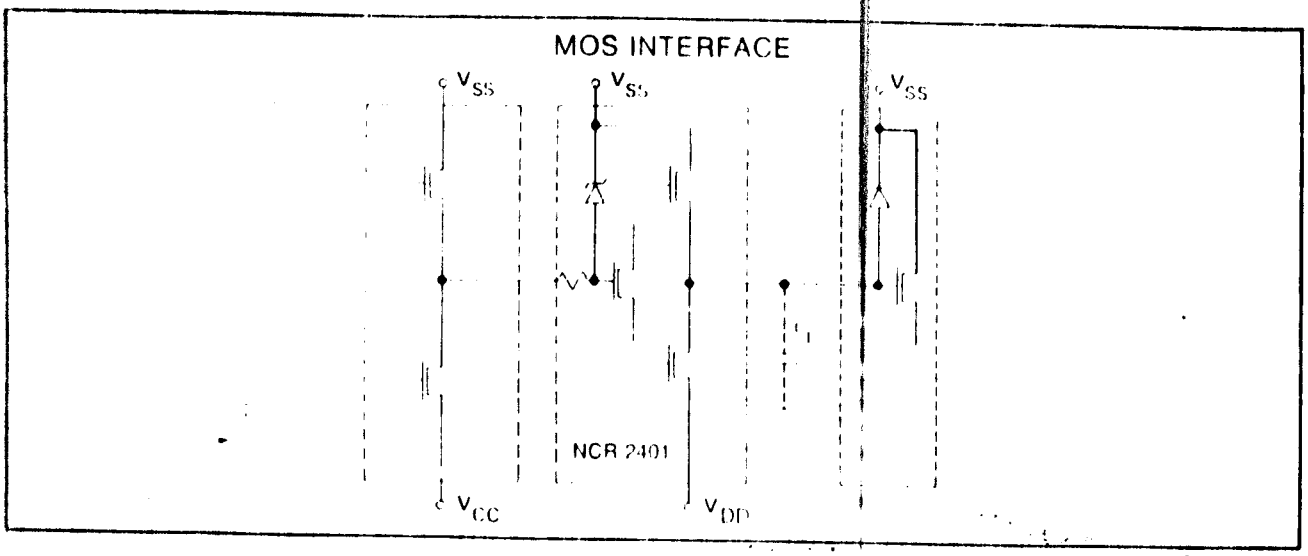
Note 2 — Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ± 10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.

Note 3 — Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.

A 4096 x 4 EAROM SUBSYSTEM ORGANIZATION



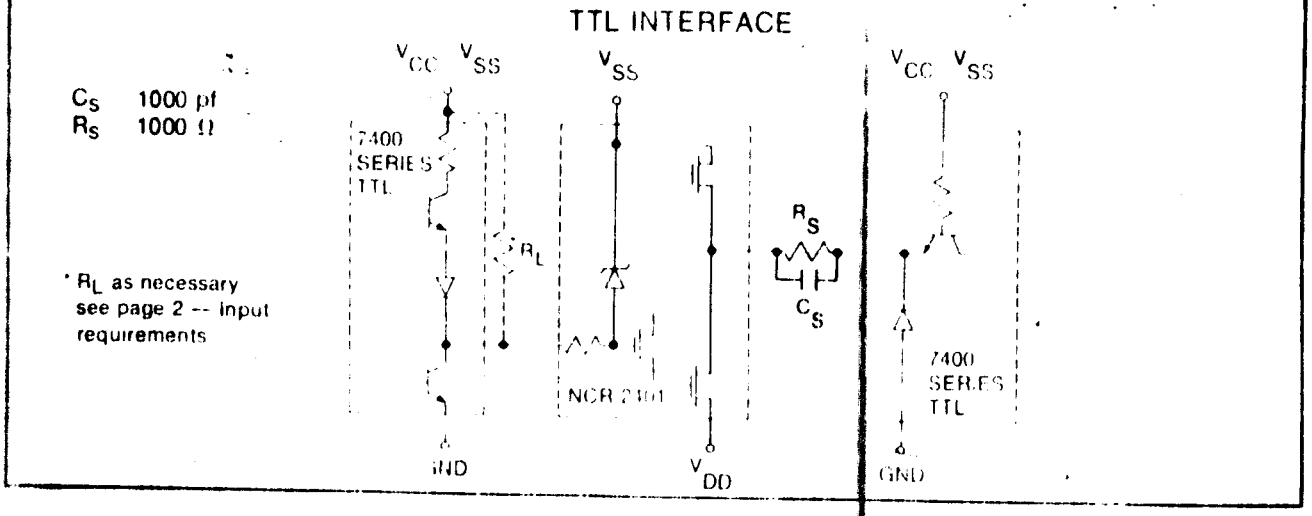
MOS INTERFACE



TTL INTERFACE

C_S 1000 pf
R_S 1000 Ω

* R_L as necessary see page 2 -- input requirements



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