

PM75CBS060

FLAT-BASE TYPE
INSULATED PACKAGE

PM75CBS060



FEATURE

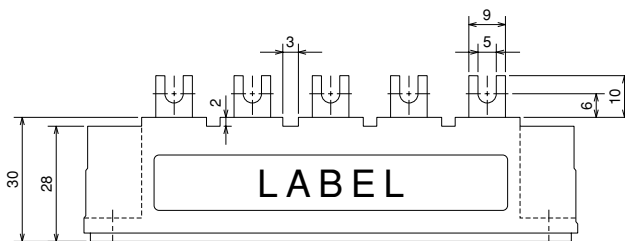
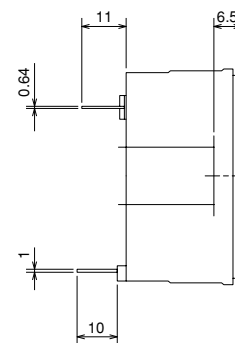
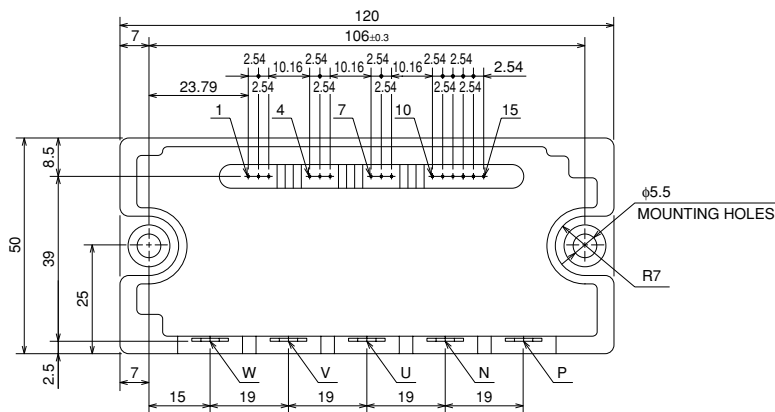
- a) Adopting 4th generation IGBT chip, which performance is improved by 1 μ m fine rule process.
For example, typical $V_{ce(sat)}$ =1.7V
- b) Using new Diode which is designed to get soft reverse recovery characteristics.
- c) Over-temperature protection by detecting T_j of the IGBT chips
 - 3 ϕ 75A, 600V Current-sense IGBT type inverter
 - Monolithic gate drive & protection logic
 - Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage
 - Acoustic noise-less 5.5/7.5kW class inverter application

APPLICATION

Servo drives and other motor controls

PACKAGE OUTLINES

Dimensions in mm



Terminal code

- | | |
|---------|---------|
| 1. VWPC | 9. VUP1 |
| 2. WP | 10. VNC |
| 3. VWP1 | 11. VN1 |
| 4. VVPC | 12. WN |
| 5. VP | 13. VN |
| 6. VVP1 | 14. UN |
| 7. VUPC | 15. Fo |
| 8. UP | |

PM75CBS060

FLAT-BASE TYPE
INSULATED PACKAGE

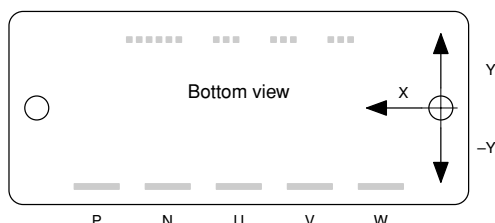
TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
VCC(prot)	Supply Voltage Protected by OC & SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _j = 125°C Start	400	V
VCC(surge)	Supply Voltage (Surge)	Applied between : P-N, Surge value	500	V
T _c	Module Case Operating Temperature	(Note-1)	-20 ~ +110	°C
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	V _{rms}

(Note-1) T_c(under the chip) measurement point is below.

(Unit : mm)

Arm Axis	UP		VP		WP		UN		VN		WN	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	83.3	83.3	41.8	41.8	16.8	16.8	70.8	70.8	54.3	54.3	29.3	29.3
Y	3.8	-4.3	3.8	-4.3	3.8	-4.3	-2.3	-10.3	-2.3	-10.3	-2.3	-10.3



THERMAL RESISTANCES

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	T _c measured point is just under the chips Inverter IGBT part (per 1/6 module)	—	—	0.27*	°C/W
R _{th(j-c)F}		T _c measured point is just under the chips Inverter FWDi part (per 1/6 module)	—	—	0.47*	°C/W
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied	—	—	0.046	°C/W

*: If you use this value, R_{th(f-a)} should be measured just under the chips.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 75A V _{CIN} = 0V, Pulsed (Fig. 1)	T _j = 25°C T _j = 125°C	—	1.7	2.3	V
V _{EC}	FWDi Forward Voltage	-I _C = 75A, V _D = 15V, V _{CIN} = 15V (Fig. 2)		—	2.2	3.3	V
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 15V↔0V V _{CC} = 300V, I _C = 75A T _j = 125°C Inductive Load (Fig. 3)		0.8	1.2	2.4	μs
t _{rr}				—	0.15	0.3	μs
t _{c(on)}				—	0.4	1.0	μs
t _{off}				—	2.4	3.3	μs
t _{c(off)}				—	0.5	1.0	μs
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _D = 15V (Fig. 4)	T _j = 25°C T _j = 125°C	—	—	1 10	mA

PM75CBS060

FLAT-BASE TYPE
INSULATED PACKAGE

CONTROL PART

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
ID	Circuit Current	VD = 15V, V _{CIN} = 15V	VN1-VNC	—	40	60	mA
			VXP1-VXPC	—	13	18	
V _{th(ON)}	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN-VNC		1.2	1.5	1.8	V
V _{th(OFF)}	Input OFF Threshold Voltage			1.7	2.0	2.3	V
OC	Over Current Trip Level	VD = 15V (Fig. 5,6)	T _J = -20°C	—	—	330	A
			T _J = 25°C	145	198	270	
			T _J = 125°C	115	—	—	
SC	Short Circuit Trip Level	-20 ≤ T _J ≤ 125°C, VD = 15V (Fig. 5,6)		—	241	—	A
t _{off(OC)}	Over Current Delay Time	VD = 15V (Fig. 5,6)		—	10	—	μs
OT	Over Temperature protection	Detect T _J of IGBT chip	Trip level	135	145	155	°C
OT _r			Reset level	—	125	—	°C
UV	Supply Circuit Under-Voltage Protection	-20 ≤ T _J ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV _r			Reset level	—	12.5	—	V
I _{FO(H)}	Fault Output Current	VD = 15V, V _{FO} = 15V (Note-2)		—	—	0.01	mA
I _{FO(L)}				—	10	15	mA
t _{FO}	Minimum Fault Output Pulse Width	VD = 15V (Note-2)		1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal OC, SC, OT & UV protection.
 Fault output of OC, SC, OT & UV protection operate by lower arm.
 Fault output of OC, SC protection given pulse.
 Fault output of OT, UV protection given pulse while over trip level.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Main terminal screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	400	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Conditions	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 400	V
V _D	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC VWP1-VWPC, VN1-VNC (Note-3)	15.0 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN-VNC	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 4.0	V
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig.8	≤ 20	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	μs

(Note-3) With ripple satisfying the following conditions
 dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

PM75CBS060

FLAT-BASE TYPE
INSULATED PACKAGE

PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "OC" and "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

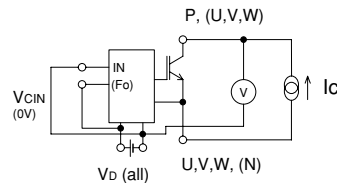


Fig. 1 $V_{CE(sat)}$ Test

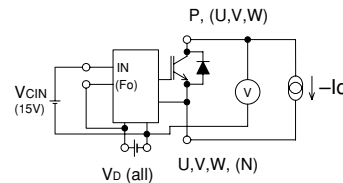


Fig. 2 V_{EC} Test

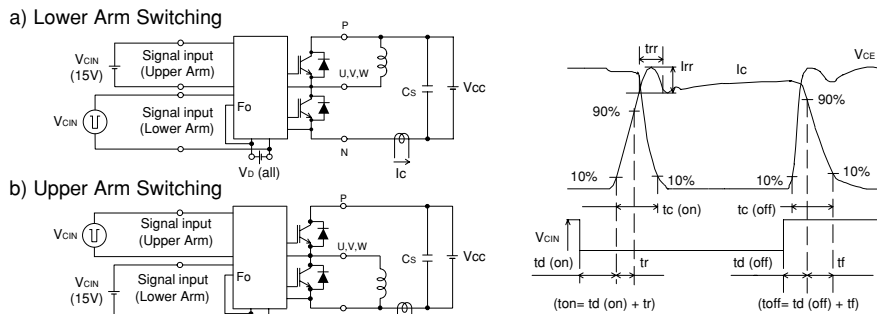


Fig. 3 Switching time Test circuit and waveform

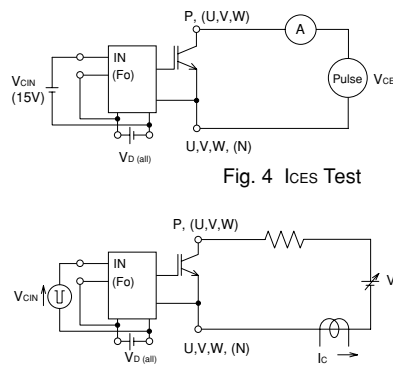


Fig. 4 I_{CES} Test

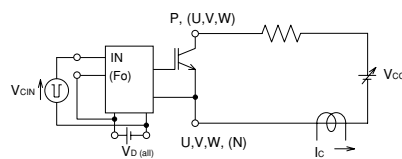


Fig. 5 OC and SC Test

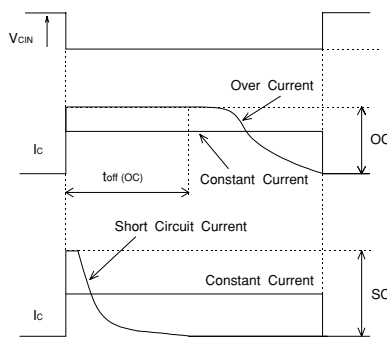


Fig. 6 OC and SC Test waveform

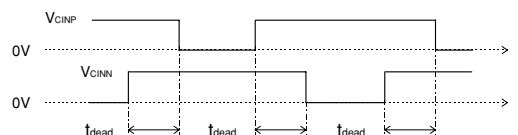


Fig. 7 Dead time measurement point example

PM75CBS060

FLAT-BASE TYPE
INSULATED PACKAGE

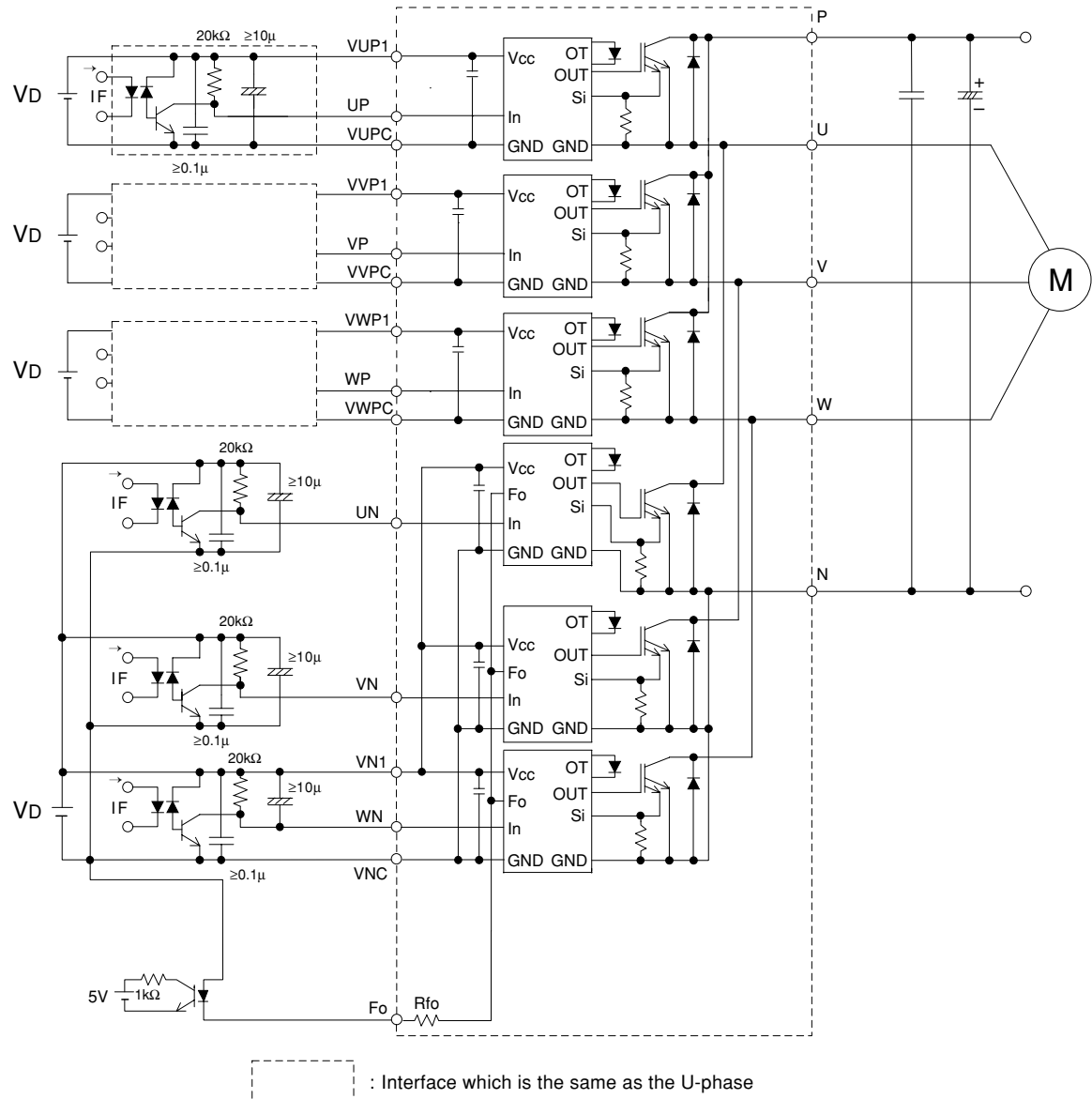


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler : CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.