
HN27C1024HG/HCC Series

65536-word × 16-bit CMOS UV Erasable and Programmable ROM

HITACHI

Description

The Hitachi HN27C1024H series is a 1-Mbit (64-kword × 16-bit) ultraviolet erasable and electrically programmable ROM. Fabricated on new advanced fine process technique, the HN27C1024H makes high speed access time 85/100 ns (max) possible. (HN27C1024H is the fastest 1-Mbit EPROM.) Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 8086 and 68000. The HN27C1024H offers high speed programming using page programming mode. It has the package variation of cerdip 40-pin and JLCC 44-pin.

Features

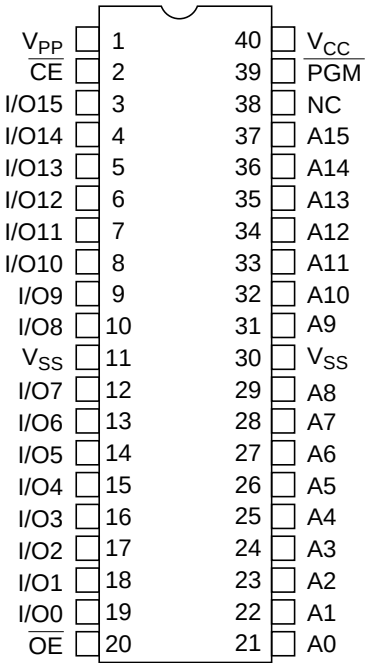
- Fast high-reliability programming mode and fast high-reliability page programming mode
Programming voltage: 12.5 V DC
Fast High-reliability page programming 14 sec (typ)
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 60 mW/MHz (typ)
- Device identifier mode: Manufacturer code and device code
- JEDEC standard

Ordering Information

Type No.	Access Time	Package
HN27C1024HG-85	85 ns	600-mil 40-pincerdip (DG-40A)
HN27C1024HG-10	100 ns	
HN27C1024HG-12	120 ns	
HN27C1024HG-15	150 ns	
HN27C1024HCC-85	85 ns	44-pin J-bend leaded chip carrier (CC-44)
HN27C1024HCC-10	100 ns	
HN27C1024HCC-12	120 ns	
HN27C1024HCC-15	150 ns	

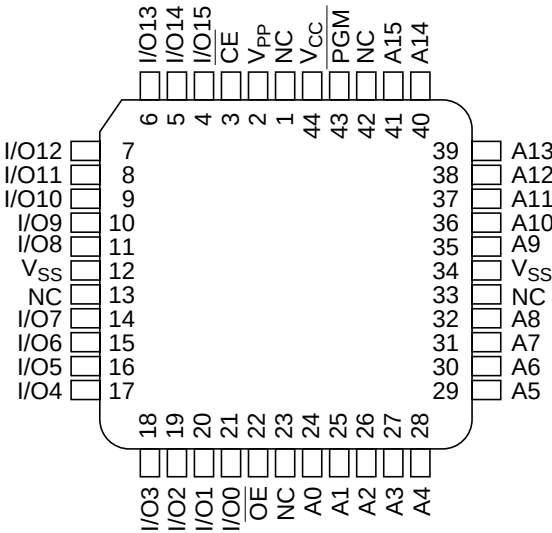
Pin Arrangement

HN27C1024HG Series



(Top view)

HN27C1024HCC Series

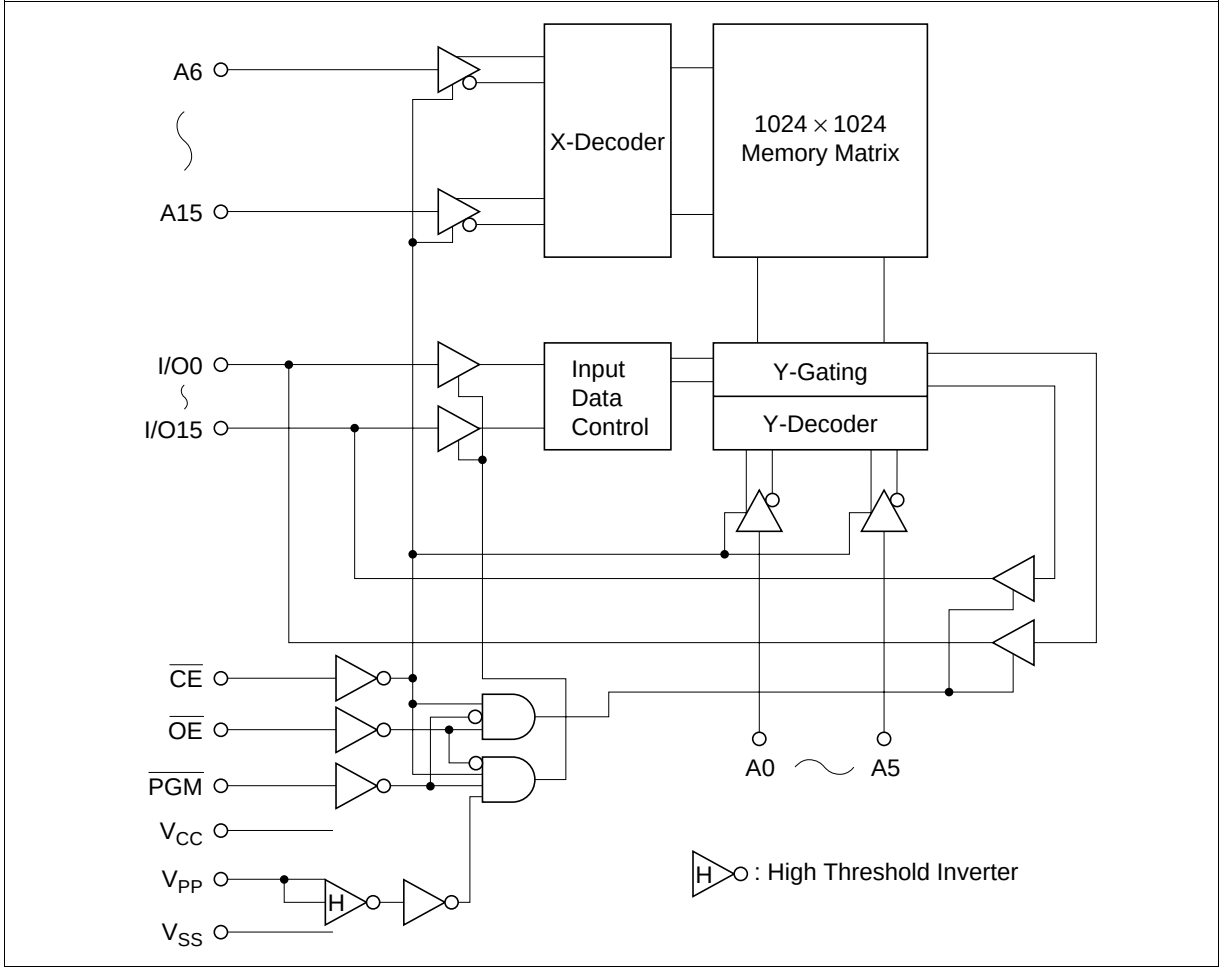


(Top view)

Pin Description

Pin Name	Function
A0 – A15	Address
I/O0 – I/O15	Input/output
CE	Chip enable
OE	Output enable
V _{CC}	Power supply
V _{PP}	Programming power supply
V _{SS}	Ground
PGM	Programming enable
NC	No connection

Block Diagram



Mode Selection

	Pin	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	V_{PP}	V_{CC}	A9	I/O
	G	(2)	(20)	(39)	(1)	(40)	(31)	(3 – 10, 12 – 19)
Mode	CC	(3)	(22)	(43)	(2)	(44)	(35)	(4 – 11, 14 – 21)
Read		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	Dout
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	X	High-Z
Standby		V_{IH}	X	X	V_{CC}	V_{CC}	X	High-Z
Program		V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	Din
Program verify		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	Dout
Page data latch		V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	Din
Page program		V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	High-Z
Program inhibit		V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	X	High-Z
		V_{IL}	V_{IH}	V_{IH}				
		V_{IH}	V_{IL}	V_{IL}				
		V_{IH}	V_{IH}	V_{IH}				
Identifier		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_{H}	Code

Notes: 1. X: Don't care
2. V_{H} : 12.0 V $\pm$ 0.5 V

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
All input and output voltages ^{*1}	Vin, Vout	−0.6 ^{*2} to +7.0	V
A9 input voltage ^{*1}	V_{ID}	−0.6 ^{*2} to +13.5	V
V_{PP} voltage ^{*1}	V_{PP}	−0.6 to +13.0	V
V_{CC} voltage ^{*1}	V_{CC}	−0.6 to 7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−65 to +125	°C
Storage temperature range under bias	Tbias	−10 to +80	°C

Notes: 1. Relative to V_{SS} .
2. Vin, Vout, V_{ID} min = −1.0 V for pulse width $\pm$ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

HN27C1024HG Series

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	12	pF	Vin = 0 V
Output capacitance	Cout	—	—	15	pF	Vout = 0 V

HN27C1024HCC Series

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{pp} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I _{LI}	—	—	2	μA	Vin = 5.25 V
Output leakage current	I _{LO}	—	—	2	μA	Vout = 5.25 V/0.45 V
V _{pp} current	I _{PP1}	—	1	20	μA	V _{pp} = 5.5 V
Standby V _{CC} current	I _{SB}	—	—	25	mA	$\overline{CE} = V_{IH}$
Operating V _{CC} current	I _{CC1}	—	—	50	mA	$\overline{CE} = V_{IL}$, Iout = 0 mA
	I _{CC2}	—	—	110	mA	f = 12 MHz, Iout = 0 mA
	I _{CC3}	—	—	25	mA	f = 1 MHz, Iout = 0 mA,
Input low voltage	V _{IL}	-0.3*1	—	0.8	V	
Input high voltage	V _{IH}	2.2	—	V _{CC} + 1.0*2	V	
Output low voltage	V _{OL}	—	—	0.45	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -400 μA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (Ta = 0 to +70°C, VCC = 5 V ± 5%, VPP = VCC)

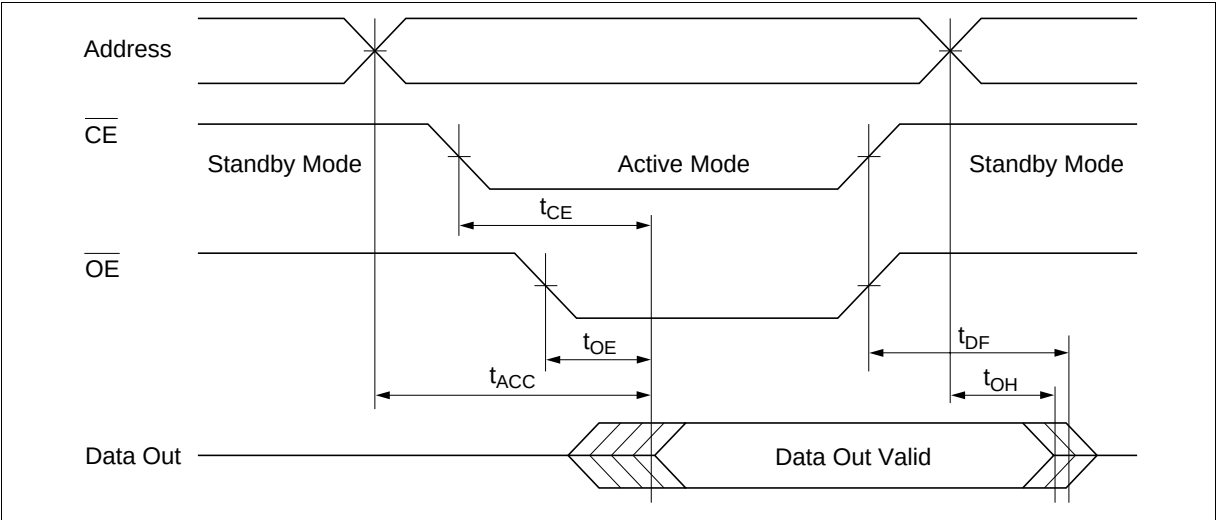
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall time: ≤ 10 ns
- Output load: 1 TTL gate + 100 pF
- Reference levels for measuring timing: Inputs; 1.5 V
Outputs; 1.5 V

		HN27C1024H									
		-85		-10		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Address to output delay	t _{ACC}	—	85	—	100	—	120	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t _{CE}	—	85	—	100	—	120	—	150	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t _{OE}	—	45	—	50	—	60	—	60	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	t _{DF}	0	30	0	50	0	50	0	50	ns	$\overline{CE} = V_{IL}$
Address to output hold	t _{OH}	0	—	0	—	0	—	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

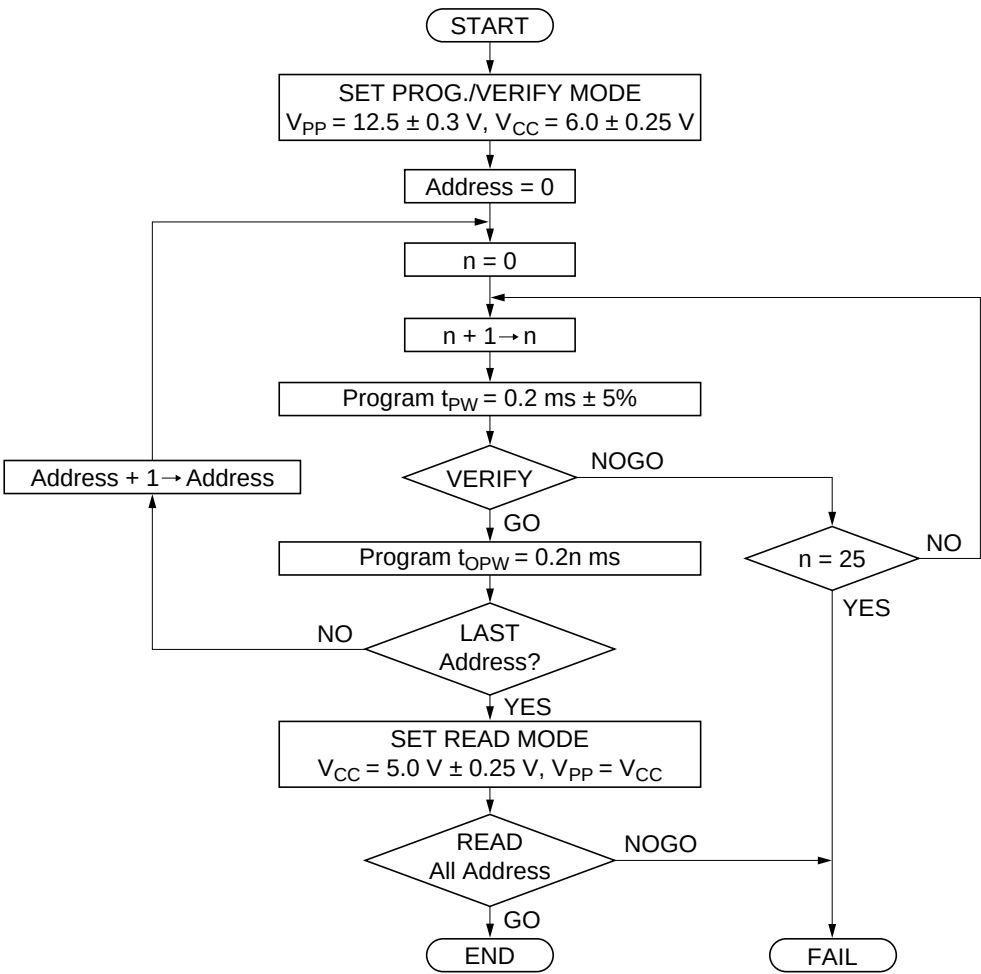
Note: tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I _{LI}	—	—	2	μA	V _{in} = 6.25 V/0.45 V
Output low voltage during verify	V _{OL}	—	—	0.45	V	I _{OL} = 2.1 mA
Output high voltage during verify	V _{OH}	2.4	—	—	V	I _{OH} = −400 μA
Operating Vcc current	I _{CC}	—	—	50	mA	
Input low level	V _{IL}	−0.1*5	—	0.8	V	
Input high level	V _{IH}	2.2	—	V _{CC} + 0.5*6	V	
V _{PP} supply current	I _{PP}	—	—	40	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

- Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = −0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ($T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$)

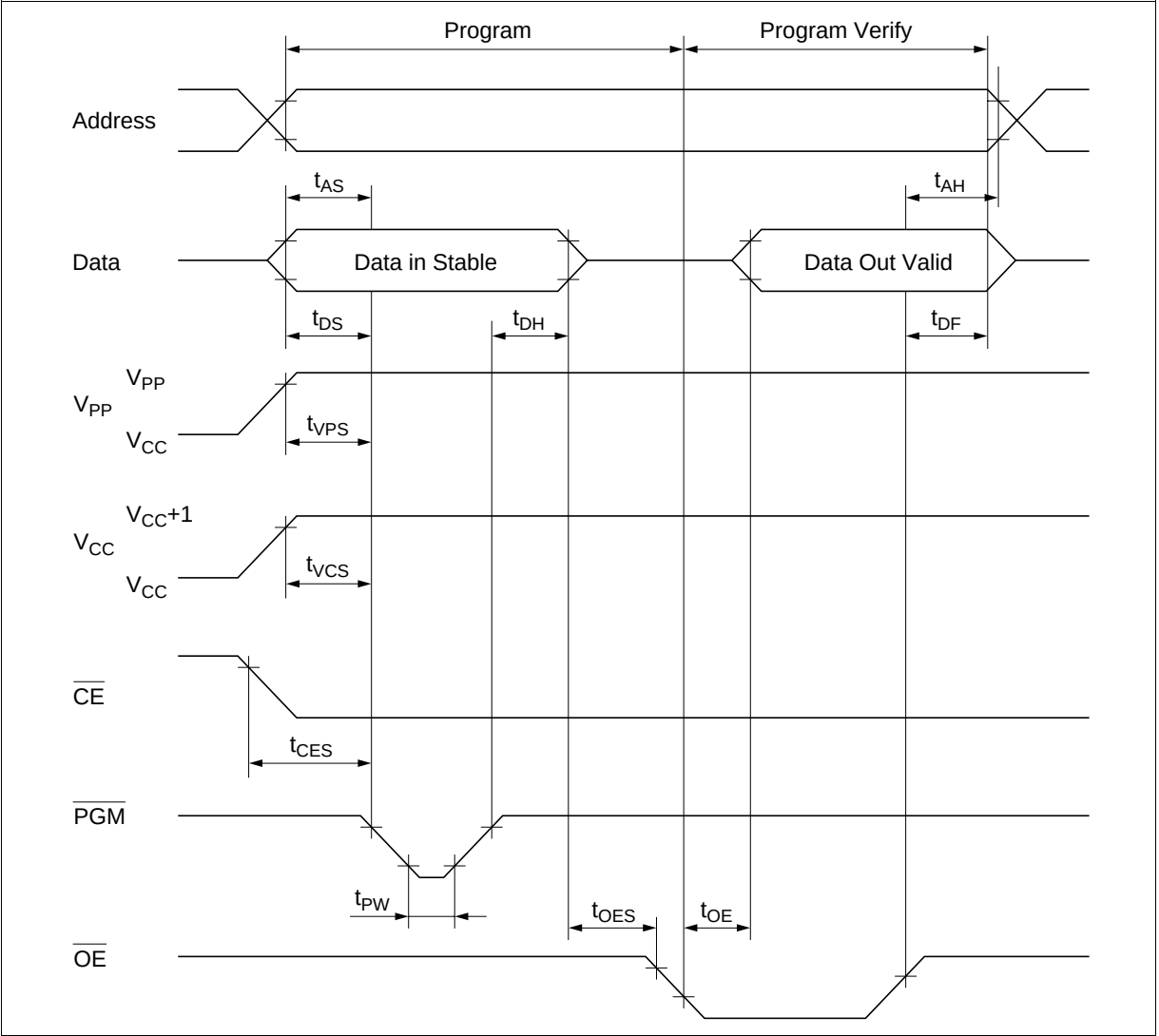
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time: $\leq 20\text{ ns}$
- Reference levels for measuring timing: Inputs: 0.8 V, 2.0 V
Outputs: 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	μs
$\overline{\text{OE}}$ setup time	t_{OES}	2	—	—	μs
Data setup time	t_{DS}	2	—	—	μs
Address hold time	t_{AH}	0	—	—	μs
Data hold time	t_{DH}	2	—	—	μs
$\overline{\text{OE}}$ to output float delay	t_{DF}^{*1}	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	μs
V_{CC} setup time	t_{VCS}	2	—	—	μs
PGM initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
PGM overprogramming pulse width	t_{OPW}^{*2}	0.19	—	5.25	ms
$\overline{\text{CE}}$ setup time	t_{CES}	2	—	—	μs
Data valid from $\overline{\text{OE}}$	t_{OE}	0	—	150	ns

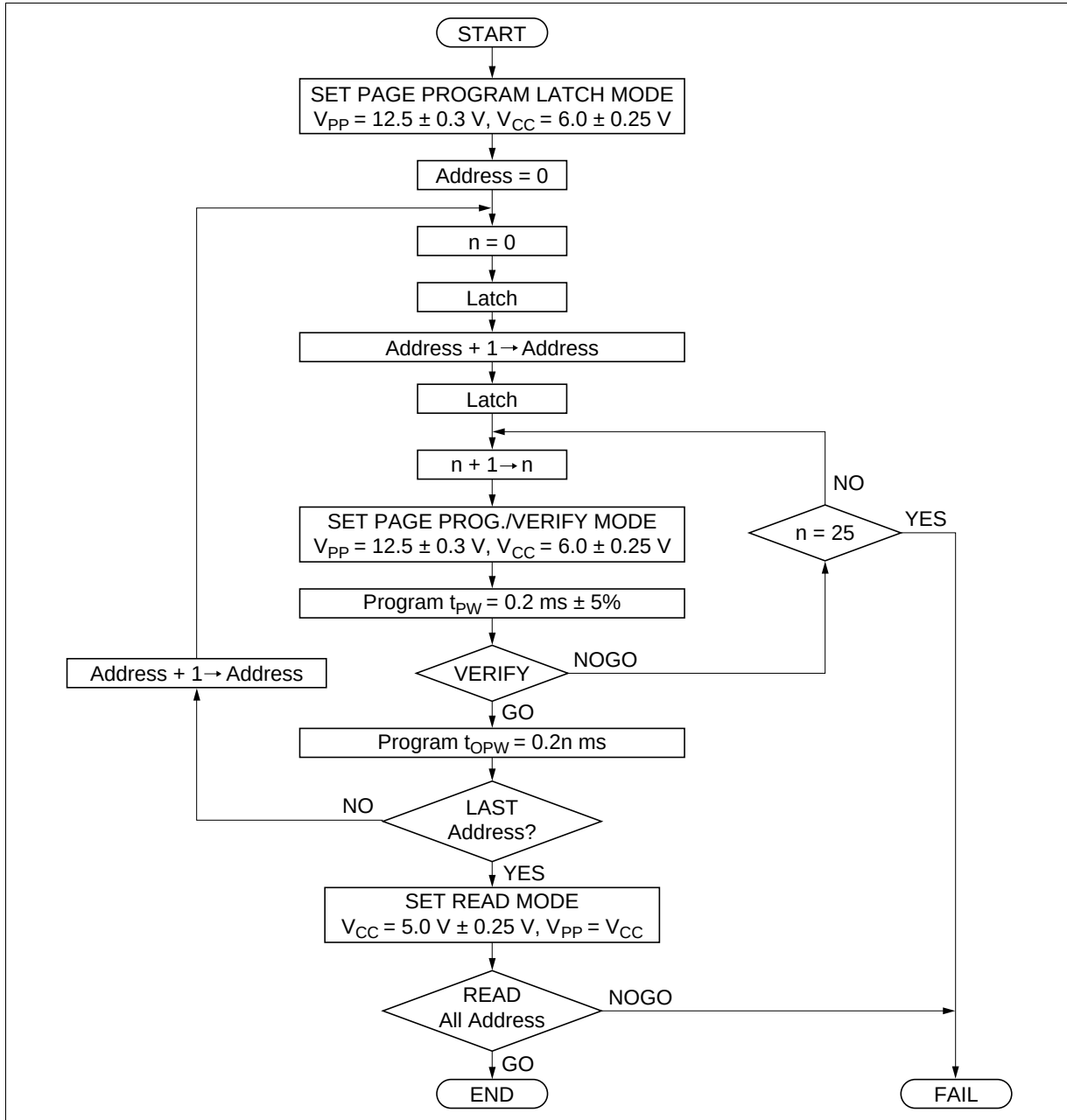
- Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW} .

Fast High-Reliability Programming Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Characteristics ($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.25\text{ V}/0.45\text{ V}$
Output low voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage during verify	V_{OH}	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input low level	V_{IL}	-0.1^{*5}	—	0.8	V	
Input high level	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
V_{PP} supply current	I_{PP}	—	—	50	mA	$\overline{\text{PGM}} = V_{IL}$

- Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously after V_{PP} .
 2. V_{PP} must not exceed 13 V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{ V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{\text{CE}} = \text{low}$.
 5. $V_{IL}\text{ min} = -0.6\text{ V}$ for pulse width $\leq 20\text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

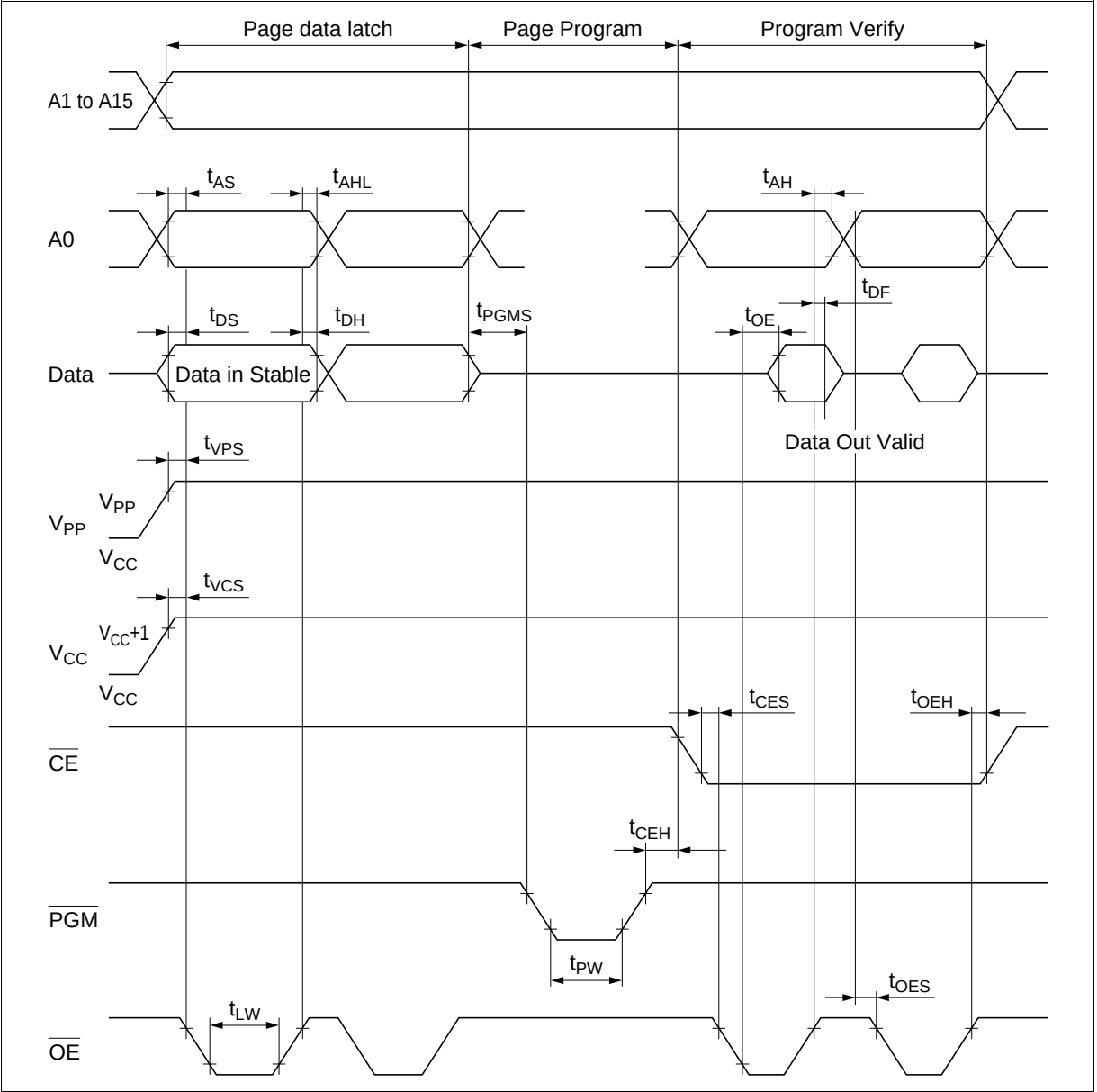
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time: $\leq 20\text{ ns}$
- Reference levels for measuring timings: Inputs; 0.8 V, 2.0 V
Outputs; 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	μs
$\overline{OE}$ setup time	t_{OES}	2	—	—	μs
Data setup time	t_{DS}	2	—	—	μs
Address hold time	t_{AH}	0	—	—	μs
	t_{AHL}	2	—	—	μs
Data hold time	t_{DH}	2	—	—	μs
$\overline{OE}$ to output float delay	t_{DF}^{*1}	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	μs
V_{CC} setup time	t_{VCS}	2	—	—	μs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	μs
$\overline{PGM}$ overprogramming pulse width	t_{OPW}^{*2}	0.19	—	5.25	μs
$\overline{CE}$ setup time	t_{CES}	2	—	—	μs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns
$\overline{OE}$ pulse width during data latch	t_{LW}	1	—	—	μs
$\overline{PGM}$ setup time	t_{PGMS}	2	—	—	μs
$\overline{CE}$ hold time	t_{CEH}	2	—	—	μs
$\overline{OE}$ hold time	t_{OEH}	2	—	—	μs

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Refer to the programming flowchart for t_{OPW} .

Fast High-Reliability Programming Timing Waveform



Erase

Erase of HN27C4096G/CC is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to “1” after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W · sec/cm².

Mode Description

Device Identifier Mode

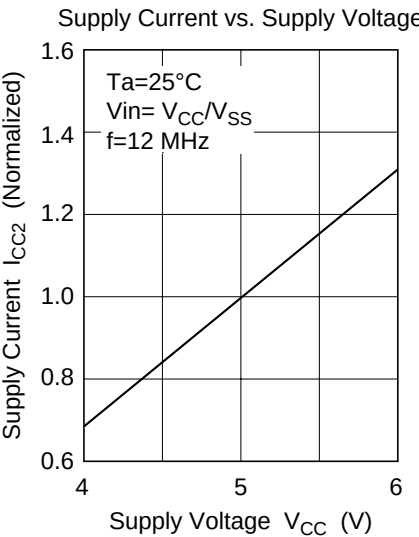
The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

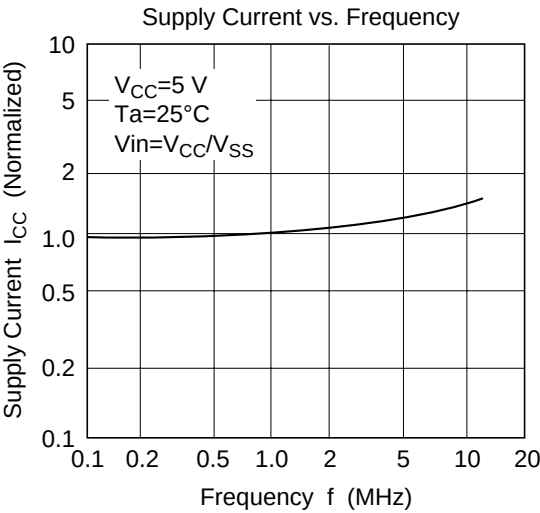
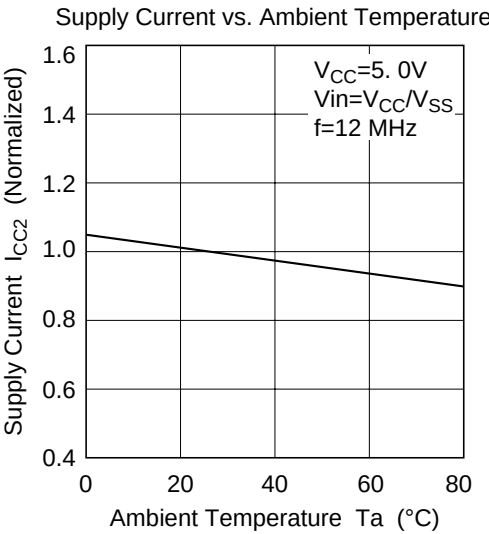
HN27C1024H Identifier Code

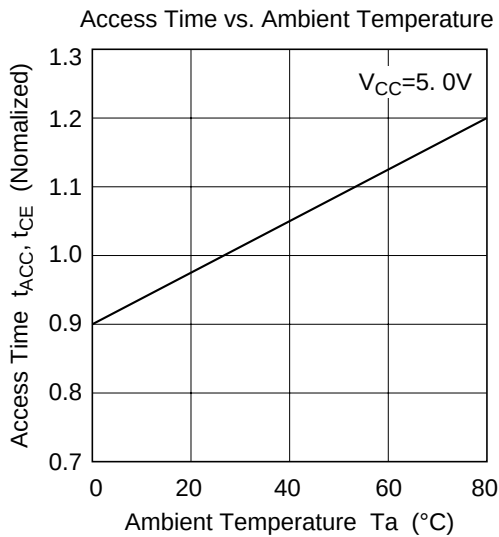
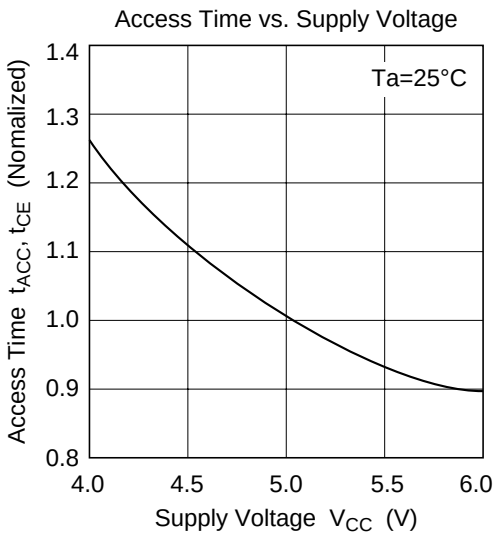
	Pin	A0	I/O8 to I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	
	G	(21)	(10) to (3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	
Identifier	CC	(24)	(11) to (4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	Data Hex
Manufacturer code	V_{IL}	X		0	0	0	0	0	1	1	1	07
Device code	V_{IH}	X		1	0	1	1	1	0	1	0	BA

Note: X: Don't care, A9 = 12.0 V $\pm$ 0.5 V, A1 – A8, A10 – A15, $\overline{CE}$, $\overline{OE}$ = V_{IL} , $\overline{PGM}$ = V_{IH}

Electric Curves





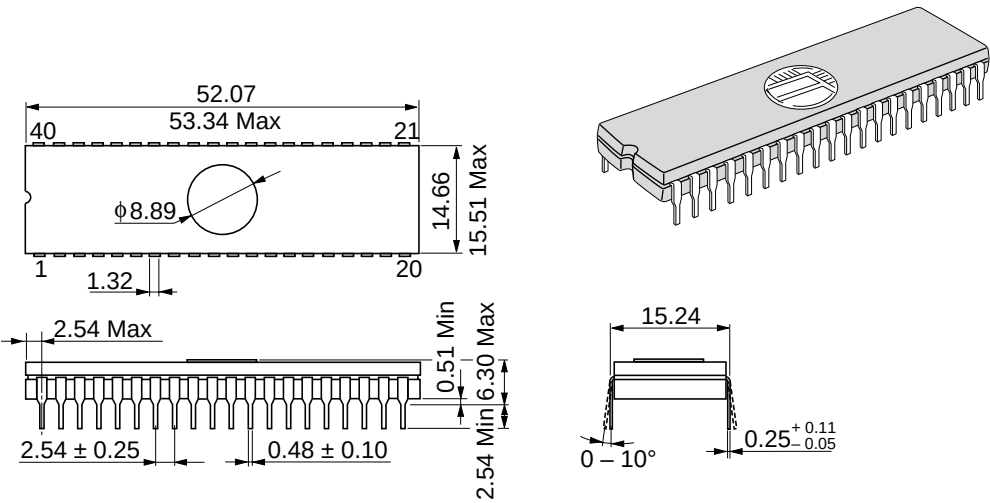


HN27C1024HG/HCC Series

Package Dimensions

HN27C1024HG Series (DG-40A)

Unit: mm



HN27C1024HCC Series (CC-44)

Unit: mm

