THE NEXT INTEGRATED-CIRCUITS OF THE 21ST CENTURY

Ahmad H. Tarakji, Ph.D
Senior Consultant – Semiconductor Device Physics & Process Integration

Related work:

- Ahmad Houssam Tarakji, Member, IEEE; A Simple Analytic Model of the FD SOI MOSFET that Captures Effects of High Bias and Body-Tied-Source. In Submission with the IEEE Trans. Elec. Dev., 2016 (underwent 1st initial review).
- Ahmad Tarakji; Approach for an Area-Efficient and Scalable CMOS Performance Based on Advanced Silicon-On-Insulator (SOI), Silicon-On-Sapphire (SOS) and Silicon-On-Nothing Technologies. U.S Patent application No. 14/821,685. Filed on 08/07/2015.
- Ahmad Tarakji; Precision Design-Rules to target Silicon Film thickness in FD-SOI/SOS/SON MOS for specific Gate-Length and Supply bias for optimal RF Power. In provisional filling with the U.S Patent and trademark office.
**THE DILEMMA:**

- The continuous downscaling of the semiconductor transistor over the past 30 years to meet competitive requirements for faster, more powerful and compact CPUs/RAMs caused it to approach its limiting “atomic” dimensions.
- Further improvements have become rather imposed by the laws of Physics and not by the technology itself.
- All efforts to circumvent this barrier for performance improvement on CPUs/RAMs are falling Nowadays in merging advancements in two categories:
  1. *Newer materials (SOI, SOS, GaAS, etc...), &*
  2. *Newer device structures (ex: FINFETs, GAAs, nanowire fabrics)*

This dilemma is mainly impacting the ICs targeting the low power high-performance computing (the computing power: CPUs/RAMs).

Components and ICs for the handheld wireless RF modules (ex: Components in Cellular phones), and the Semiconductor components for Power-Electronics are not being impacted by this downscaling constraint. (They rather require larger channel dimensions that permit the applications of their required higher potentials across their terminals).
OUTLINE:

- THE VARIOUS APPLICATIONS OF SEMICONDUCTORS
- BACKGROUND
- THE LOW-POWER ICs (CPUs, RAMs)
- RF MODULES FOR HANDHELD WIRELESS AND PORTABLE ELECTRONICS
- THE BEAUTY OF FULLY-DEPLETED SOI (FD-SOI)
- MOST ISSUES IN FD-SOI APPEAR FIXABLE (Some examples)
- CONCLUSIONS
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THE VARIOUS APPLICATIONS FOR SEMICONDUCTORS

Nanowire Biosensors
Operate at mV scale

Low-power ICs
Operate at 0.8–1.1V Supply (CPUs, RAMs)

Not being impacted by the downscaling constraint
(materials augmentations are boosting the performance)

Portable wireless handheld devices
Operate at 3–4V Supply (Cellulars)

Not being impacted at present by the downscaling constraint

High-power discrete & Integrated modules for Power-Electronics
Operate at 15–10,000V (Power-Supplies, Traction)
This all came to change with the introduction of the Semiconductor transistor in 1947.

(John Bardeen, Walter Brattain and William Shockley won the Nobel prize in 1956 for this discovery working at Bell Labs).

THE BEGINNING:

- THE VACCUM TUBES: Consumes tremendous “real estate”
  (18,000 Sq-ft of floor space for a 1 multiplier, 1 divider-square rooter and 20 adders)
- Consumes tremendous heat and is awfully energy-inefficient.
- Poor performance and reliability. (Vacuums often blew and required continuous on-going replacements).
The semiconductor transistor can be processed with lithography and chemistry, and can be manufactured with no manual assemblies.

This has permitted the continuous on-going downscaling of this first CPU chip, and with a corresponding decrease in its cost.
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BACKGROUND (the low-power ICs)

Moore’s Law:

The Continuation of Moore’s Law:

Source: Gordon E. Moore – Electronics, Vo. 30, No. 8, April 19, 1965.

First CPU on 1 chip

Intel 4004:
- First single-chip microprocessor.
- Introduced November 15, 1971
- Clock rate 740 kHz
- 0.07 MIPS
- Instruction set contained 46 instructions
- Number of Transistors 2,300 at 10 μm
- Addressable Memory 640 bytes
- Bus Width 4 bits (multiplexed address/data due to limited pins)
- Originally designed to be used in Busicom calculator

Source: Intel Corp.

“If we hadn’t shrunk the transistors, processor real-estate would be the size of Manhattan and would require 26 nuclear Power Plants to power it”.

Intel spokesman, Sean Maloney
The Continuation of Moore’s Law:

"...the trend cannot continue for ever, eventually miniaturization will lead to transistors that are the size of atoms. At that point the law cannot be sustained". Gorden E. Moore, 2005
What is next??  
(breaking the frontiers)

“...the principle of Moore’s Law will hold to be true for many decades; though we may have to abandon transistors, the principle of Moore’s Law may remain true”

Ray Kurzweil

Prototype of Quantum Computer:

The D-Wave Systems Computers:

What is next??

• Newer materials for conducting channels (Si/Ge, GaAs, etc...)
• Newer materials for substrates (SOI, SOS, SON, etc...)
• New structural designs (GAA, TFET, 3D nano-meshing, etc...)
• Quantum Computing (is probabilistic and not deterministic. May have limited applications).

WAY TO GO!!
What is next??

Low-power ICs

(breaking the frontiers)

- The advancements will rely mostly on significant shifts from the standard and conventional CMOS technology. (Newer never utilized prior technologies and processes may begin dominating the industry). A whole new Different Physics for the operating-modes of the devices will rule. Building-blocks of the ICs may need to be re-defined and designed differently.

- Companies that depended mostly on no other than the blind downscaling of the CMOS may end loosing their upper-hand in the industry. Newer Corporations, never heard of prior may suddenly emerge.

- Ex: IMEC is investigating the challenges to realize platforms for the N10 & N7 nodes and beyond, and have demonstrated some initial IV characteristics thus far - (Though still impractical!)

Source: Imec
**The next Integrated-circuits of the 21st Century**  
*Low-power ICs*

** Maneuvering the dilemma through Designs:**

- Parallel processing.
- 64Bits versus the 32Bits.
- Larger Cache
- Solid-State (Flash) Hard-drive versus magnetic.
- Graphical Processor Units (GPUs)
- Use of WiFi and Cloud-computing for parallel processing and data storage.

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Can provide boost in performance; but still do not deliver the closed-form fixes to continuously and steadily enhance the speed in clocking, in data synchronization, in data streaming and in Read/Write operations from Cache (SRAM).

The science of miniaturizing can still help. (More Speed, more Cache and more integrated functionalities).
Block-diagram of the HSDPA/WEDGE diversity radio subsystem:

**The issue in CellPhones PAs:**
- To deliver the necessary 0.8-1 Watts of transmitted RF power to Antenna, impedance transformation is required so to trade the low output voltage from the 3.5-4V Lithium-Batteries in CellPhones with higher current:
  
  \[ PL = C \times \frac{V_{amp}^2}{2 \times RL} \]

- Due to this requirement of higher current, GaAs devices are nowadays dominating the PA modules in CellPhones. (They possess higher Mobility and drift-Velocity).
- To implement PAs & RF-switches in CMOS, larger peripheries are required to meet the required higher current.

**Advantages of the SOI/SOS based CMOS over conventional CMOS are mainly its higher current, its lower Capacitive parasitic’s and its excellent Subthreshold characteristics.**

Furthermore, implementing PAs in CMOS technology may permit the full monolithic integration of the Analog RF with the Digital Baseband in a single compact Chip. That is the best part of it all!!
The next integrated-circuits of the 21st Century - RF modules for handheld wireless and portable electronics

**BUT WHY MOS PAs ANYWAY!?**

- May allow the full monolithic integration of RF Modules with the logic, memories and DSP (CMOS is a well-established and matured technology that can be integrated in dies at very extreme high densities) – More functionalities at lower cost.
- MOS is easily down-scalable (Moore’s Law). It can allow better control for scaling the bandwidth and cutoff frequencies.
- Ease of manufacturability in high-volumes. Higher yield & reliability: The CMOS process is solid and well-established. It matured steadily over a period of decades.
- Added boosts in performance will result if FD-SOI/SOS based CMOS can be used instead of conventional CMOS!

**THE BEAUTY OF FULLY-DEPLETED SOI (FD-SOI)!!**

A. Case of an Amplifier:

The reduced transport properties of CMOS (compared to GaAs) is countered with suppressed junction parasitic's that further push the performance.

To improve performance lower capacitive parasitic’s are required!
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RF modules for handheld wireless and portable electronics

THE BEAUTY OF FULLY-DEPLETED SOI (FD-SOI)!!

B. Case of a CMOS (Class D, E & F Amplifiers):

In FD-SOI/SOS, Junction Capacitances are suppressed, therefore enhancing the switching Speed!

A drastic gain results from the suppressed junction parasitic’s!!
THE BEAUTY OF FULLY-DEPLETED SOI (FD-SOI)!!

Excellent Subthreshold Characteristics!

- Thick high-quality BOX is usually required for best suppression of junction parasitic’s, and for the low $C_{eq}$ and good SS.
- Ultra thin Silicon film is generally required for good coupling between Back- and Front- Gates.
In larger-periphery structures, the FD-SOI is demonstrated to have clear superior performance to FINFET. This may be attributed to the suppression of junction parasitic's that scale with the device width.

Source: Valeriya Kilchytska et. al; ICTEAM Institute, Universite Catholique de Louvain

Source: International Technology Roadmap for Semiconductors (ITRS)
WHY NOT MULTI-LEG ARCHITECTURE TO SCALE CURRENT?

- Large-periphery Multi-Leg device is known to increase Gate-to-Body cap. \(^1\) as well as Gate-to-Drain and Gate-to-Source overlap cap. \(^2\) – Included are Multi-Leg designs based on SOI \(^3\). These severely degrade the RF performance.

The idea is to minimize the number of Legs to the extent possible while targeting largest width per Leg.

WHY NOT FINFETs?

- Aside from the fact that Single-Leg larger-periphery devices demonstrate in FD-SOI superior characteristics to FINFETs, both the single-Leg and the Multi-Leg FINFETs have higher Capacitive Parasitic’s due to the three-dimensional nature of their structures \(^3, 4\).

Some known Issues in FD-SOI:

1. Supply-bias Limitation

The device operates with its lateral Barrier already lowered due to Full-depletion of its Body. This poses strong constraint on the maximum applicable Supply bias to its Drain as the undesired Diffusion-current can dominate the performance, or even latch-up.

→ To apply the required (for Cell PAs) 3.5-4V Supply bias to the Drain, longer channels help lessening this barrier lowering.
This impacts both the Drive current and the Bandwidth.

(FIX:)

Highly doped pockets at the Gate edges (HALOs) can permit reducing the channel lengths for same Supply-bias. The VT can be least impacted when the lateral dimensions of these pockets are relatively small compared to the Gate-Length.

(Note: in Logic and in Memories that operate around the 1V Drain bias, longer channels and HALOs are not critical as the weaker lateral field gets deflected from the transversal field caused from the application of a comparable bias to the Gate. (1-2V)
Some Known Issues in FD-SOI:

2. Stabilizing the VT with varying Supply bias.

The device is designed such that most of its Body region is depleted at the target DC Supply bias for its operation ($V_{D\text{max}}$). Only one HALO pocket at Source-side remains partially un-depleted so to suppress the Diffusion-current to the extent possible. As this Supply bias reduces due to Output Swing, un-depletion in Body does occur. This can shift the VT when no structural optimization is performed.

**FIX:**

An ultra-thin Body with well-engineered Work-functions can ensure that most Body depletion is caused due to the Work-functions alone. This reduces the effect of the lateral field on Body depletion, and hence on the VT.

The lateral dimensions of HALOs must still be significantly smaller than the Gate-Length.
Some Known Issues in FD-SOI!

### 3. Fields fringing due to thicker BOX.

Due to the large distance between substrate and Source/Drain junctions, the field in the BOX emanating from the Source/Drain depletion charge tends to terminate in the Si film channel and therefore inducing substantive inversion charge at the Back-surface. This impacts the SS.

The effect becomes pronounced in shorter Gate lengths with thicker BOX.

**THE FIX**

The classical fix in the short-channels devices that operate around a 1V Supply (for low power Logic & RAM) is through thinning the BOX such to reduce the fringing effect.

In the longer Channel devices incorporating HALOs, this fringing effect is generally not an issue.

Source: Applied Materials
Some Known Issues in FD-SOI

4. Floating Body Effect due to incorporation of HALO.

Ideally a FD-SOI does not have Floating Body effect because its lateral barrier is already lowered due to Full-Depletion of its Body.

However in Devices incorporating HALOs so to permit the applications of higher Supply biases, the Floating Body still exists due to the partial depletion of the one HALO pocket at the Source-side.

This requires the incorporation of a Body-Tied-Source such to prevent this effect.

The effect can be totally eliminated given that no voltage equaling or higher than the typical Diode-drop gets developed across this Source-Side HALO from the conduction of Impact-Ionization Current.
Some Known Issues in FD-SOI!

4. Floating Body Effect due to HALO, & The Area-Efficient Scalability.

Top Layout View of a Larger-Periphery Single-Leg Structure

The Device can be scaled with more BTS to meet its target (or its desired drive current)

Design-Rule for Area Efficiency:

$$\frac{1}{2} \times \frac{I_b}{n} \times \frac{1}{q \times \mu \times \text{conc}_\partial} \times \frac{\text{SPAC}}{(W_p - x_p)(t_{si} - W_m)} \leq 0.5V$$

If the above Design-Rule is not followed, devices may not meet their target Drive currents within their specified footprints in their IC layout. To meet their target currents then, they will need to have their Peripheral widths parasitically and drastically increased due to added unnecessary BTS stripes.

TCAD Simulation (Drive Current) of an Area-inefficient design
Conclusions:

- Only the low-power ICs intended for the performance computing and the Memories appear impacted at present by the trend of Moore’s Law.
- MOS devices intended for the RF PAs and the RF-switches in CellPhones are as of today still not impacted by this trend as they generally utilize longer channels (> 100nm !) so to help support the applications of their higher Supply biases.
- FD-SOI appears to offer excellent opportunity for the designers from the experimental data available.
- Most known issues that associate with the FD-SOI are fixable as was demonstrated through some of the examples included in this presentation.
- For the larger-periphery devices that are intended for higher drive currents and higher Supply biases, the FD-SOI MOS appears to be clearly superior to FINFETs.

THANK YOU !!