Wideband High Power GaN on SiC SPDT Switch MMICs
Charles F. Campbell and Deep C. Dumka
TriQuint Semiconductor, Richardson, TX, 75080

Abstract — The design and performance of three wideband SPDT switch MMICs utilizing GaN on SiC technology are presented. The circuits are designed to cover frequency ranges of DC-6 GHz, DC-12 GHz and DC-18 GHz with input power handling optimized over the specified bandwidth. Measured in-fixture s-parameter data demonstrates a maximum insertion loss of 0.7 dB, 1.0 dB and 1.5 dB, respectively for the 6 GHz, 12 GHz and 18 GHz designs. Measured continuous wave power data demonstrates typical input RF power handling of 40 W, 15 W and 10 W, respectively for the 6 GHz, 12 GHz and 18 GHz MMICs.

Index Terms — Switch, MMIC, high power, Gallium Nitride, Silicon Carbide

I. INTRODUCTION

The electrical and thermal properties of Gallium Nitride (GaN) on Silicon Carbide (SiC) HEMT technology are well suited to high power control circuit applications, offering many advantages over existing GaAs technology. The greatly increased breakdown voltage ($V_{BD}$) will allow the use of higher control voltage and correspondingly larger RF voltage swings for off-state transistors. High maximum current capability ($I_{max}$) reduces channel resistance and increases RF current swing for on-state devices. The insulating SiC substrate reduces substrate leakage due to high RF voltage swing and improves heat transfer to the backside of the MMIC.

Significant work has been published investigating various GaN based technologies for high power microwave switch applications [1-4]. M. Yu, et al. demonstrated 20 W $P_{SLIAB}$ and 1.4 dB of insertion loss at L-band for a SP4T hybrid switch design. M. Hangai, et al. presented results for a SPST circuit achieving 1.0 dB of insertion loss and 100 W power handling at S-band. B. Y. Ma, et al. published results for a monolithic Ku-band design that demonstrated 1.4 dB of insertion loss and 4 W $P_{SL}$ at 18 GHz. An example of a wideband topology was published by A. Koudymov, et al. demonstrating DC-6 GHz bandwidth, less 1 dB insertion loss and 5 W power handling.

This paper discusses the design and performance of three wideband, high power SPDT switch MMICs that utilize the TriQuint Semiconductor GaN on SiC process. The circuits are designed to cover three different frequency ranges, each optimized for power handling over the respective design band. The paper is organized as follows; characteristics of a switch FET test structure are reviewed to determine the optimum FET cell configuration. Next, design and analysis of the switch MMICs is discussed including the circuit simulation methodology. Finally, measured in-fixture s-parameter and continuous wave power handling data for the fabricated MMICs is presented.

II. GAN SWITCH FET CHARACTERISTICS

General information regarding the TriQuint Semiconductor production GaN process has been published elsewhere [5] and will not be repeated here. Transistor characteristics pertinent to high power switching applications are as follows. Typical 1mA/mm pinch-off voltage ($V_{P}$) for the process is -4.2 V and maximum drain current ($I_{max}$) tested at $V_{d}=10$ V and $V_{gs}=1.5$ V is 1.07 A/mm. Typical reverse 2-terminal breakdown voltage is greater than 80 V at $I_{gd}=5$ mA/mm for the dual field plate configuration.

To investigate the characteristics of GaN transistors configured for switch applications a test structure was fabricated and characterized. The 5x60 μm single field plate device features a centered gate, symmetric layout with respect to the source/drain and was built with 2 μm, 3 μm, 4 μm and 6 μm source drain spacing. The transistor is in a common gate configuration and a 3 kΩ gate resistor is used to decouple the circuit from the common gate ground. Since the gate is grounded, the devices are biased by applying a positive voltage simultaneously to the source and drain ($V_{d}=0$ V) through the network analyzer bias ports. Linear s-parameters were collected on-wafer for the test structure over a range of gate bias voltages.

On-state resistance and off-state capacitance extracted from the s-parameter data at 2.1 GHz are summarized in Table 1 [6]. The on-state resistance data as a function of source drain spacing suggests a contact resistance of 0.6 Ω-mm and 285 Ω/sq. sheet resistance for the channel. This agrees well with 0.5 Ω-mm and 300 Ω/sq. obtained from DC measurements of process control structures. The off-state capacitance reduces with increasing gate bias voltage and is not a strong function of source-drain spacing. Note that the typical breakdown voltage for each source-drain spacing is also shown in Table 1.

<table>
<thead>
<tr>
<th>Gate Bias</th>
<th>Switch Parameter</th>
<th>Source-Drain Spacing (um) - $V_{ad}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V</td>
<td>$R_{on}$ (Ω-mm)</td>
<td>1.770 2.121 2.421 2.923</td>
</tr>
<tr>
<td>-10 V</td>
<td>$C_{ds}(pF/mm)$</td>
<td>0.267 0.265 0.264 0.260</td>
</tr>
<tr>
<td>-20 V</td>
<td>$C_{ds}(pF/mm)$</td>
<td>0.219 0.218 0.218 0.214</td>
</tr>
<tr>
<td>-30 V</td>
<td>$C_{ds}(pF/mm)$</td>
<td>0.188 0.187 0.186 0.182</td>
</tr>
<tr>
<td>-40 V</td>
<td>$C_{ds}(pF/mm)$</td>
<td>0.170 0.169 0.168 0.164</td>
</tr>
</tbody>
</table>

Table 1. GaN switch FET equivalent circuit parameters.
For a symmetric structure with $V_d = 0\ V$, the RF power handling (1) for an off-state FET switch is maximized for the gate bias voltage centered between the breakdown and pinch-off voltage for the process.

$$
P_{\text{off} \text{max}}(W) = \frac{(V_{\text{ad}} - V_p)^2}{2Z_0}
$$

Therefore, a trade-off exists between on-state resistance and RF power handling as a function of source-drain spacing. For example, assuming $V_p = -5.0\ \text{V}$ (1) predicts 12.3 W of maximum off-state power handling for the 2 $\mu$m source-drain spacing device at a gate bias of -22.5 V. For a transistor with a 4 $\mu$m source-drain spacing the projected off-state RF power handling increases to 42.3 W at -37.5 V gate bias. Assuming that required control voltage is available, the over 3x improvement in power handling for the 4 $\mu$m source-drain device is likely worth the 25% increase in on-state resistance. A 4 $\mu$m source-drain spacing is also compatible with production released TriQuint Semiconductor GaN/SiC process and was therefore selected for the MMIC designs described in the remainder of this paper.

### III. CIRCUIT DESIGN

To demonstrate the use of the GaN/SiC process for switch applications three experimental MMICs were designed and fabricated. All three circuits are configured as SPDT switches utilizing the wideband reflective series-shunt-shunt topology shown in Fig. 1. The designs target the following frequency bands; DC-6 GHz, DC-12 GHz and DC-18 GHz, and are optimized for maximum power handling.

Due to the lack of a suitable nonlinear transistor model extracted at $V_d = 0\ \text{V}$, a linear analysis approach was used to estimate RF power handling. Within the simulation tool voltage and current probes were placed at the terminals of the linear 3-port transistor model. A nonlinear harmonic balance source was then applied to the common port of the circuit model. For a given input power level the RF current swing from source to drain and the RF voltage swing across the gate-source and gate-drain junctions could be observed for every transistor in the circuit. The RF input power was then increased until one of the compression mechanisms was observed, either RF current swing in excess of $I_{\text{max}}$ or RF voltage swing exceeding pinch-off or breakdown. The circuit was then optimized to maximize the input power level. This technique can also be used to estimate power dissipation and junction temperatures for the transistors. The method proved useful for optimizing the design for maximum power handling, although likely less accurate for predicting actual power and compression levels. Estimated power handling and worst case power dissipation is shown in Fig. 2 and Fig. 3 respectively for the DC-6 GHz design.

![Fig. 1. Wideband SPDT switch MMIC topology.](image1)

![Fig. 2. Power handling simulation for the 6 GHz SPDT switch.](image2)

![Fig. 3. Estimated worst case power dissipation for the 6 GHz SPDT switch.](image3)
limiting due to pinch-off or breakdown. As shown in Fig. 3, at low frequency the series FET Q3 in the transmission arm has the highest power dissipation. However, at the upper band edge RF power starts leak through Q4 and is dissipated in Q5. Above 6 GHz FET Q5 is actually predicted to dissipate more power than Q3.

The transistor sizes and transmission line lengths were optimized with the AWR™ circuit simulation tool and the designs were finalized with EM simulation utilizing Sonnet™. Photographs of the fabricated MMICs are shown in Fig. 4. All three die are the same size, 1.15x1.66mm².

Fig. 4. Die photographs of the fabricated 6 GHz, 12 GHz and 18 GHz SPDT switch MMICs.

IV. MEASURED PERFORMANCE

Singulated die were soldered to Cu-Moly carrier plates for in-fixture testing. Alumina 50 Ω transmission lines are connected to the RF ports of the MMIC with two ~20 mil long bond wires. The calibration procedure de-embeds the effect of the alumina lines from the data placing the reference plane where the bond wires attach to the alumina lines. Small signal s-parameter data was collected in an open (non cut-off) environment for a -40 V gate bias condition. Therefore, bond wire to bond wire radiation will have some effect on the isolation measurements. Measured small signal s-parameter results for insertion loss and return loss are plotted in Figs. 5-7. For reference, simulated data for the insertion loss is included in the plots as the dashed trace and very good agreement with experiment was observed for all three designs. The DC-6 GHz design has -0.3 dB of low frequency insertion loss which increases to about -0.7 dB at 6 GHz. Measured common and switched port return loss is typically better than -20 dB over the design band of the MMIC. The DC-12 GHz and DC-18 GHz designs demonstrate worst insertion losses of about -1.0 dB and -1.5 dB respectively. The measured common and switched port return loss was observed to be better than -12 dB for both designs.

The isolation for the off-state arm was measured to better than -30 dB for the 6 GHz and 12 GHz MMICs. The 18 GHz MMIC had better than -30 dB of isolation up to about 16 GHz, degrading to -25 dB at 18 GHz.

Fig. 5. Measured small signal insertion loss and return loss for the DC-6 GHz SPDT switch MMIC.

Fig. 6. Measured small signal insertion loss and return loss for the DC-12 GHz SPDT switch MMIC.

Fig. 7. Measured small signal insertion loss and return loss for the DC-18 GHz SPDT switch MMIC.
Continuous wave (CW) power compression results are plotted in Figs. 8-10. Sufficient drive power was not available to cover the entire design band of the circuits. The results are therefore shown over only a portion of operating bandwidth of each MMIC. The power handling analysis described in the first part of this paper estimated about 40 W of input power handling for the DC-6 GHz design. The measured data shown in Fig. 8 demonstrates less than 0.3 dB of compression for 40 W incident RF power between 1 GHz and 4 GHz. The 12 GHz design demonstrates about 15 W of power handling up to about 9 GHz, degrading to 10-12 W between 10 GHz and 12 GHz. A similar trend was observed for data collected on the 18 GHz design. The results suggest about 10 W of power handling up to 14 GHz, reducing to about 8 W at 18 GHz. Curiously, both the 12 GHz and 18 GHz MMICs produced somewhat anomalous results at 10 GHz. Both parts were tested with same set up and calibration suggesting that there may have been an equipment issue at 10 GHz. Otherwise, the authors do not yet have an explanation for the soft compression characteristic observed at 10 GHz.

V. CONCLUSION

The design and performance of wideband SPDT switch MMICs utilizing GaN on SiC process technology have been presented. To the best knowledge of the authors these switch MMICs demonstrate state of the art performance with regard to insertion loss, bandwidth and RF power handling. The results presented here strongly suggest that GaN transistor technology is well suited to high power RF switching applications.

REFERENCES