Abstract

This paper presents a new design technique for three-stage CMOS Operational Amplifier (opamp) with Nested Miller Compensation (NMC) scheme. This design technique is suitable for power optimization with fast settling. In this paper the characteristic of on-chip opamp (i.e. load is capacitive and known in advance) is exploited to obtain the best power and settling performance. NMC scheme has been improved for power optimization after carrying out analysis of power requirement for pole-zero placements. In the proposed design technique compensation resistance (Rc) is used to place poles and zeros at appropriate location so power can be optimized with minimum settling time. NMC capacitor sizing methods are found out on basis of appropriate placements of poles and zeros. In order to achieve required settling performance and optimum power consumption combination of ratio of transconductances of all three stages and ratio of load capacitor to compensation capacitors have been established. Validity of the proposed design technique has been checked by simulation using Tanner tool in 0.35 μm CMOS technology. Simulation results obtained are Slew rate (SR) = 5.76 V/μs, Unity-gain frequency = 8 MHz, Phase margin = 64° and DC gain = 120 db." Is required to be modify as “Simulation results obtained are Slew rate (SR) = 5.76 V/μs, Unity-gain frequency (fu) = 8 MHz, Phase margin = 64° and DC gain = 120 db.
Introduction

In modern low voltage CMOS technology, it is a major challenge to design low power fast settling opamps. Due to large headroom requirement gain enhancement techniques like cascade or telescopic is not suitable for low voltage applications. So multistage amplifiers are used in low voltage applications. The most challenging part in the multistage opamp designing is the frequency compensation. NMC and reversed nested miller compensation are two compensation techniques used in three-stage opamp. Multipath nested miller compensation structure was proposed by eschauzier [1]. This structure is suitable for bipolar transistors because of its high transconductance requirement. NMC method was improved in [2] by using feed forward transconductance stage and nulling resistor. A novel opamp design technique using NMC is presented in [3] and the use of nulling resistors to remove the right hand plane zeros was discussed. NMC methods presented in [1]- [3] have considered the compensation capacitor sizing criterion based on achieving the third order butterworth response from the opamp in unity-feedback configuration. Damping factor oriented compensation capacitor sizing rules were developed in [4]. These rules are useful to design the opamp with fast settling and low power. Design procedure for three stage opamp with NMC, suitable for pencil-and-paper design was given in [5] [6]. These procedures have not given much consideration to settling time parameter. Effect of load capacitor on design parameters is also not considered. Little work has been reported in literature [7] [8] for settling time analysis of multistage opamp. Pugliese [8] has developed a design procedure for three stage NMC amplifiers with a feature of fast settling and low power. An accurate analysis of Dynamic Settling Error (DSE) \( \xi_{dyn}(t) \) is presented by Marques [7]. Work done in [7] has been extended in this paper to develop the new criterion for deciding the size of the compensation elements (capacitors and resistor). Power constraint is taken under consideration to decide the size of the compensation elements and values of transconductances for achieving minimum settling time.

DSE parameters for three stage opamp

In this section, accurate relationships between circuit parameters (transconductances of different stages, compensation capacitors and load capacitor) and DSE \( \xi_{dyn}(t) \) parameters have been established. Parameters (damping factor, damping frequency and natural frequency of oscillation) of quasi-linear period of the settling time can be derived from the small signal model of the three-stage opamp with NMC. Block diagram and small signal model for three stage CMOS opamp with NMC are shown in figure 1 and figure 2 respectively [2][3].
Here $g_{m1}$, $g_{m2}$ and $g_{m3}$ are transconductances and $r_{o1}$, $r_{o2}$ and $r_{o3}$ are output resistances of the first, second and third stages of opamp. $R_c$, $C_{c1}$ and $C_{c2}$ are the compensation resistance and capacitors respectively. $C_{o1}$ and $C_{o2}$ are the parasitic capacitors at first and second stage respectively and $C_L$ is load capacitor. Figure 1 shows that $C_{c1}$ and $C_{c2}$ are connected across the gain stages, due to the miller effect, miller equivalent values of $C_{c1}$ and $C_{c2}$ will be in parallel to the $C_{o1}$ and $C_{o2}$. Hence $C_{o1}$ and $C_{o2}$ can be neglected because of their low values as compared to miller equivalent of $C_{c1}$ and $C_{c2}$. Transfer function of three stage opamp shown in figure 2 can be expressed as:

$$A(s) = A_o \frac{1 + \left( R_c C_{c1} + \left( R_c - \frac{1}{g_{m3}} \right) C_{c2} \right) s + \left( \frac{g_{m3} R_c - 1}{g_{m2} g_{m3}} \frac{C_{c1} C_{c2}}{} \right) s^2}{\left[ 1 + \frac{s}{\Omega_{p1}} \right] \left[ 1 + \frac{1}{g_{m2}} - \frac{1}{g_{m3}} \right] C_{c2}s + \frac{1 - g_{m2} R_c}{g_{m2} g_{m3}} C_{c2} C_L s^2}$$

(1)

Here, $\Omega_{p1}$ is pole frequency of first stage. $A(s)$ open loop gain and $A_o$ is dc gain. Under open loop condition transfer function of generic third order system can be given as [7].
Here $\omega_{z_1}$ and $\omega_{z_2}$ are the zeros. $\xi_o$ and $\omega_{no}$ are the damping factor and natural frequency of oscillation respectively under open loop condition. By applying miller effect on $C_{c_1}$, Unity gain frequency ($\omega_u$) can be given as [9].

$$f_u = \frac{g_{m1}}{C_{c1}} \times \frac{1}{2\pi}$$

(3)

Here $f_u$ can also be given as: $f_u = A_u \times \omega_{p1} \times \frac{1}{2\pi}$ and $f_u = \frac{\omega_u}{2 \times \pi}$.

By the comparison of equations (1) and (2), $\omega_{no}$ and $\xi_o$ can be given as:

$$\omega_{no} = \sqrt{\frac{g_{m2} \times g_{m3}}{(1 - g_{m2} R_c) C_c \times C_L}}$$

(4)

$$\xi_o = 0.5 \times \left[ \frac{g_{m3} - g_{m2} \times \sqrt{C_c \times C_L \times \frac{1}{\sqrt{1 - g_{m2} R_c}}}}{g_{m3} \times g_{m2}} \right]$$

(5)

Setting performance of generic third order system can be expressed by $\xi_{dyn}(t)$. $\xi_{dyn}(t)$ can be given as [7]:

$$\xi_{dyn}(t) = 20 \times \log_{10} \left( a \times \exp(-\omega_d t) + b \times \exp(-\xi \omega_d t) \times \text{sign}(q) \times \sin \left( \sqrt{1 - \xi^2} \times \omega_d t + \tan^{-1} \left( \frac{p}{q} \right) \right) \right)$$

(6)

Here $\omega_n$, $\omega_d$ and $\xi$ are natural frequency of oscillation, damped frequency of oscillation and damping factor respectively for closed loop third order system. Constants $a$, $b$, $p$ and $q$ in equation (6) can be given as:

$$a = \frac{1 - \frac{\omega_d}{\omega_n}}{K_1} \left( 1 - \frac{\omega_d}{\omega_{z_2}} \right)$$

(7)

$$b = \sqrt{p^2 + q^2}$$

(8)

$$p = A_u \left( \frac{\omega_d}{\omega_n} \right)^2 - 2 \times \xi \times \frac{\omega_d}{\omega_n} + \frac{\omega_d}{\omega_{z_1}} + \frac{\omega_u}{\omega_{z_2}} - \frac{\omega_d}{\omega_n}$$

(9)
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\[ q = A_n \left( \frac{\omega_n}{\omega_h} \left( 1 - \frac{\omega_d}{\omega_n} - \frac{\omega_d^2}{\omega_n^2} \right) + \xi \left( \frac{\omega_n}{\omega_h} \right)^2 + \frac{\omega_d}{\omega_n} + \frac{\omega_d^2}{\omega_n^2} - \frac{2 \xi \omega_d}{\omega_n} \right) \times \left( \sqrt{1 - \xi^2} \right) \]  

(10)

In equations (7), (9) and (10), \( K_1 \) is given as: \( K_1 = 1 + \left( \frac{\omega_d}{\omega_n} \right)^2 - 2 \xi \times \frac{\omega_d}{\omega_n} \).

Relationship between open loop and closed loop parameters of the quasi-linear period of the settling time can be given as [7]:

\[ \omega_n = \frac{\omega_d}{\sqrt{K_2}} \]  

(12)

\[ \xi = \xi_n \times \sqrt{K_2} - 0.5 \times \frac{\omega_d}{\omega_n} \times \left( 1 - \frac{\omega_n^2}{\omega^2} \right) \]  

(13)

In equations (11), (12) and (13), \( K_2 \) is given as:

\[ K_2 = 1 + \frac{2 \xi \omega_d}{\omega_n} - \frac{\omega_d}{\omega_n} \left( \frac{\omega_d}{\omega_n} + \frac{\omega_d}{\omega_n} \right) \]  

(14)

Equations (3) to (6) and (11) to (13) give the relationship between settling time and circuit parameters. Marque [7] has concluded in his work that when zeros have low frequency, settling time can be improved by following conditions.

i. By maximizing the \( \omega_n \).

ii. By keeping \( \xi \) close to unity.

iii. By making \( \xi \times \omega_n \) just above to \( \omega_d \).

To satisfy condition (iii), following equation (15) can be derived by using the equations (11) to (13).

\[ 1.05 \times \omega_n \times K_2 = \xi_n \times \omega_n + 0.5 \times \omega_n \times K_2 \times \left( 1 - \frac{\omega_n^2}{\omega_n \omega^2} \right) \]  

(15)

To satisfy conditions (ii) and (iii), \( \xi = 0.9 \) and \( \xi \times \omega_n = 1.05 \times \omega_d \) can be assumed respectively. So, \( \omega_n / \omega_d \) can be given as:

\[ \omega_n / \omega_d = 1.16 \]  

(16)
Power Dissipation (PD) in three-stage opamp

PD in generic three-stage opamp with differential amplifier as a first stage can be given as:

\[ PD = (2 \times I_{D1} + I_{D2} + I_{D3}) \times V_{DD}. \]  

(17)

Basic relationship between transconductance and bias current in case of opamp can be given as:

\[ g_m = \frac{1}{2} I_D / V_{eff} \]  

(18)

Here \( I_{D1} \), \( I_{D2} \) and \( I_{D3} \) are biasing currents of first, second and third stage of the opamp respectively.

\( V_{DD} \) is supply voltage and \( V_{eff} \) is driving voltage of transistor.

From the equations (17) and (18), PD can be given as:

\[ PD = 0.5 \times (2g_{m1} + g_{m2} + g_{m3}) \times V_{DD} \times V_{eff} \]  

(19)

Here, it is assumed that driving voltages of all three stages are same i.e. \( V_{eff} = V_{eff\,1} = V_{eff\,2} = V_{eff\,3} \). Therefore, value of transconductances directly affects the PD. For the analytical analysis, in this paper PD is calculated by assuming \( V_{DD} = 2 \) V, \( V_{eff} = 180 \) mV and \( g_{m1} = 13.8 \mu A/V \) for a noise \( (S_{f\,n}(f)) \) constraint of \( 40 nV/\sqrt{Hz} \) as \( S_{f\,n}(f) \approx 16/3 \times (kT/g_{m1,2}) \). Here \( k \) is boltzman constant and \( T \) is temperature in Kelvin.

Ratio of transconductances

Most challenging part in three stage CMOS opamp design is to find out optimum ratio of transconductances at different stages. In earlier design techniques [1], [3] transconductance of third stage is assumed to be very large to simplify the design method. In low power CMOS opamp design such assumptions will not be applicable. Commonly circuit designers use simulation tools to find out optimum values of transconductance. Such methods are not more accurate. Higher transconductances at second and third stage are needed to shift the poles at higher value than \( \omega_p \). In this section analysis of relationship between transconductance and location of poles is done to find out the optimum value of transconductances.

In equation (1), because of miller effect first pole frequency \( (\omega_{p1}) \) is at very low value so it will not affect the stability of the opamp. Second pole frequency \( (\omega_{p2}) \) and third pole frequency \( (\omega_{p3}) \) are required to be placed above \( \omega_p \) for the stability of the opamp in closed loop. From equation (1), \( \omega_{p2} \) and \( \omega_{p3} \) can be given as:
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$$\omega_{p2} = \frac{b}{2a} \left[ -1 + \sqrt{1 - \frac{4a}{b^2}} \right]$$  \hfill (20)

$$\omega_{p3} = \frac{b}{2a} \left[ -1 - \sqrt{1 - \frac{4a}{b^2}} \right]$$  \hfill (21)

In equations (20) and (21), \( \frac{b}{2a} \) and \( \frac{4a}{b^2} \) can be given as:

\[
\frac{b}{2a} = 0.5 \times \left[ \frac{\left( \frac{g_{m1}}{g_{m2}} - 1 \right) \times C_{c2}}{1 - g_{m2}R_C} \right]
\]  \hfill (22)

\[
\frac{4a}{b^2} = 4 \times \left[ 1 + \left( \frac{g_{m1}}{g_{m2}} \right)^2 - 2 \times \left( \frac{g_{m3}}{g_{m2}} \right) \right]
\]  \hfill (23)

From the equations (20) to (23), it can be observed that ratio of transconductance \( \frac{g_{m1}}{g_{m2}} \) decides the location of the pole \( \omega_{p2} \) and \( \omega_{p3} \) at higher value than \( \omega_n \). From equation (20) and (21) it can be observed that shifting of \( \omega_{p2} \) at higher value is crucial issue. Therefore, shifting of \( \omega_{p2} \) is considered for analysis purpose. Using equations (20) to (23) variation of normalized pole with circuit parameters is shown in figure 3. It can be observed from figure 3 that as \( \frac{g_{m3}}{g_{m2}} \) increases pace of shifting of \( \omega_{p2} \) reduces. Separation between curve 1, 2 and 3 is more as compared to separation between curve 4, 5 and 6. Poles can be shifted efficiently for a value of \( \frac{g_{m3}}{g_{m2}} = 4 \). Further increase in \( \frac{g_{m3}}{g_{m2}} \) will not shift the poles effectively. So the optimum value of \( \frac{g_{m3}}{g_{m2}} \) will be 4 and by using this value in equation (19) power constraint will set the value of \( \frac{g_{m2}}{g_{m1}} \). Here pole is normalized with \( g_{m1}/C_{c2} \).
Figure 3: Normalized pole $|\frac{\omega}{p_2}|$ for different values of compensation capacitor.

Compensation resistance
Equations (20) to (23) are used to show the variation of normalized poles with $C_{c2}$ for different values of normalized $Rc$ (i.e $R_c g_{m2}$).

Figure 4: Normalized poles for different values of compensation capacitor.

It can be seen from figure 4 that for the value of $R_c g_{m2}$ greater than unity, pole $\omega_{p_3}$ is located in right hand plane, which will make the system unstable. So $R_c g_{m2} \geq 1$ is not an applicable value. Further, it can be observed that for $R_c g_{m2} = 0.95$, one complex pole is there and for $R_c g_{m2} = 0.9$, three complex poles are there. So as $R_c g_{m2}$ decreases below the unity, number of complex poles increases. Because of this range of $C_{c2}$ provides the real poles reduces. Hence, $R_c g_{m2}$ should not be more than unity as well as it should not be very less than unity.
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Placement of zeros and poles
From equation 1, \( \omega_{z1} \) and \( \omega_{z2} \) can be given as:

\[
\omega_{z1} = \frac{b}{2a} \left[ -1 + \sqrt{1 - \frac{4a}{b^2}} \right]
\]

(24)

\[
\omega_{z2} = \frac{b}{2a} \left[ -1 - \sqrt{1 - \frac{4a}{b^2}} \right]
\]

(25)

Where, \( \frac{b}{2a} \) and \( \frac{4a}{b^2} \) can be expressed as:

\[
\frac{b}{2a} = 0.5 \times \frac{g_{m2}}{C_{c1}} \left( \frac{C_{c1}}{C_{c2}} \times \frac{g_{m3}R_c}{(g_{m3}R_c - 1)} + 1 \right)
\]

(26)

\[
\frac{4a}{b^2} = 4 \times \frac{g_{m3}}{g_{m2}} \times \frac{(g_{m3}R_c - 1) \times C_{c1}}{C_{c2}} - \frac{(g_{m3}R_c)^2 \times \left( \frac{C_{c1}}{C_{c2}} \right)^2 + 2C_{c1}}{C_{c2}} + 1 - 2g_{m3}R_c \times \left( \frac{C_{c1}}{C_{c2}} + 1 \right)
\]

(27)

Shifting behavior of zeros is analyzed by considering the specific case of opamp designing with following specifications. \( \omega_{u} = 10 \text{ MHz} \), power budget of 100 µW, noise = 40 nV/√Hz. \( g_{m3}/g_{m2} = 4 \) and \( R_c g_{m2} = 0.95 \) can be assumed based on discussions in section 4 and section 5. Further, \( g_{m1} = 13.8 \mu A/V \) and \( C_{c1} = 0.22 \text{ pf} \) can be found out from section 3 and equation (3). For the given power budget, from equation (19) \( g_{m2}/g_{m1} \) can be found out equal to 6.37. Using equations (20) to (23) and (24) to (27) variation of poles and zeros is shown in table 1.

Table 1: Normalized values of poles and zeros for different circuit parameters with 10 pf load.

<table>
<thead>
<tr>
<th>( C_{c1} )</th>
<th>( \frac{g_{m1}}{g_{m2}/C_{c1}} )</th>
<th>( \frac{g_{m1}}{g_{m2}/C_{c1}} )</th>
<th>( \frac{g_{m3}}{C_{c2}} )</th>
<th>( \frac{g_{m3}}{C_{c2}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>-6.91944</td>
<td>-17.0396</td>
<td>-1.42 + j0.53</td>
<td>( \rho = 0.99 )</td>
</tr>
<tr>
<td>0.3</td>
<td>-6.1454</td>
<td>-15.058</td>
<td>-1.16 + j1.24</td>
<td>( \rho = 0.94 )</td>
</tr>
<tr>
<td>0.5</td>
<td>-5.9675</td>
<td>-17.3083</td>
<td>-2.47 + j1.28</td>
<td>( \rho = 0.95 )</td>
</tr>
<tr>
<td>0.7</td>
<td>-2.77217</td>
<td>-6.0792</td>
<td>-1.8348</td>
<td>-3.71692</td>
</tr>
<tr>
<td>0.9</td>
<td>-2.1292</td>
<td>-6.1598</td>
<td>-1.6003</td>
<td>-5.35997</td>
</tr>
<tr>
<td>1.1</td>
<td>-1.78834</td>
<td>-6.1949</td>
<td>-1.9663</td>
<td>-7.9137</td>
</tr>
<tr>
<td>1.3</td>
<td>-1.59968</td>
<td>-6.21767</td>
<td>1.453</td>
<td>-8.847</td>
</tr>
<tr>
<td>1.5</td>
<td>-1.18112</td>
<td>-6.2399</td>
<td>-1.21792</td>
<td>-10.5835</td>
</tr>
<tr>
<td>1.7</td>
<td>-1.11204</td>
<td>-6.44664</td>
<td>-1.3926</td>
<td>-12.2074</td>
</tr>
<tr>
<td>1.9</td>
<td>-0.99531</td>
<td>-6.2525</td>
<td>-1.3425</td>
<td>-13.8286</td>
</tr>
<tr>
<td>2.1</td>
<td>-0.8997</td>
<td>-6.2971</td>
<td>-1.3611</td>
<td>-15.4399</td>
</tr>
<tr>
<td>2.3</td>
<td>-0.81829</td>
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<td>-1.34899</td>
<td>-17.0511</td>
</tr>
<tr>
<td>2.5</td>
<td>-0.75042</td>
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<td>-1.34784</td>
<td>-18.6643</td>
</tr>
<tr>
<td>2.7</td>
<td>-0.69063</td>
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<tr>
<td>2.9</td>
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<tr>
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<tr>
<td>3.5</td>
<td>-0.53632</td>
<td>-6.26113</td>
<td>-1.3142</td>
<td>-26.6886</td>
</tr>
</tbody>
</table>
From Table 1, it can be observed that as $C_{c2}$ is increasing, $\omega_{z1}$ is decreasing and coming closer to $\omega_u$. For a specific high value of $C_{c2}$, value of $\omega_{z1}$ will be less than $\omega_u$. This condition will make opamp unstable in closed loop. Hence upper range of $C_{c2}$ in this case will be 1.7 pf as can be seen from the table. Further, it can be seen from Table 1 that as $C_{c2}$ decreases poles become complex with low value of $\xi$. This results in poor settling performance. From equations (20) to (23) condition for real poles can be derived as: $\frac{4a}{b^2} \leq 1$. This condition is used to find out the lower limit of $C_{c2}$ as:

$$C_{c2} \geq 4 \times \left[ \frac{1 - R_c \times g_{m2}}{g_{m3}} \times \frac{g_{m3} \times C_L}{g_{m2}} \right]$$

From equation (28) lowest value of $C_{c2}$ can be found out, which provides good settling performance.

**Design Technique**

On the basis of above analysis and discussions design steps for three-stage opamp with NMC can be given as:

**Step 1:** As per the discussions in [10], value of driving voltage ($V_{eff}$) for transistors M1, M2, M3, M4 M9 and M10 is to be set up.

**Step 2:** Constraint of noise sets the value of $g_{m1}$ as discussed section 3.

**Step 3:** Constraint of $\omega_u$ sets the value of $C_{c1}$ as discussed section 6.

**Step 4:** Based on discussion in section 5, $g_{m2}$ and $g_{m3}$ will be chosen to satisfy the power constraint.

**Step 5:** $R_c$ can be found out based on discussion in section 5.

**Step 6:** $C_{c2}$ can be found out on the basis of discussions in section 6 to satisfy the condition of proper placement of poles and zeros.
Step 7: By using basic opamp relationship \( \frac{W}{L} = \frac{g_m}{\mu_n p C_O X V_{eff}} \), aspect ratios \( \left( \frac{W}{L} \right) \) of M1, M2, M10 and M9 can be found out.

Step 8: Current through all three stages can be found out from drain current equation of MOSFET [9]

\[
I_D = \mu_n p C_O X \frac{W}{L} \times \left( V_{eff} \right)^2
\]  

Step 9: Using equation (29), \( \frac{W}{L} \) for transistors M3 and M4 can be found out.

![Figure 5: Three-stage CMOS opamp with NMC.](image)

![Figure 6: Loop-Gain frequency response: Gain and Phase curve.](image)
**Table 1: Circuit Parameters.**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>(W/L)_{1,2}</td>
<td>1.79/0.7</td>
</tr>
<tr>
<td>(W/L)_{3,4}</td>
<td>1/1</td>
</tr>
<tr>
<td>(W/L)_{5,6}</td>
<td>2.49/0.7</td>
</tr>
<tr>
<td>(W/L)_{7,8}</td>
<td>21/0.7</td>
</tr>
<tr>
<td>(W/L)_{9}</td>
<td>40/0.7</td>
</tr>
<tr>
<td>(W/L)_{10}</td>
<td>7.8/1</td>
</tr>
<tr>
<td>IB1,IB2 and IB3</td>
<td>3.3 μA, 10 μA and 50 μA</td>
</tr>
<tr>
<td>C1, C2 and C_L</td>
<td>0.35pf, 0.65pf and 10pf</td>
</tr>
<tr>
<td>R</td>
<td>5.5 KΩ</td>
</tr>
</tbody>
</table>

**Simulation results**

The proposed technique was validated through simulations on Tanner tool, using the model parameters of a 0.35 - μm double metal double-poly process with transistors’ threshold voltages of about 600mV. The following design parameters were assumed: Supply voltage (VDD-VSS) = 2V, CL = 10pF, Slew Rate (SR) = 6V/μs, ωc = 8 MHz, Phase margin (φ (m)) = 65°, S(n) = 40nV/Hz, PD =100 μW. Steps of design techniques proposed in section 7 are used to design the CMOS opamp with NMC shown in figure 1. Aspect ratios $\left(\frac{W}{L}\right)$ of different transistors, biasing currents and compensation elements are given in table 1. Figure 6 shows the open-loop gain and phase variation with frequency. Figure 7 is showing the step response of the designed
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It shows that opamp performance is highly stable with reasonable value of $\omega_v$. By considering the constraints of PD and noise to fulfill the conditions for minimum settling time transconductance and currents of first, second and third stage are obtained as shown in table 2. From the table 2 it can be seen that in the proposed method even though noise and settling performance are poor as compared to earlier methods. But power consumption is reduced by a large amount. In the proposed method SR and $\omega_v$ obtained are 5.76V/μs and 8 MHz respectively. These values are less than the values obtained (10 V/μs, 10 MHz) in earlier methods [5] [6]. Reason for poor values of slew-rate and unity gain frequency in proposed method is very less biasing current available to charge the capacitors at different nodes. Proposed method provides reasonable values of other parameters with low power dissipation.

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<tbody>
<tr>
<td>Transconductance of first stage ($g_{m1}$), second stage ($g_{m2}$), Third stage ($g_{m3}$) in μA/V</td>
<td>14.9, 140 and 615</td>
<td>88, 441 and 1841</td>
<td>250, 500 and 2000</td>
</tr>
<tr>
<td>Biasing currents in first stage (ID1), second stage (ID2), Third stage (ID3) in μA</td>
<td>3.3, 10 and 50</td>
<td>35, 31.5 and 233</td>
<td>40, 35, and 250</td>
</tr>
<tr>
<td>PD (μtw)</td>
<td>14.6</td>
<td>595</td>
<td>650</td>
</tr>
<tr>
<td>Settling time (ns)</td>
<td>155</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>Noise (nV/Hz)</td>
<td>40</td>
<td>7</td>
<td>8</td>
</tr>
</tbody>
</table>

Conclusion

Relationship between settling time parameters and circuit parameters of opamp with NMC is established in this paper. This relationship is explored to obtain the minimum settling time for the given power and noise constraints. Appropriate ratios between the transconductances are obtained to fulfill the conditions of minimum settling time, power and noise constraints. Power efficient shifting of poles is taken under consideration to obtain the optimum ratio of transconductances. Through numerical simulation shifting behavior of poles with Rc is analyzed to find out optimum value of Rc. New method is developed to calculate the compensation capacitor of second stage ($C_2$). Proposed method is suitable for the applications that needed low power with reasonable value of other circuit parameters.

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References


