### Document information

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<td><strong>Keywords</strong></td>
<td>RF power transistor, Doherty architecture, LDMOS, RF performance, Digital PreDistortion (DPD), IS-95, W-CDMA, BLF7G27LS-150P</td>
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<tr>
<td><strong>Abstract</strong></td>
<td>This application note describes 2.5 GHz to 2.7 GHz RF performance tests for a Doherty power amplifier design using the BLF7G27LS-150P LDMOS power transistor</td>
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1. Introduction

This application note describes RF performance tests over the range 2.5 GHz to 2.7 GHz for a Doherty power amplifier design using the BLF7G27LS-150P LDMOS power transistor.

The amplifier uses one BLF7G27LS-150P push-pull device in a Doherty architecture on a 0.76 mm (0.030") thick RF-35 printed-circuit board (PCB). One section functions as the main amplifier for the carrier signal, while the other functions as the peak amplifier for signal peaks. The design ensures high-efficiency while maintaining a very similar peak power capability of two sections of the push-pull device combined. The input and output sections are internally matched, contributing to high gain and good gain flatness and phase linearity over a wide frequency band.

The BLF7G27LS-150P is 150 W push-pull N-channel Enhancement-Mode Laterally Diffused MOSFET: a seventh generation LDMOS device using NXP Semiconductors' advanced LDMOS process.

The amplifier board layout is shown in Figure 1. The component layout is shown in Figure 12 on page 10 and the list of components are given in Table 1 on page 11.
2. Test summary

Amplifier under test: board number: 1298; date code D101003BP.

The amplifier was set up and tested under the following conditions:

- **Frequency band**: 2500 MHz to 2700 MHz
- **Network analyzer measurements** for gain ($G_p$), delay ($\tau_d$) and Input Return Loss (IRL) at:
  - output power ($P_L$) = 43 dBm
  - drain-source voltage ($V_{DS}$) = 28 V
  - main power amplifier quiescent drain current ($I_{Dq (main)}$) = 500 mA
  - gate-source voltage of peak amplifier ($V_{GS (peak)}$) = 0.4 V
- **CDMA Interim Standard (IS-95)** at $V_{DS} = 28$ V, $I_{Dq (main)} = 500$ mA and $V_{GS} = 0.4$ V
- **Peak output power (P3dB) capability**
  - using CDMA IS-95 signal, ratio of peak power to average power = 9.7 dB at 0.01 % probability, $V_{DS} = 28$ V, $I_{Dq (main)} = 500$ mA and $V_{GS (peak)} = 0.4$ V
  - using a pulsed signal and measuring the 3 dB compression points with a pulse width of 12 $\mu$s, 10 % duty cycle at $V_{DS} = 28$ V, $I_{Dq (main)} = 500$ mA and $V_{GS (peak)} = 0.4$ V
- **Digital PreDistortion (DPD) measurements** using a DPD system, 2-carrier W-CDMA signal, 10 MHz spacing, Peak-to-Average ratio (PAR) = 7.4 dB at 0.01 % probability (total signal), $V_{DS} = 28$ V, $I_{Dq (main)} = 500$ mA, $V_{GS (peak)} = 0.4$ V
3. RF Performance

3.1 Network analyzer measurements

Network analyzer measurements were made under the following conditions:

- \( P_L = 43 \text{ dBm} \)
- \( V_{DS} = 28 \text{ V} \)
- \( I_{Dq \text{ (main)}} = 500 \text{ mA} \)
- \( V_{GS \text{ (peak)}} = 0.4 \text{ V} \)

Fig 2. Power gain and input return loss as a function of frequency

Fig 3. Delay and input return loss as a function of frequency
### 3.2 IS-95 measurements

The IS-95 measurements were made under the following conditions:

- Bias: \( V_{DS} = 28 \) V
- \( I_{DQ\text{ (main)}} = 500 \) mA
- \( V_{GS\text{ (peak)}} = 0.4 \) V

![Graph showing power gain and drain efficiency as a function of average output power, IS-95](image)

#### Fig 4. Power gain and drain efficiency as a function of average output power, IS-95

1. \( G_p = 2500 \) MHz.
2. \( G_p = 2600 \) MHz.
3. \( G_p = 2700 \) MHz.
4. \( \eta_D = 2500 \) MHz.
5. \( \eta_D = 2600 \) MHz.
6. \( \eta_D = 2700 \) MHz.

![Graph showing adjacent channel power ratio as a function of output power](image)

#### Fig 5. Adjacent channel power ratio as a function of output power

1. 2500 MHz – 885 kHz.
2. 2500 MHz + 885 kHz.
3. 2600 MHz – 885 kHz.
4. 2600 MHz + 885 kHz.
5. 2700 MHz – 885 kHz.
6. 2700 MHz + 885 kHz.
7. 2500 MHz – 1.98 MHz.
8. 2500 MHz + 1.98 MHz.
9. 2600 MHz – 1.98 MHz.
10. 2600 MHz + 1.98 MHz.
11. 2700 MHz – 1.98 MHz.
12. 2700 MHz + 1.98 MHz.

### 3.3 Peak output power measurements

Two methods were used to measure peak output power.

- Using a standard IS-95 signal (PAR = 9.7 dB at 0.01 % probability on the CCDF), determining the output power where the PAR reaches 6.7 dB at 0.01 % probability on the CCDF, measured as the 3 dB compression point (Figure 6)
- Using the pulsed signal (12 \( \mu \)s width and 10 % duty cycle), measuring the 1 dB and 3 dB compression points (Figure 7)

The peak power measurements were made under the following conditions:
4. DPD measurements

4.1 Test signal

The DPD measurements were made using an in-house designed DPD system under the following conditions:

- 2-carrier W-CDMA signal, spacing: 10 MHz, PAR = 7.4 dB at 0.01 % probability (total signal)
- $V_{DS} = 28 \text{ V}$, $I_{Dq \text{ (main)}} = 500 \text{ mA}$, $V_{GS \text{ (peak)}} = 0.4 \text{ V}$
4.2 2.6 GHz DPD correction

The following DPD measurements were made under the following conditions:

- $f_c = 2.6$ GHz
- $P_L = 45$ dBm
- $IMD = 15$ MHz offset from $f_c$
- $IBW = 3.84$ MHz

Fig 8. Test signal CCDF

4.3 2.5 GHz DPD correction

The following DPD measurements were made under the following conditions:

- $f_c = 2.5$ GHz
- $P_L = 45$ dBm
- $IMD = 15$ MHz offset from $f_c$
- $IBW = 3.84$ MHz
4.4 2.7 GHz DPD correction

The following DPD measurements were made under the following conditions:

- $f_c = 2.7$ GHz
- $P_L = 45$ dBm
- IMD = 15 MHz offset from $f_c$
- IBW = 3.84 MHz

Fig 10. DPD measurement, $f_c = 2.5$ GHz

(1) IMD uncorrected: −30.6 dBc (lower) −29.8 dBc (upper).
(2) IMD corrected: −55.2 dBc (lower) −54.9 dBc (upper).

Fig 11. DPD measurement, $f_c = 2.7$ GHz

(1) IMD uncorrected: −32.3 dBc (lower) −33.5 dBc (upper).
(2) IMD corrected: −54.8 dBc (lower) −54.5 dBc (upper).
5. BLF7G27LS-150P Doherty amplifier board

(1) To ensure RF performance results given in this Application Note, add thin copper to area indicated.

Fig 12. BLF7G27LS-150P Doherty amplifier board component layout
## 5.1 BLF7G27LS-150P Doherty amplifier board components

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
<th>Part identifier</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input PCB</td>
<td>RF35; $\varepsilon_r = 3.5$; thickness 0.76 mm (0.030”)</td>
<td>BLF7G27LS-150P Doherty PA Input-Rev1</td>
<td>Ohio circuits</td>
</tr>
<tr>
<td>Output PCB</td>
<td>BLF7G27LS-150P Doherty PA Output-Rev1</td>
<td>Ohio circuits</td>
<td></td>
</tr>
<tr>
<td>C1, C2, C7, C8</td>
<td>1 μF ceramic chip capacitor</td>
<td>GRM31MR71H105K88L</td>
<td>MuRata</td>
</tr>
<tr>
<td>C3, C4, C5, C6, C9, C10</td>
<td>100 nF ceramic chip capacitor</td>
<td>S0805W104K1HRN-P4</td>
<td>Multicomp</td>
</tr>
<tr>
<td>C11, C12</td>
<td>12 pF ceramic chip capacitor</td>
<td>100B</td>
<td>American Technical Ceramics</td>
</tr>
<tr>
<td>C13</td>
<td>0.2 pF ceramic chip capacitor</td>
<td>100B</td>
<td>American Technical Ceramics</td>
</tr>
<tr>
<td>C14, C15</td>
<td>8.2 pF ceramic chip capacitor</td>
<td>100B</td>
<td>American Technical Ceramics</td>
</tr>
<tr>
<td>C16, C17</td>
<td>100 nF ceramic chip capacitor</td>
<td>GRM21BR71H104KA01L</td>
<td>MuRata</td>
</tr>
<tr>
<td>C18, C19, C26, C27</td>
<td>12 pF ceramic chip capacitor</td>
<td>100B</td>
<td>American Technical Ceramics</td>
</tr>
<tr>
<td>C20, C21, C22, C23, C28</td>
<td>10 μF ceramic chip capacitor</td>
<td>GRM32ER7YA106K88L</td>
<td>MuRata</td>
</tr>
<tr>
<td>C24, C25</td>
<td>2200 μF electrolytic capacitor</td>
<td>PCE3474CT-ND</td>
<td>Panasonic</td>
</tr>
<tr>
<td>C29</td>
<td>0.4 pF ceramic chip capacitor</td>
<td>100B</td>
<td>American Technical Ceramics</td>
</tr>
<tr>
<td>D1, D2</td>
<td>0805 Green SMT LED</td>
<td>APT2012CGCK</td>
<td>KingBright</td>
</tr>
<tr>
<td>L1, L2, L3, L4</td>
<td>Ferroxcube bead</td>
<td>2743019447</td>
<td>Fair Rite</td>
</tr>
<tr>
<td>L5</td>
<td>3.6 nF inductor</td>
<td></td>
<td>Colcraft</td>
</tr>
<tr>
<td>Q1, Q2</td>
<td>78L08 voltage regulator</td>
<td>NJM#78L08UA-ND</td>
<td>NJR</td>
</tr>
<tr>
<td>Q3, Q4</td>
<td>SMT 2N2222 NPN transistor</td>
<td>PMBT2222</td>
<td>NXP Semiconductors</td>
</tr>
<tr>
<td>Q5</td>
<td>BLF7G27LS-150P</td>
<td>BLF7G27LS-150P</td>
<td>NXP Semiconductors</td>
</tr>
<tr>
<td>R1, R2, R7, R8, R12</td>
<td>432 Ω resistor</td>
<td>CRCW0805432RFKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R3</td>
<td>75 Ω resistor</td>
<td>CRCW080575R0FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R4</td>
<td>0 Ω resistor</td>
<td>CRCW08050R0FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R5, R6, R13, R14</td>
<td>1.1 kΩ resistor</td>
<td>CRCW08051K10FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R9, R10</td>
<td>200 Ω potentiometer</td>
<td>3214W-1-201E</td>
<td>Bourns</td>
</tr>
<tr>
<td>R11</td>
<td>2 kΩ resistor</td>
<td>CRCW08052K00FKTA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R15, R16</td>
<td>11 kΩ</td>
<td>CRCW080511K0FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R17, R18</td>
<td>5.1 Ω</td>
<td>CRCW08055R1FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R19, R20, R28, R29</td>
<td>9.1 Ω resistor</td>
<td>CRCW08059R09FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R21, R22</td>
<td>499 Ω/0.25 W resistor</td>
<td>CRCW2010499RFKEF</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R23, R24</td>
<td>5.1 kΩ resistor</td>
<td>CRCW08055K10FKTA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R25, R26</td>
<td>910 Ω resistor</td>
<td>CRCW0805909RFKTA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>R27</td>
<td>100 Ω/1 W resistor</td>
<td>-</td>
<td>Panasonic</td>
</tr>
</tbody>
</table>
6. Abbreviations

Table 2. Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>ACPR</td>
<td>Adjacent Channel Power Ratio</td>
</tr>
<tr>
<td>CCDF</td>
<td>Complementary Cumulative Distribution Function</td>
</tr>
<tr>
<td>DPD</td>
<td>Digital PreDistortion</td>
</tr>
<tr>
<td>IBW</td>
<td>Integration BandWidth</td>
</tr>
<tr>
<td>LDMOS</td>
<td>Laterally Diffused Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Silicon Field Effect Transistor</td>
</tr>
<tr>
<td>PAR</td>
<td>Peak-to-Average power Ratio</td>
</tr>
<tr>
<td>W-CDMA</td>
<td>Wideband Code Division Multiple Access</td>
</tr>
</tbody>
</table>
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