Current Mode Control Integrated Circuit with High Accuracy Current Sensing Circuit for Buck Converter

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Abstract – A current mode control integrated circuit with accuracy current sensing circuit (CSC) for buck converter is presented in this paper. With the proposed accurate integrated current sensor, the sensed inductor current combined with the internal ramp signal can be used for current mode DC-DC converter feedback control. The proposed CSC doesn’t need an op amp to implement, and has been fabricated with a standard 0.35 μm CMOS process. Simulation result show that the switching converter can be operated up to 1MHz with duty-ratio ranging from minimum ON time to 100%. The supply, which is suitable for signal cell lithium-ion battery supply applications, the power efficiency is over 85% for supply voltage from 2.5V to 5V and output current is 200mA. The performance of the proposed circuit is the good compared to the other circuits.

I. INTRODUCTION

In today’s consumer market, battery powered portable electronic devices are in great demand. Portable systems require high frequency and low voltage DC/DC supply converters to efficiently generate low-voltage supplies from a single cell battery source to maximize system run time. To decrease the size and weight of these devices, power module minimization is essential. As a result, the trend is to focus on CMOS converter implementations with low power consumption.

It is well-known that the current-mode control (CMC) DC-DC buck converter has the advantages of automatic over-current protection, better stability, better line regulation and faster dynamic responses compared with the voltage-mode control [1]. It is used for over-current protection and current-mode feedback control. Many different current-sensing schemes have been developed and implemented to sense the inductor current [2-5]. Other current sensing approaches include using a series resistor, power MOSFET on-resistance and even an integrator [4]. However, these schemes have limitations such as high power dissipation, process dependence, control difficulty and high implementation complexity. Therefore, an accurate current sensing circuit (CSC) is necessary for all CMC switch-mode power supplies (SMPS).

Figure 1 illustrates a simplified buck converter structure with CMC integrated circuit. This converter is composed of a power stage and a feedback network. The current sensing circuit function block provides an accurate integrated current sensor. This function block can be used for current mode DC-DC converter feedback control. The power stage contains a switching element, consisting of a power PMOSFET, NMOSFET transistors and an output filter, that is constructed using an inductor L1 and a filtering capacitor C. The output voltage is scaled down to bVo to compare with the reference voltage Vref before feeding into the compensator. The compensator, compensation ramp and sensed inductor current signal output will pass through the modulator and digital control block to define the duty ratio d(t). The duty ratio d(t) controls the on-time and off-time duration of the power transistors. The negative feedback is achieved to control the duty ratio perturbation to regulate the buck converter output voltage V_o.

Therefore, a high accuracy CSC for CMC DC-DC buck converter with a Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm polycide 2P4M CMOS process is proposed. The proposed circuit presents the lowest average power consumption, the highest current-sensing accuracy and the lowest number of MOSFETs since it doesn’t need an operational amplifier or BICMOS process treated as a voltage mirror for the current-sensing scheme. The existing CSC is addressed in section . The operating principle of the proposed on-chip CSC is described in section III. The simulation result is included in section IV. Section V states our conclusions .
II. EXISTING CSC SCHEMES

A high side current sensing amplifier is referenced in the U. S. as Pat. No. 5,627,494 [2]. The high side current sense amplifier is comprised of a feedback resistor, a current sensing resistor, an amplifier and a Darlington transistor pair. The feedback resistor has first and second inputs coupled to a non-inverting amplifier input. The Darlington transistor pair has a collector coupled to the non-inverting amplifier input. A base is coupled to the amplifier output. The current sense resistor is coupled between the emitter of the Darlington transistor pair and ground. A differential voltage is applied across the first feedback resistor input and the amplifier inverting input. The Darlington transistor pair converts the amplifier output voltage into a feedback current for generating a voltage across the feedback resistor. Under stable conditions the voltage across the feedback resistor is equal to the differential voltage. However, the amplifier must used diodes to provide a bias voltage and Darlington pair to generate the current sensing signal. They cannot be used in the low voltage condition.

There are other simple sensing circuits implemented using the standard CMOS process [3]. A circuit and a related method to sense the DC/DC converter inductor current have been achieved. The inductor current is sensed by generating a voltage drop across a fully integrated sense resistor. The voltage drop is proportional to the inductor current in the pass device by supplying a fraction of the inductor current out of a source-follower, which matches the power MOSFET stage. The source-follower source is connected to a sense-resistor that is connected to the same supply as the power MOSFET stage. The passed current of the power MOSFET generates the voltage drop, and feedback into the inductor current for minimizing the power loss. Mirroring amplification and voltage drop offset correction across the sense-resistor are performed using a single matching pair of source-followers. However, the CMOS current mirror cannot provide a good current mirror and thus the accuracy of the current sensing circuit is seriously degraded.

There is another simple sensing circuit implemented using the standard CMOS process. The CMOS high accuracy current sensing circuit depends mainly on the voltage at VA and VB, as shown in Fig. 2 [4,5]. To achieve high accuracy, an operational amplifier is used to force the voltage at nodes A and B into the same voltage level. The two current sources I1 and I2 have small and equal magnitude pulling the current from nodes VA and VB. An output current I o, that flows through the power transistor MP1 is mirrored to the sensing transistor MP2. Any change in VA will force a similar change in VB due to the virtual short-circuit provided by the operational amplifier. Thus, the drain-to-source voltage VDS of transistors MP1 and MP2 are nearly the same, as well as their drain current density. Nevertheless, the transistor MP1 and MP2 are scaled so that power transistor MP1 on the output side of the circuit has an aspect ratio that is much greater than that of transistor MP2 on the sensing side. As a result, the current ISENSE on the sensing side is much smaller than, and proportional to, the current I0 on the output side. The output sensing current ISENSE, which passes through the internal resistor RSEN, is the difference between the sensing current ISENSE flowing through the small biasing current source. Consequently, the current Isense flowing through the internal resistor RSEN is proportional to and substantially much smaller than current I0 flowing through the load. However, this scheme needs an operating amplifier to implement the voltage mirror, which will lead to higher power consumption and number of MOSFET devices.

III. PROPOSED CMC INTEGRATED CIRCUIT

Figure 3 shows the proposed current-sensing circuit. This scheme is modified from the high side current sense amplifier in [2] and the current sensing circuit for buck converter in [3], which can control the output voltage and manage the load current of the buck converter. The CSC of the buck converter is performed by adding a PMOSFET source follower M3 to the PMOSFET power device MP1. A sense-resistor RSEN is connected to the source follower M3 and to the supply voltageVDD. The source of the power device is also connected to VDD. The drain of the power device MP1 and the drain of the source follower M3 are connected to the drain of the synchronous device MN2, which is connected to the buck converter external inductor. In a preferred embodiment, a switching frequency of 1MHZ is used.

The voltage drop across the sense-resistor RSEN is mirrored with a second pair of PMOSFET source followers M4 and M5, working as a common gate amplifier from one side of said pair to the other side. The common gate stage is comprised of PMOS transistors M4 and M5 and resistors R1 and R2. Transistors M4 and M5 have equal conductive width/length such that they conduct equal currents with equal voltage bias. The current mirror stage is comprised of NMOS transistors M8, M9, M10 and M11. The current mirror stage mirrors the
current of NMOS transistors M11 to NMOS M10. The NMOS transistors M8 and M9 are a cascade device that provides high output impedance to the drain of PMOS transistor M8. However, cascade device will limit the Vout maximum value and waste one PMOS threshold voltage in the swing. So that M8 and M9 are biased at the edge of the triode region [6].

The voltage to current output stage provides current feedback to maintain a condition where nodes VA and VB are at an equal voltage. This corresponds to the voltage across resistor R1 being equal to the combined voltage of the differential voltage Vsense and the voltage across resistor R2. The current of PMOS transistors M4 and M5 is approximately I1 in this stable condition. A feedback current I fb and the I1 current of the PMOS transistor M5 combine to generate a voltage drop across resistor R1 to bring the current sensing circuit into balance. Hence, the current IM7 flowing through the internal resistor R4 is proportional to and substantially smaller than the current Io flowing through the load.

In the system design, the current-mode DC/DC buck converter circuit implementation with internal current-sensing technique is addressed and based on the structure shown in Fig. 1. For the power stage of the current-mode converters, the control-to-output transfer function has real poles. The pole from the output filtering capacitor is heavily dependent on the equivalent resistance of the output load R L, the transfer function and angular frequency of the pole are given as [1]:

\[
T(s) = \frac{V_{OUT}(s)}{I_c(s)} = \frac{R_L}{1 + sR_LC}
\]  

(1)

\[
\omega_p = \frac{1}{2\pi \times R_L \times C_L}
\]  

(2)

For dynamic response consideration, pole-zero cancellation is preferable to dominant pole compensation, as the bandwidth can be internal with pole-zero cancellation to speed up the response time. A compensator is used in the feedback network to generate zero for pole-zero cancellation, as shown in Fig. 4. The compensation zero angular frequency in the network characteristic is given as:

\[
\omega_z = \frac{1}{2\pi \times R_z \times C_z}
\]  

(3)

\[
\omega_z \text{ is used to cancel the power stage pole } \omega_p, \text{ so that the loop gain has -20dB/dec rate when it reaches the 0dB line. The compensation values are } R_z (=900k\Omega ) \text{ and } C_z (=100pF ).
\]
transconductance of transistor M1, and goA is the overall conductance at node A. M=5 is the current gain of the current mirror. Figure 6 shows the simulated frequency responses of $y_{in}$ in comparison with an ideal 100pF capacitor. The three corner frequencies of $y_{in}$ are

$$\omega_1 = \frac{g_{oA}}{C_{p2} + (M+1)C_i} \approx \frac{g_{oA}}{C_1}$$  \hspace{1cm} (4)

$$\omega_2 = \frac{g_{ml}}{\left(C_i + C_{pl}\right)} \approx \frac{(M+1)g_{ml}}{C_{pl}}$$  \hspace{1cm} (5)

and

$$\omega_3 = \frac{(M+1)g_{ml}}{C_{pl}}$$  \hspace{1cm} (6)

The leading-edge spike and overshoot are design issues of the current-mode DC/DC converter. The leading-edge spike will be addressed in this section. This problem is on the sensed-current waveform as the power switch turns on. This spike is large enough to prematurely terminate the PWM pulse before regulation. The error signal on the next pulse is larger because of the output drop and the pulse is longer. Over many cycles, the result is PWM-pulse jitter, which is quite visible on a scope. One way of suppressing with this spike is to use leading-edge blanking, which momentarily disables current sensing at the leading edge of power-switch turn-on, preventing premature turn-off. One problem with this approach is that it imposes a minimum duty-cycle limit. Because the current-sense function is effectively blind at the moment of power-switch turn-on, a minimum pulse-width value exists. This problem, which exists at very light loads or no load, causes the output capacitor to overcharge because the duty cycle cannot be low enough. The occurrence of a fault, such as a direct short circuit in the output, delays current limiting, resulting in possibly destructive power dissipation. This signal is used as the oscillator set signal in the proposed method. The set pulse width is 50ns.

The other design issue is the output voltage overshoot. The circuit implementation of the current-mode DC/DC converter with internal soft-start technique is addressed [8] when the current-mode DC/DC converter power is ON. The Vout must rise from its initial value of 0V to its regulated value. Because the Vout is typically initially much lower than its regulated value, the power MOSFET duty cycle during start up can be very high. This situation can cause the inductor current to rise above its equilibrium value, producing inrush current. Moreover, because the current in inductor L1 cannot change instantaneously, it must remain above its equilibrium value for a short time. This can cause the output voltage to rise above its regulated value. This excessive rise is commonly referred as overshoot. This problem has already been addressed in [8]. A so-called “soft-start” capability has been provided to control the inductor current of the current-mode buck DC/DC converter. A block diagram of the soft start is shown in Fig. 6.
In the soft-start function circuit implementation, the ladder-voltage can be generated using a digital to analog converter (DAC). When it increases to some value, the Vout will maintain its value because the DAC output has not changed. This state is like the normal regulation state of the switching regulator. When the next cycle is coming, the DAC output will decrease. The Vout will then increase again. This process will repeat again and again until the end of the soft-start.

IV. SIMULATION RESULTS

The current sensing simulations are based on the circuits shown in Fig. 3. Ideal gate signals are used to drive the power transistors and the two switches, MP1 and MN2 for the DC/DC converter PWM control. The simulation results for the sensing signal and the scale inductor current are shown in Fig 6. The value of inductor L1 is 6.8 μH. The capacitance of the output capacitor C is 47 μF and Rf = 5 Ω, respectively. The ideal gate driver’s switch frequency is 1MHZ and the duty cycle is 50%. When the supply voltage VDD is 3.6V, Fig. 7 shows that the inductor peak current is 436 mA at 247.5 μsec. Figure 8 shows that the current sense circuit signal is 440 mV at 247.5 μsec. The accuracy of the current-sensing is 99.0%. When the supply voltage VDD is 2.5V, the inductor peak current is 316mA at 246.7 μsec, as shown in Fig. 9. In Fig. 10, the current sense circuit signal is 320mV at 246.7 μsec. The current-sensing accuracy is up to 98%.

The system design simulations are based on the circuits shown in Fig. 1. The converter is supplied with an input voltage of 3.6V and switching frequency of 1MHZ. The simulation results for the current-sensing and error-amplifier output signal are shown in Fig. 11. Figure 12 shows the simulation result for the current-mode DC/DC converter with proposed soft-start scheme during the power switch-on. The inductor current is matched to the soft-start with no overshoot.

The efficiency is shown in Fig. 13 with the output voltage of 1.8V and the output current of 200mA. The maximum efficiency is 93.4% at 4.4V input voltage. There are two major power dissipations, conduction loss and switching loss, in the switching-mode power supplies and they depend on the size of the power transistor. For PWM and synchronous rectification control, switching loss is dominant at light and conduction loss is dominant at heavy load conditions. Figure 13 shows that conduction loss is dominant when the input voltage is larger than 4.4V and the efficiency is increased.

The performance of the other current sensing circuits, compared with the simulation results are summarized in Table 1. The proposed circuit has the lowest average power consumption, the highest current-sensing accuracy and the lowest number of MOSFETs since it doesn’t need an operational amplifier as a current mirror. The proposed circuit performance is better than the other CMOS current sensing circuits.
Fig. 10 The waveform of the current sensing signal on supply voltage is 2.5V

Fig. 11 The waveform of the regulated signal on output voltage is 1.8V

Fig. 12 The waveform of the inrush inductor current on power ON with soft-start function

Fig. 13 Efficiency at Vo=1.8v and Io=200mA

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<tr>
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<tbody>
<tr>
<td>Technology</td>
<td>Austria Miko Systeme Integration</td>
<td>Taiwan Semiconductor Manufacturing Company</td>
</tr>
<tr>
<td></td>
<td>AG 0.6um CMOS Process</td>
<td>0.35um polycide 2P4M CMOS Process</td>
</tr>
<tr>
<td>Numbers of core circuit’s MOSFET</td>
<td>44</td>
<td>9</td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td>3V-5V</td>
<td>2.5V-5V</td>
</tr>
<tr>
<td>Accuracy of Current-Sensing</td>
<td>96%</td>
<td>98%</td>
</tr>
<tr>
<td>Need an op amp to as a voltage mirror</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Maximum Operating Frequency</td>
<td>1MHZ</td>
<td>1MHZ</td>
</tr>
<tr>
<td>Maximum Efficiency</td>
<td>89.5%</td>
<td>93.4%</td>
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Table 1: Comparison of the CSC for CMC DC-DC converter

V. CONCLUSIONS

In this paper, the proposed current mode control IC with the current sensing scheme is addressed including the principles of operation, design issues, circuit implementation and simulation results. The results show that the performance of the proposed current sensing technique is more accurate and simpler than the conversional methods. In addition, this technique is not strongly dependent on other parameter variations, such as frequency, temperature and processes. This CMC IC with the CSC can be simply fabricated using any standard CMOS process. From the simulation results of the proposed CMC integrated circuit, the proposed current sensing scheme can successfully operate up to 1MHZ with the duty-ratio ranging from minimum on time to 100%, and the accuracy of proposed current-sensing circuit is 98%. This work will be supported by certification conducted in the
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VII. REFERENCE


