Design of a Continuous-Time $\Sigma\Delta$ Modulator for Bluetooth Receiver in 65nm CMOS

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Outline

• Introduction
• Overview of the continuous-time $\Sigma\Delta$ modulators
• Continuous-time $\Sigma\Delta$ modulator system-level design (MATLAB/Simulink)
• Continuous-time $\Sigma\Delta$ modulator circuit-level design (Cadence/VerilogA)
• Simulation results
• Conclusion
Introduction

RF-Frontend development

- **Trend:** Handsets integrate more wireless services in one chip. (3G, WiFi/Bluetooth/GPS)
- **Challenge:** Considering budget of cost/size/power and hardware updating for legacy standards, a reconfigurable multi-standard, multi-band radio is needed.
- **Solution:** Using SDR, more signal processing shifts from analog to digital domain, thus utilizing the robust digital circuits and process scaling at nanometer level.

![Diagram of SDR](image)

ADC design challenge

- As the interface, ADCs need to provide higher DR, lower power consumption and smaller area.
- Bluetooth requires 1MHz bandwidth, 10-12bits resolution and low power consumption.

**ADCs choices**

<table>
<thead>
<tr>
<th>FLASH (Parallel)</th>
<th>SAR</th>
<th>DUAL SLOPE (Interleaved ADC)</th>
<th>PIPELINE</th>
<th>BISSMA DELTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ultra-high Speed when power consumption not primary concern?</td>
<td>Medium to high resolution (8 to 16bit), 1MHz and under, low power, small size.</td>
<td>Monitoring DC signals, high resolution, low power consumption, good noise performance ICL7106.</td>
<td>High speeds, few Mmps to 150+ Mmps, 8 bits to 16 bits, lower power consumption than flash.</td>
<td></td>
</tr>
</tbody>
</table>

**Solution:** Using SDR, more signal processing shifts from analog to digital domain, thus utilizing the robust digital circuits and process scaling at nanometer level.

![Diagram of ADC in Proposed Low-IF](image)

- **ADCs in a proposed Low-IF**

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Overview of the CT $\Sigma\Delta$ modulators

- **Oversampling $\Sigma\Delta$ ADCs** - use coarse quantizer to realize high resolution

- **Continuous-time (CT) vs. Discrete-time (DT) $\Sigma\Delta$ Modulator**

<table>
<thead>
<tr>
<th>Loop Filter</th>
<th>DT (Hz) SC integrator</th>
<th>$\checkmark$ CT (Hz) Active-RC or Op-amp integrator</th>
<th>Topology/ (Nr. of Quantizers)</th>
<th>Quantizer</th>
<th>Feedback DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed of Operation</td>
<td>Normally less than 100MHz</td>
<td>Clock up to few GHz</td>
<td>$\checkmark$ Single-stage Potential instable for higher-order</td>
<td>Single-bit inherent linear, but bad for jitter</td>
<td>$-$$charge$ redistribution for DT $\checkmark$Current steering for CT</td>
</tr>
<tr>
<td>Power Consump</td>
<td>More with the setting issue</td>
<td>Less</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Anti-aliasing Filter</td>
<td>Necessary</td>
<td>Inherent</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock jitter sensitivity</td>
<td>Low</td>
<td>High $\checkmark$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process variation</td>
<td>Low (capacitor matching well)</td>
<td>High $\checkmark$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Excess loop-delay (ELD)</td>
<td>Low (calculation one clock)</td>
<td>High $\checkmark$</td>
<td>Multi-stage Worse matching between A/D</td>
<td>Multi-bit Improve stability Jitter immunity</td>
<td>Multi-bit Non-Return Zero (NRZ) pulse shape Jitter immunity</td>
</tr>
</tbody>
</table>

- **Therefore**, initially the design targets on a **low-pass single-stage CT $\Sigma\Delta$ modulator** with multi-bit quantizer and NRZ feedback DAC.
Overview of CT $\Sigma\Delta$ modulators

**DT & CT equivalence**

- Usually, begin with mature DT Loop filter, then use equivalence method (IIT) to transfer to CT counterpart

**Rectangular DAC pulse shape**

- Procedure:

1. $u(n) = u_c(t)|_{t=nT_s}$
2. $h(n) = [h_{DAC}(t) * h_c(t)]|_{t=nT_s}$

$$Z^{-1}(H(z)) = L^{-1}(H_{DAC}(s)H_c(s))|_{t=nT_s}$$

CTΣΔ modulator system-level design
(MATLAB/Simulink)

Design Methodology

- Top-down design flow for CT ΣΔ modulators
- System-level design flow for CT ΣΔ modulators

Modulator parameters & LF optimized coefficients

Non-idealities & Solutions

Transfer Function Design and Optimization
- Stable & SNR?
  - good
  - bad
- Stable & SNR?
  - good
  - bad
Add Non-idealities
- Improvement Techniques for non-idealities
  - Achieve Specification? (SNDR, IMD)
    - Yes
    - No
CTΣΔ modulator system-level design

Modulator topology & parameters

- System Level Parameters (N, L, OSR)
- Design targets: 63dB DR over 1MHz, OSR=26
- Survey on published designs of ΣΔ ADCs for Bluetooth application.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Performance (dB)</th>
<th>Loop order</th>
<th>Quantizer level</th>
<th>Signal BW (MHz)</th>
<th>OSR</th>
<th>Process</th>
<th>Power mW</th>
<th>Modulator Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>80</td>
<td>2</td>
<td>17</td>
<td>1</td>
<td>16</td>
<td>2.7V</td>
<td>1.8</td>
<td>DT CIFF</td>
</tr>
<tr>
<td>[2]</td>
<td>81</td>
<td>4</td>
<td>7</td>
<td>1</td>
<td>10</td>
<td>0.1V</td>
<td>75</td>
<td>DT M1NH</td>
</tr>
<tr>
<td>[3]</td>
<td>76</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>0.18V</td>
<td>4.4</td>
<td>CT CIFF Complex</td>
</tr>
<tr>
<td>[4]</td>
<td>88</td>
<td>3</td>
<td>31</td>
<td>1.1</td>
<td>16</td>
<td>0.5V</td>
<td>62</td>
<td>CT CIFF</td>
</tr>
<tr>
<td>[5]</td>
<td>60</td>
<td>2</td>
<td>5</td>
<td>1</td>
<td>24</td>
<td>0.13V</td>
<td>3.2</td>
<td>CT CIFF</td>
</tr>
<tr>
<td>[6]</td>
<td>56.8</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>50</td>
<td>0.18V</td>
<td>22.2</td>
<td>CT CIFF</td>
</tr>
</tbody>
</table>

DR = \frac{P_s}{P_n} = \frac{3}{2} \left( \frac{2L+1}{\pi L} \right) \left( 2^N - 1 \right)^2 OSR^{2L+1}

<table>
<thead>
<tr>
<th>N</th>
<th>2nd-order</th>
<th>3rd-order</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>60.8 dB</td>
<td>78.8 dB</td>
</tr>
<tr>
<td>3</td>
<td>69.7 dB</td>
<td>86.3 dB</td>
</tr>
<tr>
<td>4</td>
<td>74.9 dB</td>
<td>91.9 dB</td>
</tr>
<tr>
<td>5</td>
<td>79 dB</td>
<td>99.2 dB</td>
</tr>
</tbody>
</table>

Chosen 3rd-order 4-bit CT CIFF ΣΔ modulator

![Pole-Zero Plot](image)

- Loop filter NTF design
  - Require SNDR
  - Stability
  - NTF design using DToolbox
  - Separating Zeros makes notch at band edge
  - Moving Poles far from zeros increases Out-of-Band Gain
  - Balance of required SNDR & Stability
  - Ideal 101.5dB @-1dBFS

\[ H(s) = \frac{1.367(s^2 + 0.794s + 0.304)}{s(s^2 + 0.009)} \]
CTΣΔ modulator system-level design

Non-idealities: Excess Loop Delay (ELD) 1

- Delay due to the long switching time of the comparator and DAC responding time. More serious in CT modulator than DT. Although RZ and HRZ is better for ELD, NRZ is chosen here for better jitter immunity.

\[
DAC_{NRZ}(s) = \frac{1-e^{-s\tau_d}}{s}
\]

\[
DAC_{NRZ_d}(s) = \frac{1-e^{-s\tau_d}}{s}e^{-\tau_d s}
\]

E.g. 2nd-order LF

\[
H(z) = \frac{2z^{-1} - z^{-2}}{(1-z^{-1})^2}
\]

One more order!

\[
H(z, \tau_d) = \frac{(2-2.5\tau_d + 0.5\tau_d^2)z^{-1} - (1-4\tau_d + \tau_d^2)z^{-2} - (1.5\tau_d - 0.5\tau_d^2)z^{-3}}{(1-z^{-1})^2}
\]

- Without improving analog circuit, we can use another feedback path to compensate ELD at system level [5].

A proposed 3rd-order CFFE architecture for ELD compensation

\[
LF_m[z] = Z\{L^{-1}\left[(H_m(s) + c_c)DAC(s)e^{-\tau_d s}\right]_{s=\omega T}\}
\]

Using theorems of Laplace & Z-T

\[
LF_m[z] = z^{-1} \cdot Z\{L^{-1}\left[(H_m(s) + c_c / S\right]_{s=\omega T}\} - z^{-2} \cdot Z\{L^{-1}\left[(H_m(s) + c_c / S\right]_{s=\omega T}\}
\]

Mapping coefficients with original H(z)

Non-idealities
Excess Loop Delay (ELD) 2

- For stability consideration, need rescale the modified coefficients, to ensure no overflow happens.

Histograms of three integrators output value after ELD compensation and scaling

Excess loop delay (relative to sampling period Ts)

-60 -40 -20 0 20 40 60 80 100
SNR-3dBFS(dB)

-60 -40 -20 -10 0 10 20 30 40 50 60 70 80

0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4

0.2 0.4 0.6 0.8 1.0

normalized output amplitude w.r.t full scale range
Non-idealities
Clock jitter and DAC pulse shape

- NRZ vs. RZ for multi-bit DAC

Timing error of feedback DAC is not shaped which increases noise floor. Furthermore, compared with the DT modulator (decaying DAC wave form), CT clock jitter generates more charge error. [11]

Random noise model of jitter in DAC

Clock jitter effect on SNDR vs. jitter standard deviation in DAC

\[
\sigma_{\text{SNR}}^2 = \sigma_{\text{DAC,NRZ}}^2 \left( \frac{\sigma_{\text{M}}}{T_s} \right)^2
\]

\[
\text{SNR}_{\text{jitter}} = \frac{P_s}{P_{\text{jitter}}} = \frac{A^2 \cdot \text{OSR}}{2 \cdot \sigma_{\text{DAC,NRZ}}^2 \left( \frac{\sigma_{\text{M}}}{T_s} \right)^2}
\]

\[
\text{SNR}_{\text{NRZ-RZ}} = 10 \log_10 \left( \frac{8 \cdot \sigma_{\text{DAC,NRZ}}^2}{\sigma_{\text{DAC,NRZ}}^2} \right) \text{dB}
\]

Non-idealities
Multi-bit DAC mismatch and DWA

- **Advantages of using multi-bits**
  1) SDNR is increased by 6dB/bit added,
  2) The feedback loop becomes more linear and stable, so NTF can be chosen more aggressive.
  3) Less sensitive to clock jitter for CT modulator

- **Disadvantages:** Element mismatch error can not be noise shaped by the loop filter

- **Current-steering DAC:**
  current source drain current mismatch standard deviation reaches 0.8% using 65nm CMOS Monte-Carlo (1000 runs)

- **Data-Weighted-Averaging (DWA)** algorithm utilizes the 1st-order high-pass noise shaping which is widely used due to its low complexity. It uses all the DAC elements at maximum possible rate and ensure that each of them is used the same number of times.

![Diagram showing SNDR comparison between Bi-DWA DAC, Basic DWA DAC, and No linearization DAC]

- Basic DWA: [1,1,1,..]
- Bi-DWA: [1,-1,1,..]

![Diagram of current-steering DAC circuitry with Modulo-Arithmetic]

![Diagram of data-weighted-averaging DAC configuration]

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2011-5-5 CDNLive! EMEA 2011 Design of a CT ∑Δ Modulator for Bluetooth Receivers in 65nm CMOS
Non-idealities
Integrator non-idealities

\[
\frac{V_o(s)}{V_{in}(s)} = \frac{-1}{s R_{in} C_f b} = \frac{k \cdot f_i}{s}
\]

Just finite Adc

\[
\frac{V_o(s)}{V_{in}(s)} = \frac{-A_{DC}}{1 + s A_{DC} R_{in} C_f b}
\]

Consider both Adc & BW

\[
\frac{V_o(s)}{V_{in}(s)} = \frac{-1}{s^2 R_{in} C_f b A_{DC} \omega b + s(R_{in} C_f b + \frac{1}{A_{DC} \omega b})} = \frac{k \cdot f_i}{s} \frac{1 - GE}{s \frac{1}{\omega_2} + 1}
\]

\[
GE = \frac{k \cdot f_i}{UGBW + k \cdot f_i}
\]

\[
\omega_2 = UGBW + k \cdot f_i
\]

Non-idealities
RC variations

- Integrator gain is determined by RC product.
- On-chip resistor and capacitors vary independently, can depart nominal \(+\)\(-20\%\) result in instability.

\[ C_{in-use} = 4C + k \cdot C \quad (k = 0 \sim 7) \]

- Capacitor array tuning

\[ \frac{C_{max}}{C_{min}} = 2.75 \quad (-50\% \sim 37.5\%) \]

\[ \text{tuning accuracy: } C/8C = 12.5\%. \]
System Level Design Conclusion

• Final 3rd-order 4-bit CT \(\Sigma\Delta\) modulator system-level architecture

• Output spectrum for the modulator in ideal case at system level

• Output spectrum for the modulator with all non-idealities at system level

<table>
<thead>
<tr>
<th>Non-Idealities</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Excess Loop delay</td>
<td>0.9 Ts (Ts=20ns)</td>
</tr>
<tr>
<td>Clock Jitter</td>
<td>1 ps</td>
</tr>
<tr>
<td>DAC Mismatch</td>
<td>0.8%</td>
</tr>
<tr>
<td>1st OpAmp UGBW/DC gain</td>
<td>160MHz/60dB</td>
</tr>
<tr>
<td>RC constant variation</td>
<td>-18%~25%</td>
</tr>
<tr>
<td>Output Swings</td>
<td>-0.6~0.6 V</td>
</tr>
<tr>
<td>Input Referred Thermal Noise</td>
<td>0.5 (\mu) V</td>
</tr>
</tbody>
</table>
**CTΣΔ modulator circuit-level design**

(Cadence/VerilogA)

- Fully-differential 3rd-order dual-loop CIFF loop filter circuit

Coefﬁcients:

\[ k_i = \frac{1}{f_s R C_i} \]
\[ c_1 = \frac{1}{f_s R_{fb} C_1} \]
\[ g_z = \frac{R_2}{R_g} \]
\[ a_1 = \frac{C_{k1}}{C_3}; a_2 = \frac{C_{k2}}{C_2} \]
\[ c_e = \frac{C_{fb}}{C_3} \]

**Pros:**

+ Power efﬁcient
+ More linear than Gm-C integrator realizing feedforward gain
+ Eliminate summing circuit!
+ 1st-stage high driving requirement
CTΣΔ modulator circuit-level design

Telescopic OpAmp

- Telescopic OTA:
  + High speed, lower power consumption, lower input thermal noise compared with 2-stage, folded-cascode.
  - Output swing is limited! At system level, coefficients was scaled to ensure the output swing of each stage is not too large. (I=0.6~0.6) with FS input.)

- Common-mode feedback (CMFB)

![Diagram of CTΣΔ modulator circuit-level design](image-url)
CTΣΔ modulator circuit-level design
Modulator front-end noise analysis

- Simulation in MATLAB: shows more than 25μ_rms thermal noise injected at input, more than 15dB SNR drop in-band.

- Noise simulation summary in Spectre:

<table>
<thead>
<tr>
<th>Noise summary</th>
<th>Main contributor</th>
<th>Value (V)</th>
<th>SNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st-integrator and Rfb</td>
<td>M7.8: 29.5% flicker</td>
<td>3.56μVrms</td>
<td>85.6dB</td>
</tr>
<tr>
<td></td>
<td>M1.2: 12.6% flicker</td>
<td>1.52μVrms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rin: 1.36% thermal</td>
<td>0.165μVrms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rfb: 3.78% thermal</td>
<td>0.456μVrms</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>47.24%</td>
<td>Total input referred noise: 124 pV^2</td>
<td></td>
</tr>
</tbody>
</table>

- Noise sources
1) 2 input-resistors and feedback-resistors:
\[ V_{Rin}^-^2 = 8kT(R_{in} + R_{fb})\Delta f \] Lower than Q-noise power

2) 1st-OpAmp:
Thermal:
\[ V_{in,thn}^-^2 = 8kT_f \cdot \frac{2}{3} \left( \frac{1}{g_{m7}^2} + \frac{g_{m1} + g_{m,nbias}}{g_{m7}^2} \right)\Delta f \]
Flicker:
\[ V_{in,flt}^-^2\Delta f = 2 \left( \frac{k_p}{(WL)_1 C_{ox} f} + \frac{k_N}{(WL)_1 C_{ox} f} \frac{g_{m7}^2}{g_{m1} + g_{m,nbias}} \left( \frac{g_{m,nbias}}{g_{m7}^2} \right) \right) \ln \left( \frac{f_{max}}{f_{min}} \right) \]
CTΣΔ modulator circuit-level design
OpAmp and loop filter simulation results

- 1st-OpAmp Simulation results
  ![1st-OpAmp Simulation results](image1)

- Loop filter Schematic simulation
  fin=301.5KHz, -6dBFS, 16384FFT
  ![Loop filter Schematic simulation](image2)

- OpAmp Simulation vs. Specification
  ![OpAmp Simulation vs. Specification](image3)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
<th>Simulations -op1 op2 op3</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain (dB)</td>
<td>&gt;60</td>
<td>64/64/64</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>&gt;170</td>
<td>172.7/500/500</td>
</tr>
<tr>
<td>3-dB (kHz)</td>
<td>&gt;200</td>
<td>150/433/333</td>
</tr>
<tr>
<td>PM (degree)</td>
<td>&gt;50</td>
<td>54.7/63.2/63.2</td>
</tr>
<tr>
<td>Output Swing (mVoltage)</td>
<td>≤600</td>
<td>±755/755/755</td>
</tr>
<tr>
<td>Power Dissipation (mW)</td>
<td>As low as possible</td>
<td>2.64/0.4/0.41</td>
</tr>
<tr>
<td>Resistor Load (ohms)</td>
<td>Single-end: 33K/82K/1.33M</td>
<td></td>
</tr>
<tr>
<td>Capacitor Load (f)</td>
<td>Single-end: 25p/4p/4p</td>
<td></td>
</tr>
<tr>
<td>VDDA/VSSA</td>
<td>1.2V/0V</td>
<td></td>
</tr>
</tbody>
</table>
CTΣ∆ modulator circuit-level design

Wide-swing constant-Gm bias circuit

- Off-chip resistor to stabilize the Gm

Simulation results:

\[ g_{m3} = \frac{2 \left( 1 - \left( \frac{W}{L} \right)_3 \right)}{\left( \frac{W}{L} \right)_2} \]

\[ g_{mi} = \frac{\mu_m (W/L)_3 I_{D3}}{\mu_m (W/L)_2 I_{D2}} \cdot g_3 \]

All current derived from this bias network. Its Gm is stable!!!

DAC bias tuning: 3.9% - 3.16%
CTΣΔ modulator circuit-level design
Sample and hold circuit

- **Problem arises**: Large sampling capacitors in the comparator make settling problem. S&H is used to flat the input of quantizer
- **Sample and Hold** Isshikawa

**Design Criteria:**
- KT/C noise: accuracy, get $C_2 \tau$
- Finite acquisition time: speed, get $g$ and $R$
- Switch-on resistance: distortion, large W/L
- Charge injection: DC offset, GE, distortion

- **S&H and Comparator**
- **Comparator input offset cancellation (IOS)**: widely in the multi-bit quantizer since it has wide input common mode range. [8]

$$V_{OS} = \frac{V_{OSL} + \Delta g}{1 + A_0} + \frac{V_{OSL}}{C_x A_0}$$

CTΣΔ modulator circuit-level design

Flash ADC

- 4-bit flash ADC
- Comparator

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CTΣ∆ modulator circuit-level design

Clock generator

• CLK generator

• Variable Delay cell: in the test chip, for the sake of flexibility.

10~20ps rising and falling time
**CTΣΔ modulator circuit-level design**

**Current-steering DAC**

- **Critical part**: require high linearity (better than whole modulator) and fast speed.
- **Problem**: current source mismatch and output impedance [8]

Thermometer code is monotonic originally, then by using DWA the element mismatch issue is compensated. However, the glitch problem becomes worse since at some switching instance more bits change. **High crossing switch scheme** minimize the glitch energy.

![Diagram](image)

Design from output impedance requirement [8]:

\[
R_{out} \approx \frac{I_{unit} R_L N^2}{4INL} \quad R_L = \frac{VFS_{DAC}}{N_{unit}}
\]

\[
R_{out} \approx \frac{N_{R_L}}{4SFDR}
\]

\[
R_{out} \approx g_{m1} g_{m2} r_{o1} r_{o2} r_{o3} r_{o4} \propto L_1 \cdot \sqrt{W_2 L_2} \cdot \sqrt{W_3 L_3} \cdot \sqrt{W_4 L_4}
\]

- Clock feedthrough; Switch-on resistance; DWA (delay)
- Good current-steering DAC design should be further studied.

Simulation results 1

- Co-simulation results without DAC mismatch.
- Tools: Cadence Virtuoso IC5141_USR6, Spectre MMSIM7_10_034 Matlab/Simulink
- All transistor-level transient simulation for 150us takes about 1 week! So using VerilogA to co-simulate the circuit allows an incremental design. Consequently, it is easy to debug the whole circuit.

**Parameters and simulations results**

<table>
<thead>
<tr>
<th>Non-ideality</th>
<th>Figure 5.1 (a)</th>
<th>Figure 5.1 (b)</th>
<th>Figure 5.1 (c)</th>
<th>Figure 5.1 (d)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC Mismatch</td>
<td>none</td>
<td>none</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>1st integrator</td>
<td>Verilog A-Matlab</td>
<td>Schematic</td>
<td>Schematic</td>
<td>Schematic</td>
</tr>
<tr>
<td>2nd integrator</td>
<td>Verilog A-Matlab</td>
<td>Schematic</td>
<td>Schematic</td>
<td>Schematic</td>
</tr>
<tr>
<td>3rd integrator</td>
<td>Verilog A-Matlab</td>
<td>Schematic</td>
<td>Schematic</td>
<td>Schematic</td>
</tr>
<tr>
<td>OpAmp model: Matlab=VerilogA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1st OpAmps gain-error</td>
<td></td>
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</tr>
<tr>
<td>DAC: 0.75-0.75V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW1: 0.75-0.75V</td>
<td></td>
<td></td>
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<tr>
<td>SFDR: 0.75-0.75V</td>
<td></td>
<td></td>
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<tr>
<td>SNR: 0.75-0.75V</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ADC: 0.75-0.75V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quantizer model: VerilogA=Schematic</td>
<td></td>
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</tr>
</tbody>
</table>

**Dynamic Range (using condition (b))**

- Dynamic Range (using condition (b))
- OpAmp model: Matlab=VerilogA
- DAC non-linearity introduce HD2
- Quantizer model: VerilogA=Schematic

2011-5-5 CDNLive! EMEA 2011 Design of a CT ∑Δ Modulator for Bluetooth Receivers in 65nm CMOS
Simulation results 2

- DAC mismatch cancellation verification
- Co-simulation using DAC Monte-Carlo mismatch model (16384FFT)

- Summary of final simulation results and performance estimation

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Simulation results and estimation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Co-simulation Model of Figure 5.1(b)</td>
<td>Transistor-level Model of Figure 5.1 (d)</td>
</tr>
<tr>
<td>Peak SNDR/SFDR @ 301.5KHz</td>
<td>78.6dB/79.8dB (simulated)</td>
</tr>
<tr>
<td>Dynamic Range/ENOB</td>
<td>84dB/13.7ENOB (simulated)</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>52MHz</td>
</tr>
<tr>
<td>Oversampling Ratio (OSR)</td>
<td>26</td>
</tr>
<tr>
<td>Power consumption</td>
<td>7.8mW (Analog &amp; AD/DA)</td>
</tr>
<tr>
<td>Process</td>
<td>65nm, 1.2V TSMC</td>
</tr>
</tbody>
</table>

- Noise contribution:
  - Analyzed at system level, 1ps jitter noise effect drops SNDR about 10dB
  - Simulated at circuit level 11uVrms thermal noise drops SNDR more than 15dB
Conclusion

• **Summary**
  - 3rd-order loop filter with reasonably large OBG and optimized NTF notches, to provide sufficient noise shaping for in-band quantization and internal sampling error noise.
  - Multi-bit quantizer is used to further reduce the quantization noise and ensure the higher-order single loop stability.
  - Dual-loop feedback is used to relax the excess loop delay up to one sampling period.
  - Non-Return-Zero multi-bit DAC is used to reduce the clock jitter sensitivity.
  - Capacitive tuning is used to overcome the time-constant shift due to process variation which influences the CT modulator performance significantly.
  - DWA digital block is used to suppress the multi-bit DAC mismatch error.

• **Future work**
  - The feedback DAC should provide more linearity performance. It is supposed to use a Switch-Capacitor DAC with exponentially decaying pulse shape. This innovative choice for CT modulator design is worth exploring since it can also reduce the jitter sensitivity.
  - The loop filter transfer function of modulator should be designed less sensitive to clock jitter which is a big problem to be resolved in this work.
  - The 1st -OpAmp in the modulator which drives a big load capacitor should be designed more robust without losing UGBW and phase margin, meanwhile 2nd and 3rd OpAmp which are not as critical as the 1st one can be designed with lower UGBW, hence reducing the power consumption.
  - The transistor-level design should be completed for the next layout of the entire modulator.

• Combine all the techniques, the modulator transistor-level simulation result could achieve 80dB DR over 1MHz bandwidth without jitter or device noise. Sampling clocking is 52MHz, and power consumption is 7.8mW at 1.2V supply.
Thank you for your attention!
Any questions?

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