RESEARCH

The Study and Design Of a Wireless ECG Monitoring System

Hongli Yang and Jihong Chai

Abstract
This paper describes a research project on wireless electrocardiogram (ECG) monitoring systems. A detection and measurement processor designed by a MSP430 microcontroller accomplishes the analog-to-digital conversion, digital filtering, QRS wave detection, and heart rate calculation. The data of detection can be sent to the central controller and personal computer (PC) by wireless on-chip MG2455 through a ZigBee network. This design can be used widely in home healthcare, community healthcare, and sports training, as well as in healthcare facilities, due to its characteristics of low power consumption, small size, and reliability.

Introduction
The electrocardiogram (ECG) is one of the most important tests for diagnosing heart disease and a widely used tool in monitoring a patient’s condition. With the rapid evolution of technology, the use of ECG monitoring is growing, especially outside traditional hospitals, turning up, for example, in home healthcare and sports training. But with these new uses come new needs. Many current ECG monitors cannot meet these requirements because they consume too much power, are too big, cannot record ECG waves continuously, and cannot transmit easily.

With new ways of communicating and exchanging information and with new developments in medical device technology, it is possible to achieve a kind of remote wireless ECG monitor. This paper examines one example on a wireless ECG monitor system, which is designed both on the microprocessor MSP430 and on the on-chip ZigBee wireless network. This design can be used in both home healthcare and sports training settings.

System Description
The designed ECG monitoring system is generally composed of two parts—the monitor terminal and the central controller. The wireless monitor terminal would be worn by the monitored person. The ECG signal would be sampled and collected from the electrode, and then be amplified and filtered by the analog circuits. The single chip MSP430 microcontroller converts the amplified analog signal into the digital signal, processed by the digital filter and then calculates the heart rate. All the processed data and parameters will be sent to the wireless transmitter through the serial port. Lastly, the processed data will be sent to the central controller through the wireless network. The central controller consists of the ZigBee receiver and a personal computer (PC), which can receive the processed data. The ZigBee network could establish a point-to-point connection or a point-to-multipoint connection.

About the Authors
Hongli Yang is an associate professor in the Department of Electrical Engineering at Shenzhen Polytechnic in Shenzhen, China. One of her specialties is medical device design. E-mail: szyhl@126.com

Jihong Chai is a lecturer in the Department of Electrical Engineering at Shenzhen Polytechnic in Shenzhen, China.

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between central controller and monitor terminals, which would have three kinds of topology—Star networks, Tree networks, and Mesh networks. Figure 1 is a block diagram of the Star network.

**Design of Monitor Terminal**

The monitor terminal would start at the ECG electrodes, which would be connected to the person being monitored. The blocks of the monitor terminal are analog amplifier, microcontroller MSP430 (we choose the four-series chip MSP430FG439), and wireless transmitter in the order shown as in Figure 2.

The collected ECG signal from the electrodes is generally weak and cannot be processed directly by the filters. Therefore, a pre-amplification is needed before it can be sent out to the filter. The pre-amplifier is a type of CMOS instrumentation amplifier INA321. The gain is only up to 5. There is a 50Hz notch filter following the pre-amplifier, which eliminates 50Hz industrial electricity interference effectively. The internal operational amplifier of MSP430FG439 provides the majority amplification. It has the gain of 100 with a total gain of 500(5x100=500). Thus, the amplitude of ECG signal can get high enough to implement analog-to-digital conversion. The sampled data can be sent wirelessly to a central controller after the 12-bit analog-to digital conversion and digital filter. The digital filter, which is executed by the software program, would eliminate the high-frequency interferences.

**A. MSP430FG439 Function**

The core element of monitor terminal is the microcontroller MSP430FG439. It is a 16-bit processor. It features very low power consumption, high integration, high memory capacity, online processing, and is easy to interface with a wireless on-chip system.

- **Low power consumption**: Power consumption is 300 μA when it is on active mode at 1 MHz, 2.2 V, while standby mode is 1.1μA, and off mode is only 0.1μA. Low supply voltage range is 1.8–3.6V. Five power save modes are LPMO, LPM1, LPM2, LPM3, and LPM4. These features maintain the low power consumption.

- **Rich on-chip integrated module**: Watch-dog timer; integrated LCD driver for up to 128 segments; two serial communication Interface (USART0); 16-BitTimer_A and Timer_B with three capture/compare-with-shadow registers; 12-Bit A/D converter with internal reference, sample-and-hold and auto scan feature; three configurable operational amplifiers OA0, OA1, OA2.

- **Powerful processing ability**: 16-Bit RISC architecture; 125-ns instruction cycle time. serial onboard programming. The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data.

**B. Wireless Transmitter**

MG2455TA1 meets the requirement for short distance wireless communication. It is a standard microprocessor and transceiver with Zigbee protocol. Data transmission can be achieved point to point, point to multipoint, or multipoint to multipoint. The chip can communicate over long distances, has good anti-interference ability, network design flexibility as well as excellent stability. Three kinds of topology—Star networks, Tree networks and Mesh networks—can be built. Both broadcast
mode and object addresses mode are applied in the data transmission design.\(^6\)

C. Amplifier and Filter

There are three units in the analog circuit: front end pre-amplifier, double-T filter, and a main operational amplifier.\(^7\)

Prior to the pre-amplifier circuit, there are low pass filters (R\(_5\), R\(_7\), C\(_2\), and C\(_4\)) on each electrode input to block RF above several kHz. The components NE2H constitute high-voltage protection circuit. They can protect the device from damage if it is attached to a patient while that patient is defibrillated. The two neon bulbs NE2H are in the off state and have no function under normal circumstances. They will switch to on while the input electrodes have high-voltage pulse. The high voltage will be discharged, and most of high-voltage energy will be consumed. Thus, the subsequent amplifiers and circuits can be protected.

The pre-amplifier must have high input impedance, high common mode rejection ratio, as well as low zero drift. Because of the high contact resistance and common mode voltage, the gain of pre-amplifier must not be too large to bring saturation distortion. The differential amplifier used in the front end of this application is an INA321 instrumentation amplifier that has perfectly matched and balanced integrated gain resistors. This device is specified to operate with a minimum of 2.7V single rail power supply. The INA321 provides a fixed amplification of 5X for the ECG signal. With its CMRR specification of 94 dB extended up to 3 kHz, the INA321 rejects the common-mode noise signals including the line frequency and its harmonics. D1 and C8 are implantable pacemaker pulse rejection circuit. It can reduce the amplitude and enlarge the cycle of pacemaker pulse. Thus, the pulse cannot be collected and recorded.

The frequency range of ECG is 0.05Hz-100Hz. The main factor interfering with ECGs is the industrial electricity power frequency signal, which is 50-Hz/60-Hz. In order to obtain clear ECGs, the circuit should have a band pass filter and 50-Hz/60-Hz notch filter. A double T filter is adopted in this design which includes R\(_6\), R\(_7\), R\(_8\), C\(_2\), C\(_3\) and C\(_4\). The double T filter can be replaced by an adaptive software notch filter. The adaptive notch filter needs not to know the accurate interference frequency. It has the ability of automatic frequency tracking, thus it is most adaptive to remove power-line frequencies. Low pass filter is done via the 3.9 nF capacity in parallel with the OA0’s 1MΩ feedback resistor. The -3dB corner frequency is about 41Hz.

The main operation amplifier is the internal configurable operational amplifier OA0 in MSP430FG43. OA0 is configured to get a 100 gain. The voltage after OA0 is about 1V, enough to digitize with reasonable resolution. Because of the large amplification factor, the output is sensitive to the variations in DC offset of the electrodes to skin contact resistance. This results in a variation of the DC content of the amplified differential signal and manifests itself as a drift in the baseline of the ECG. This is popularly called baseline wandering and often causes wavy traces of the ECG. This issue is managed by using an analog integrator scheme designed with OA1. The integrator integrates the DC content of the 5X amplified ECG and feeds it back to the INA321. The feedback allows the INA321 to maintain a constant DC level at the output, regardless of the change in skin contact resistance. At the same time, the integrator acts as a high pass filter. The effective high pass corner frequency of this as drawn is the 0.48 Hz due to the integrator time constant R\(_5\)C\(_1\).

D. Software Design

The first step of the program design is ADC. The amplified ECG signal is internally fed to the on-chip analog-to-digital converter ADC12 input channel A1. The ADC12 samples the ECG signal with a sampling frequency, f\(_{sample}\), of 512 Hz. Precise sampling sample period is achieved by triggering the ADC12 conversions with the Timer_A pulses. Timer_A is clocked by ACLK, which is generated from the 32.768-kHz low-frequency crystal oscillator.

Secondly, the sampled ECG waveform contains some amount of superimposed line-frequency content. This line-frequency noise is removed by digitally filtering the samples. A 17-tap low-pass FIR filter is implemented in this application. The filter coefficients are scaled to compensate the filter attenuation and provide additional gain for the ECG signal at the filter output. This adds up to a total amplification factor of greater than 1000. In order to calculate the heartbeat accurately,
the QRS complex must be detected for every beat. Finally, both the sampled and filtered ECGs signal and heart rate are sent to MG2455 and transmitted wirelessly.

The flow diagram shown as Figure 3 includes a main program and several interrupt subroutine program. Detector terminal would be switched into low-power consumption mode after initialization and until the interrupt is active.

**Design of Central Controller**

The central controller includes two units: the wireless receiver and central PC. The wireless receiver coordinates and receives all the data from the terminals. All data will then be sent to the PC and be displayed on the screen. The wireless receiver is the same type chip MG2455TA1 as the detector terminal. RS-232 is used to connect the receiver and PC. Visual Basic language program used in PC implements the display interface design. The block diagram is shown as Figure 4.

For the receiver, the main task is establishment of the communication protocol between the detection terminal and central controller. The protocol has three layers, such as physical layer, data link layer, and application layer. There are two information transmission modes in the network. In one mode, the central controller acts as the administrator to set up the polling and request instructions sent to the monitor terminal for the physiological parameters. The instructions are transmitted to the detection terminal node worn by the patient through ZigBee wireless network. The monitor terminal then performs signal acquisition and detection immediately, and then returns detected data to the central controller.

In the other mode, the initial transmission request would be initiated by the monitor terminal. After the request message is sent out, the monitor terminal then waits for the confirmation message from the central controller. If the request is confirmed, the data transmission...
process is set up the same way as in the first mode. For example, the monitor terminal will send a 8-bit data “11111111” to central controller when it needs transmit data. The central controller will resend a 8-bit data “00000000” to the monitor terminal after receiving the data “11111111” from the monitor terminal. The communication between them can proceed. We define these datas as a “handshaking” signal. In other words, in this mode, the monitor terminal should first send out the handshaking signal to the central controller, and then send the patient physiological parameter data after receiving a handshaking confirmation signal from the central controller. Therefore, in the development of the application layer protocol, the relationship between the central controller and the monitor terminal is in the master-and-slave mode. The software flow chart of the monitor terminal data transmission is shown in Figure 5.

Conclusions
In this paper, the design of a wireless ECG monitor system based on ZigBee technology is presented. The new ECG system breaks the traditional medical care mode, and makes full use of this advancing ZigBee technology and rich resources in MSP430FG439. For patients with chronic illnesses such as heart disease or for the athlete in training, the system can provide a useful approach for continuous health monitoring.

The paper also proposes a model for a prospective healthcare system for the future in which the hospital, as the information processing center, is connected to communities, families, and individuals through the Internet and the wireless LAN, leading to the formation of an organic system. The system will ensure that individuals both in and out of hospitals— and even in remote areas—can receive timely, effective, and professional medical diagnosis and treatment recommendations. It will thereby significantly improve the delivery of healthcare and the quality of people’s lives.

References